

MODEL NAME : Aventador

PCB NO : LA-D781P

BOM P/N : TBD



	R1	R3	R3	R3
CPN	DAA000CE010	DAA000CE011	DAA000CE012	DAA000CE013

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Schematic Document

Aventador (Kabylake Y)

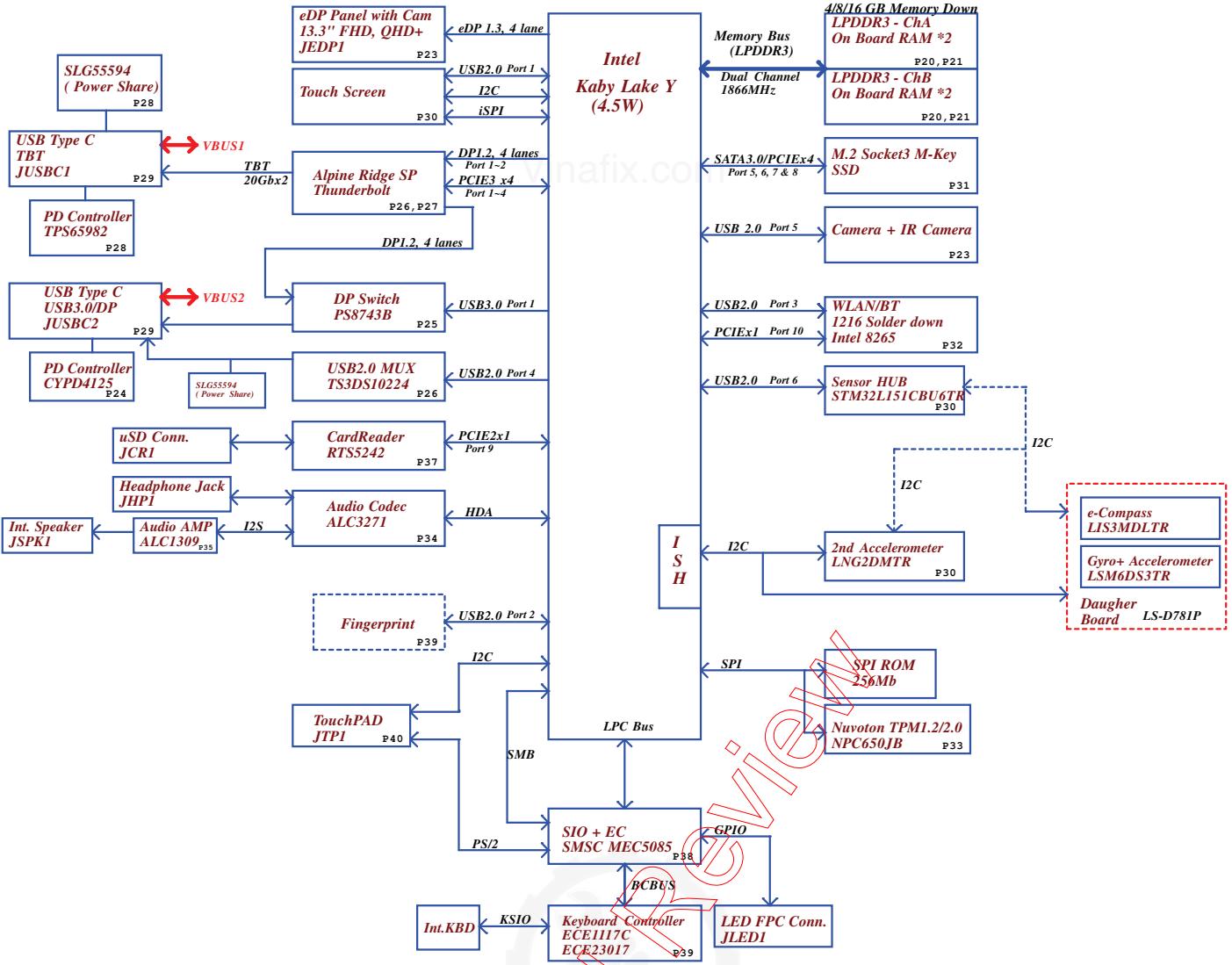
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nVpro CPU Option				
UC1 QLD@ SA0009A20L HE8067702739525 QLD0	UC1 QLDR@ SA0009A40L HE8067702739823 QLD1 HE8067702739824 QLD5	UC1 QLDS@ SA0009A41L HE8067702739823 SR2Z	UC1 SR2Z@ SA0009A40L HE8067702739526 QLY7	
Vpro CPU Option				
UC1 QLDV@ SA0009A20Q HE8067702739525 QLDV HE8067702739527 QLY8 HE8067702739526 QLY7	UC1 QLYB@ SA0009A20L	UC1 QLYT@ SA0009A20L		

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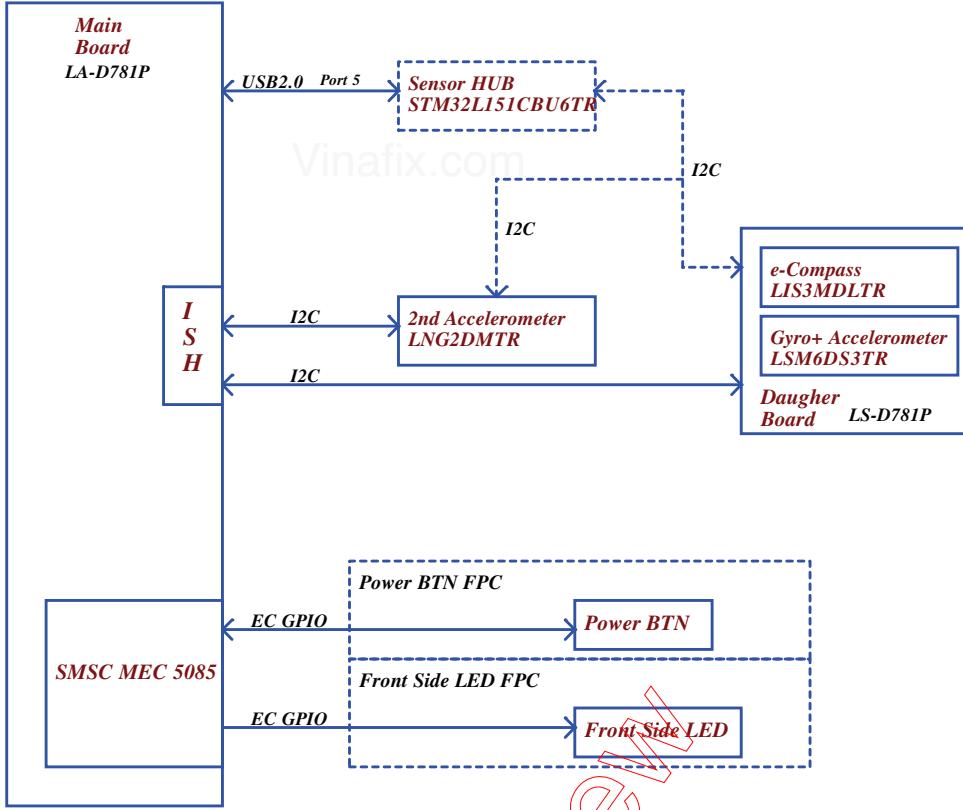
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POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF		LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

Power plane	+3VAILW_DSW +5VALW +3VBLW +3VLP	+3V_PCH +1.8V_PRIM +1.8V_PRIMATE +1.0V_VCCST	+1.2V_DDR +3.3V_CV2 +1.8V_MEM +1.0V_VCCST	+5VS +1.8VS +0.85VS_VCCIO +VCC_SA +VCC_GA +VCC_CORE
S0	ON	ON	ON	ON
S3 /AC	ON	ON	ON	OFF
DS3	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

Control Table

		MEC5085	BATT	XDP	USH	TI PD	CCG4	ECE1117	AMP	Charger
SMIOLCLK	SMBDATA	PCH								
SMII_SMBCLK	SMBDATA	PCH	V							
SMBCLK	SMBDATA	PCH		V						
MCP23017_SMBDAT	MCP23017_SMBCLK	MEC5085				V				
UPD_SMBDAT	UPD_SMBCLK	MEC5085				V				
EC_I2C_CLK	EC_I2C_DAT	MEC5085					V			
PBAT_SMBCLK	PBAT_SMBDAT	MEC5085		V						
CCG4_I2C_CLK	CCG4_I2C_DATA	MEC5085				V				
CHARGER_SMBCLK	CHARGER_SMBDAT	MEC5085					V			

Board ID Table

Vcc	3.3V +/- 5%	R	C	PCB Revision	REV
0	240K +/- 5%	4700p	0.1	EVT1.0	
1	130K +/- 5%	4700p	0.2	DVT1.0/DVT1.1	
2	62K +/- 5%	4700p			
3	33K +/- 5%	4700p			
4	8.2K +/- 5%	4700p			
5	4.3K +/- 5%	4700p			
6	2K +/- 5%	4700p			
7	NC				

SOC DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
SOC PCIE Port Mapping	2	Alpine Ridge
	Lane 1	Alpine Ridge
	Lane 2	
	Lane 3	
	Lane 4	
	Lane 5	NGFF (SSD)
	Lane 6	
	Lane 7	
	Lane 8 / SATA 1	
	Lane 9	Cardreader
	Lane 10	WLAN
CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	Alpine Ridge
	CLKOUT_PCIE2	WLAN
	CLKOUT_PCIE3	SDD
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	

USB 3.0 PORT#	DESTINATION
1	USB DP MUX
2	USB Debug
3	
4	
USB 2.0 PORT#	DESTINATION
1	USB Type C (nAR)
5	Sensor Hub
7	Fingerprint
3	Touch Panel
9	CAM & IR CAM
2	NGFF(WLAN)

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	LPC Debug

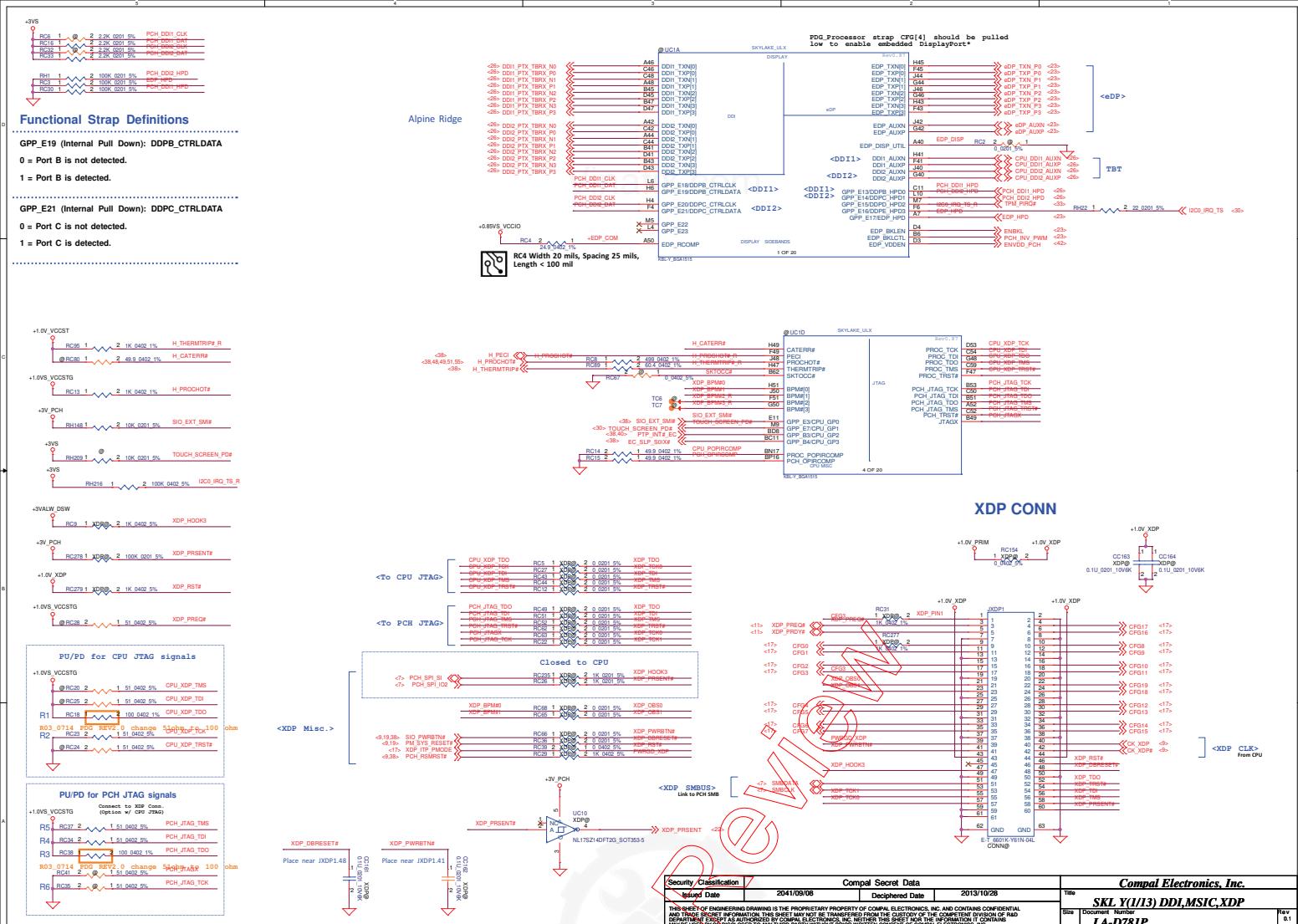
Symbol Note :

@ : means de-pop

▽ : means Digital Ground

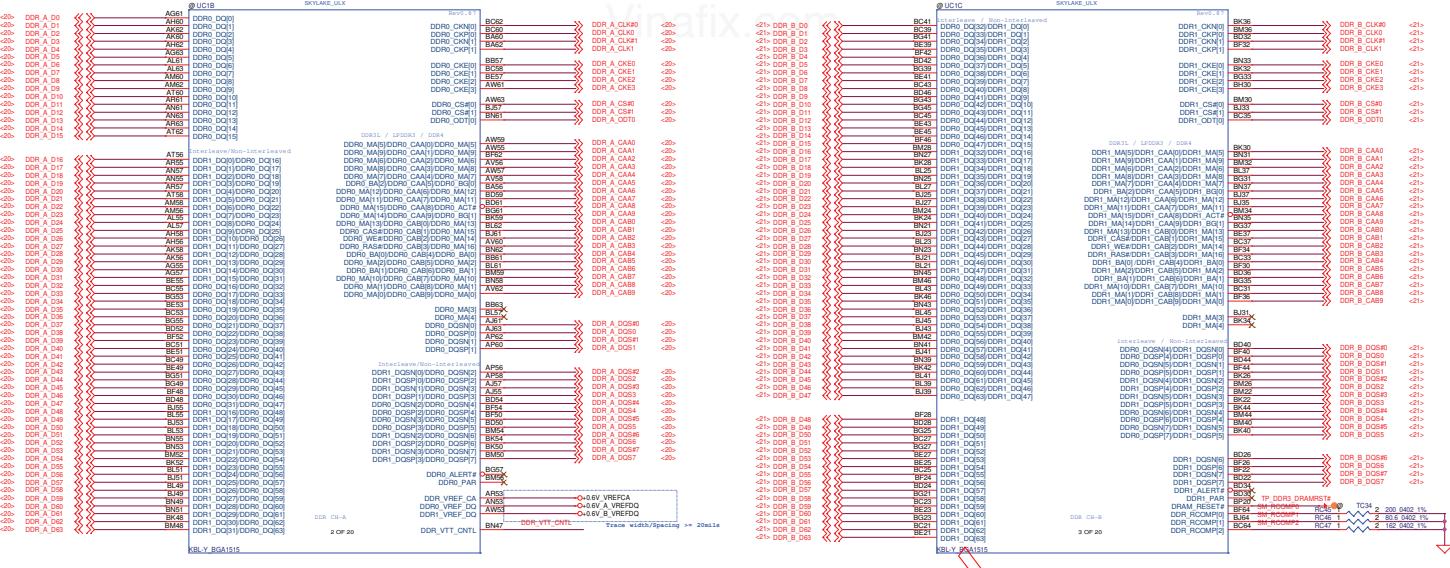
— : means Analog Ground

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For Dell

Non-Interleave Memory



DDR_VIT_CNTL RC48_1 2 0 0402 5% ➡ SM_PG_CTRL

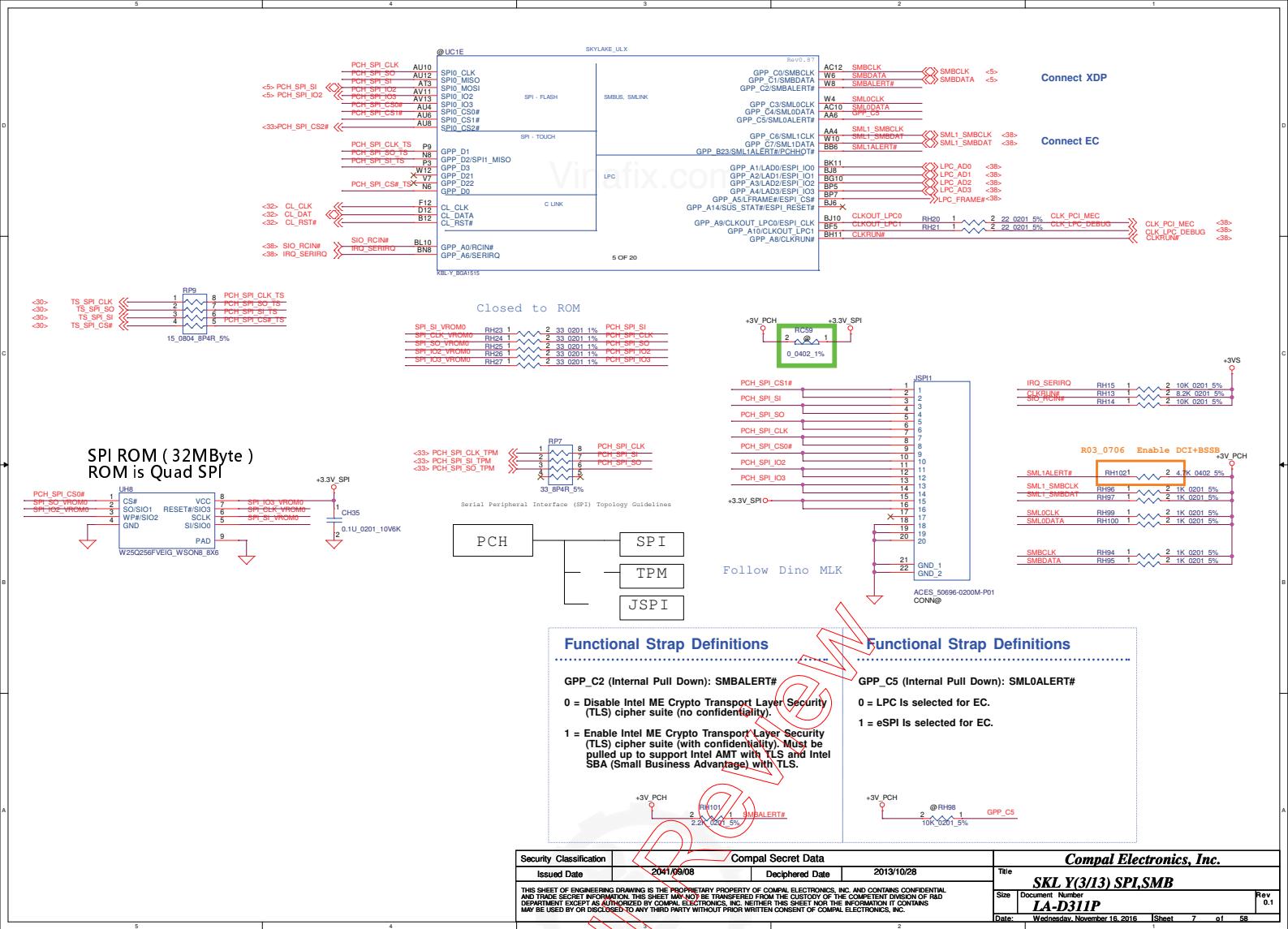
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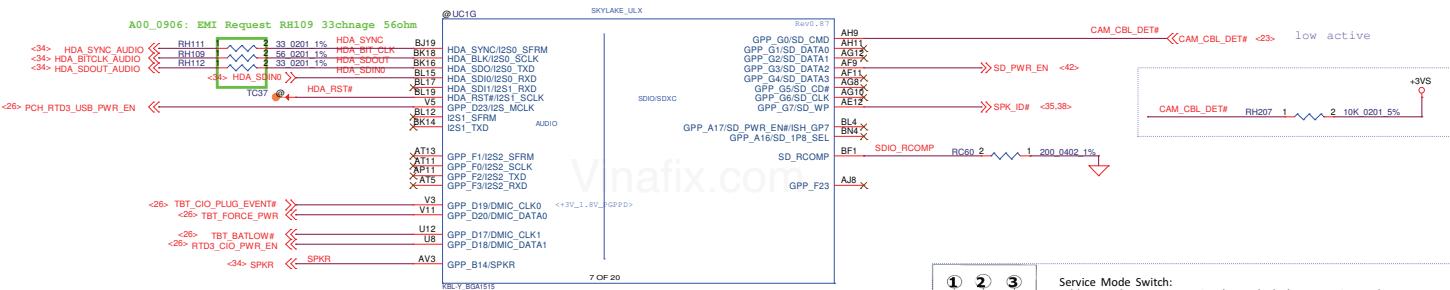
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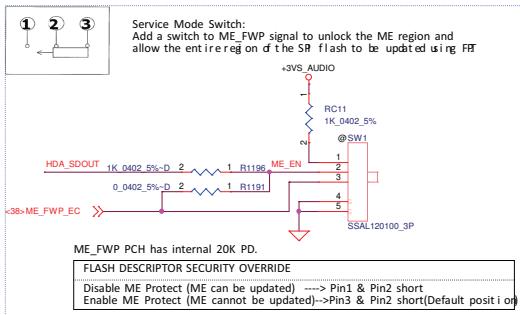
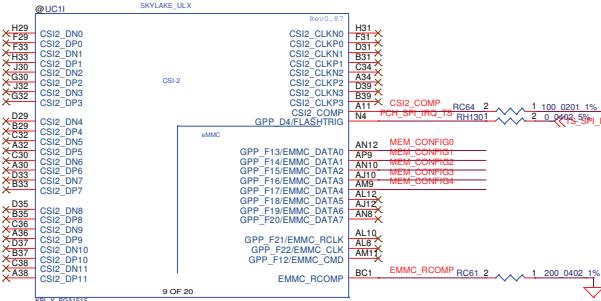
SKL YC/13) DDRIII
LA-D781P





Functional Strap Definitions

GPP_B14 (Internal Pull Down): SPKR
TOP Swap Override
0 = Disable TOP Swap mode--> AAU30 Use
1 = Enable TOP Swap Mode.



ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)

Pin Name	RH150	RH149	RH148	RH147	RH146	RH145	RH144	RH143	RH142	RH141	RH140	RH139	RH138	RH137	RH136	RH135	RH134	RH133
MEM_CONFIG0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MEM_CONFIG1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MEM_CONFIG2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MEM_CONFIG3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MEM_CONFIG4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

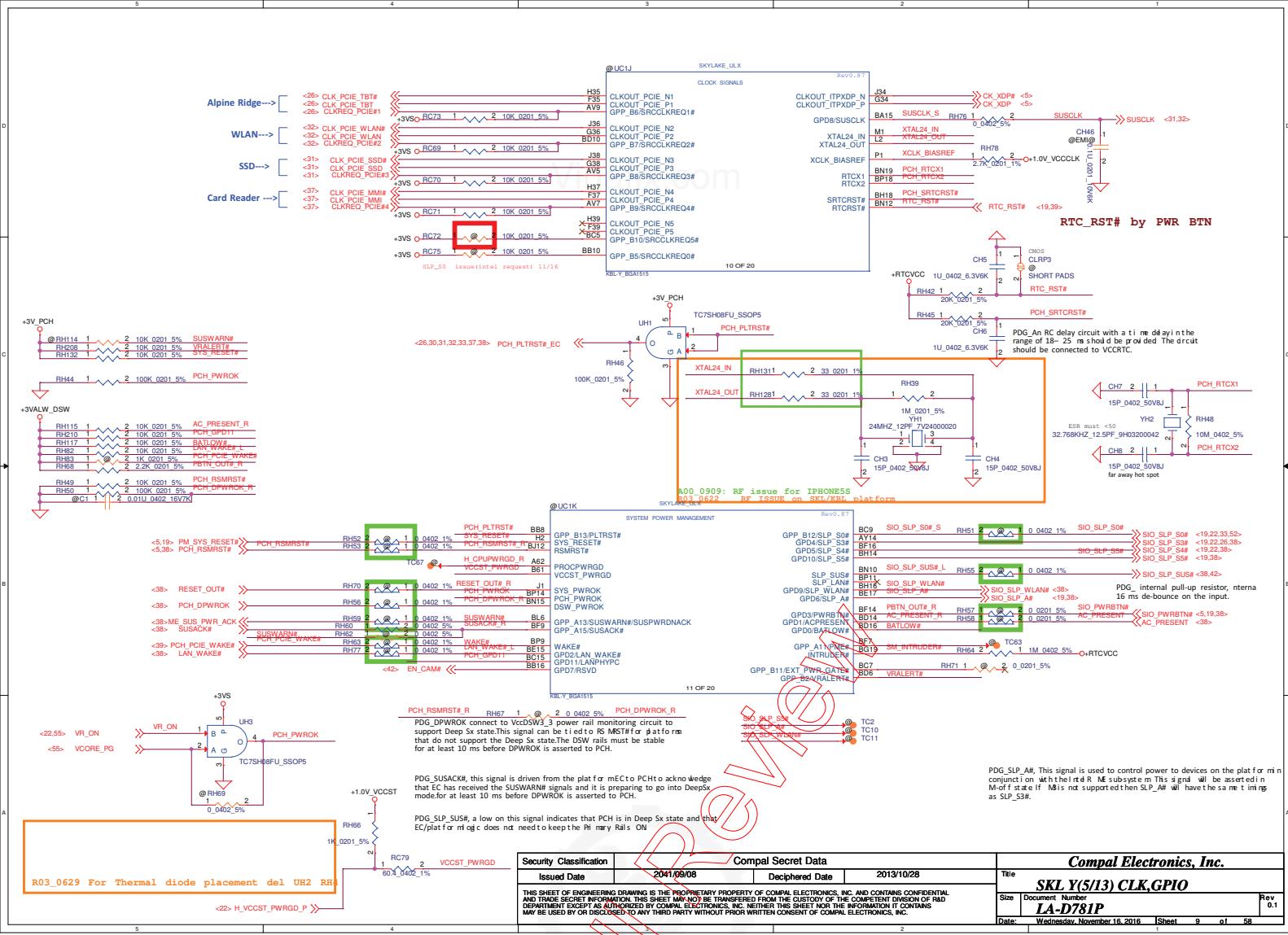
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SKL Y(4/13) HDA,EMMC,SDIO		
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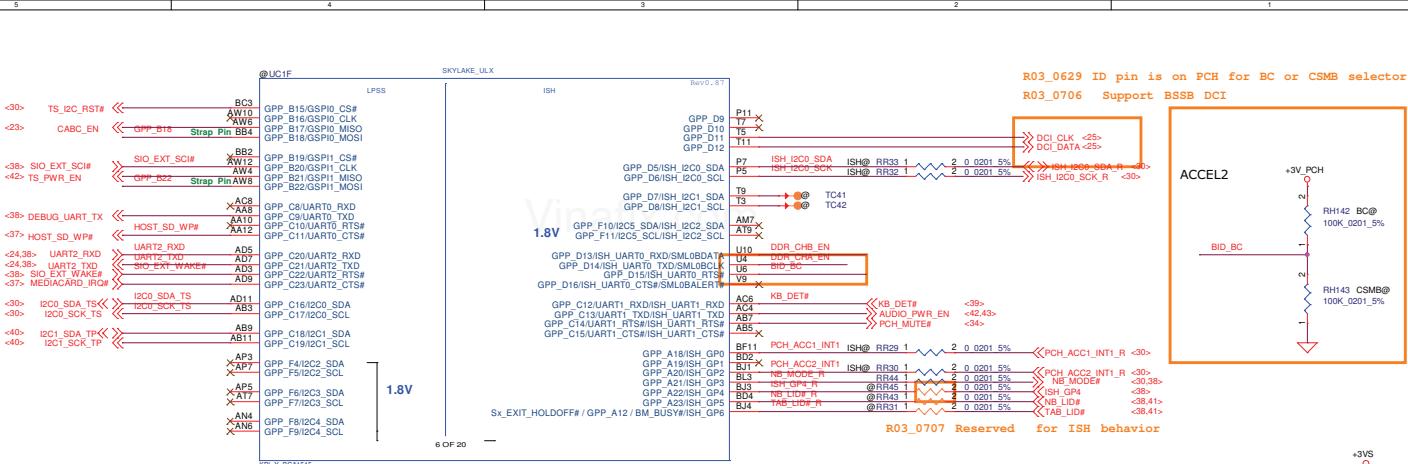
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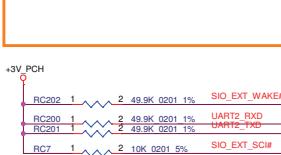
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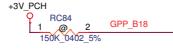


R03_0622 Del RC286,RC287 change power rail to +3V_TS



Functional Strap Definitions

GPP_B18 (Internal Pull Down): GSSPIO_MOSI
No Reboot
0 = Disable No Reboot mode. => AAU30 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

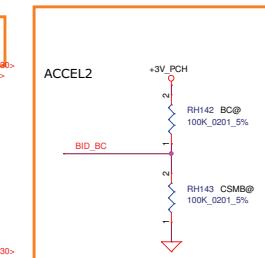


Functional Strap Definitions

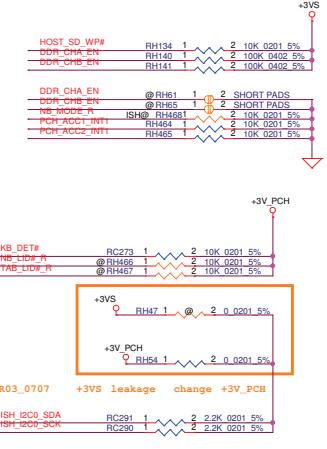
GPP_B22 (Internal Pull Down): GSSPI1_MOSI
Boot BIOS Strap Bit
0 = SPI Mode => AAU30 Use
1 = LPC Mode



R03_0629 ID pin is on PCH for BC or CSMB selector
R03_0706 Support BSSB DCI



R03_0707 Reserved for ISH behavior



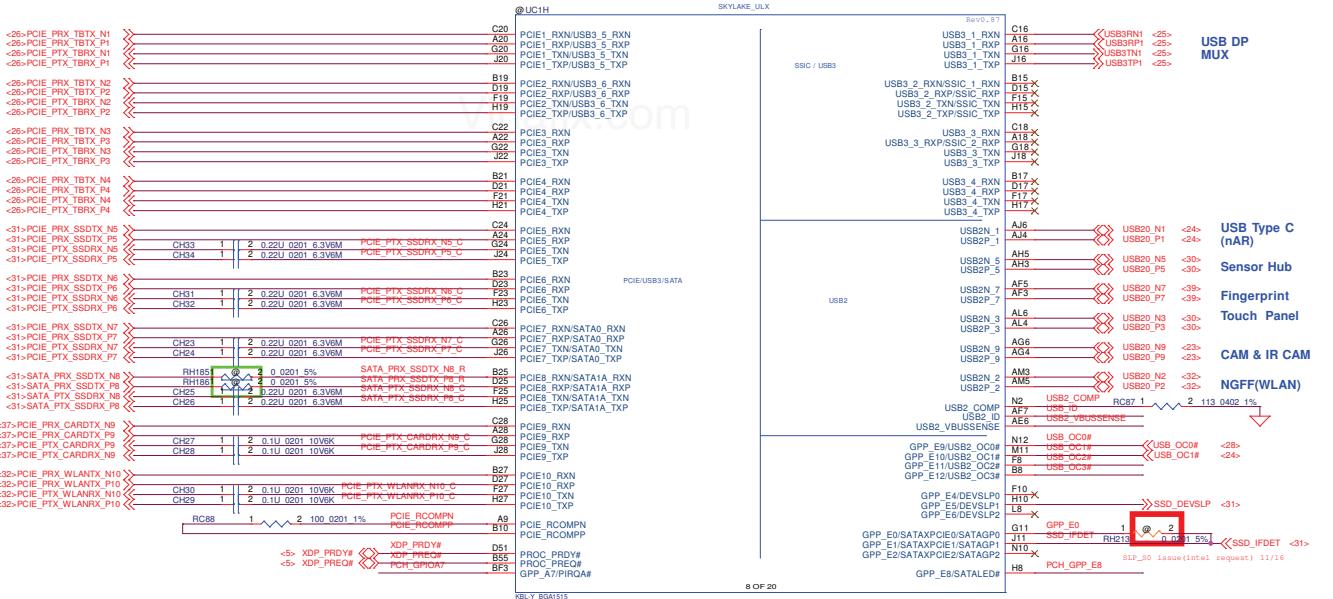
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SKLY(6/13) GPIO,LPIO,I2C

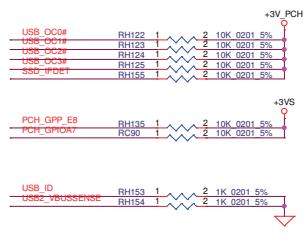
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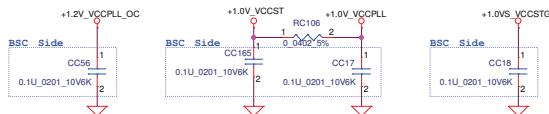
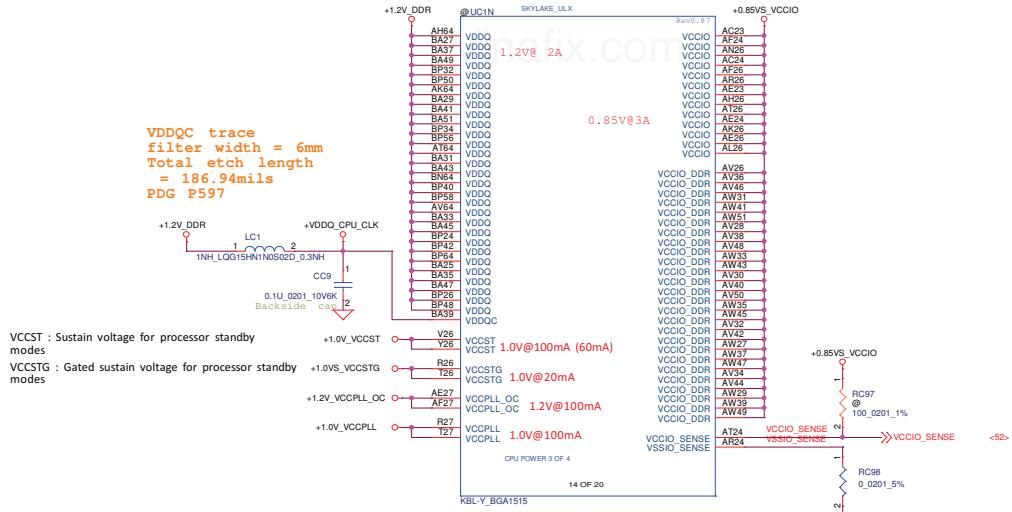


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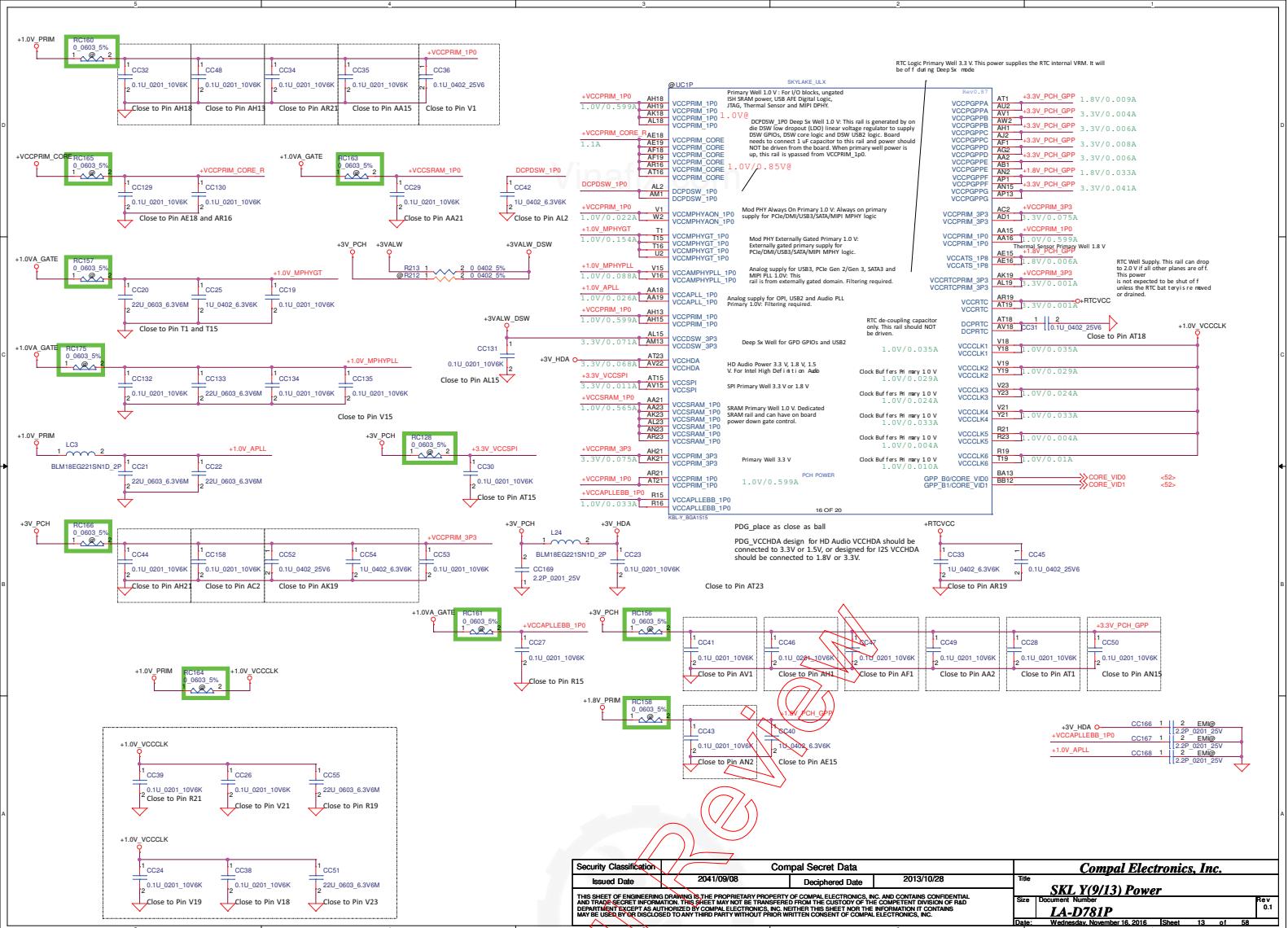


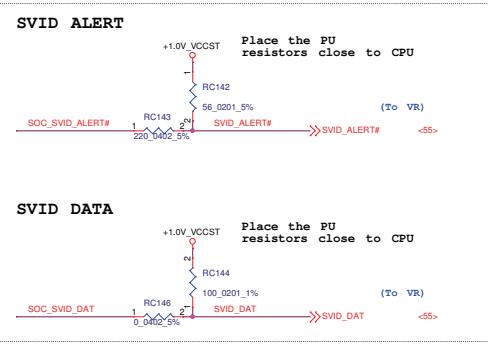
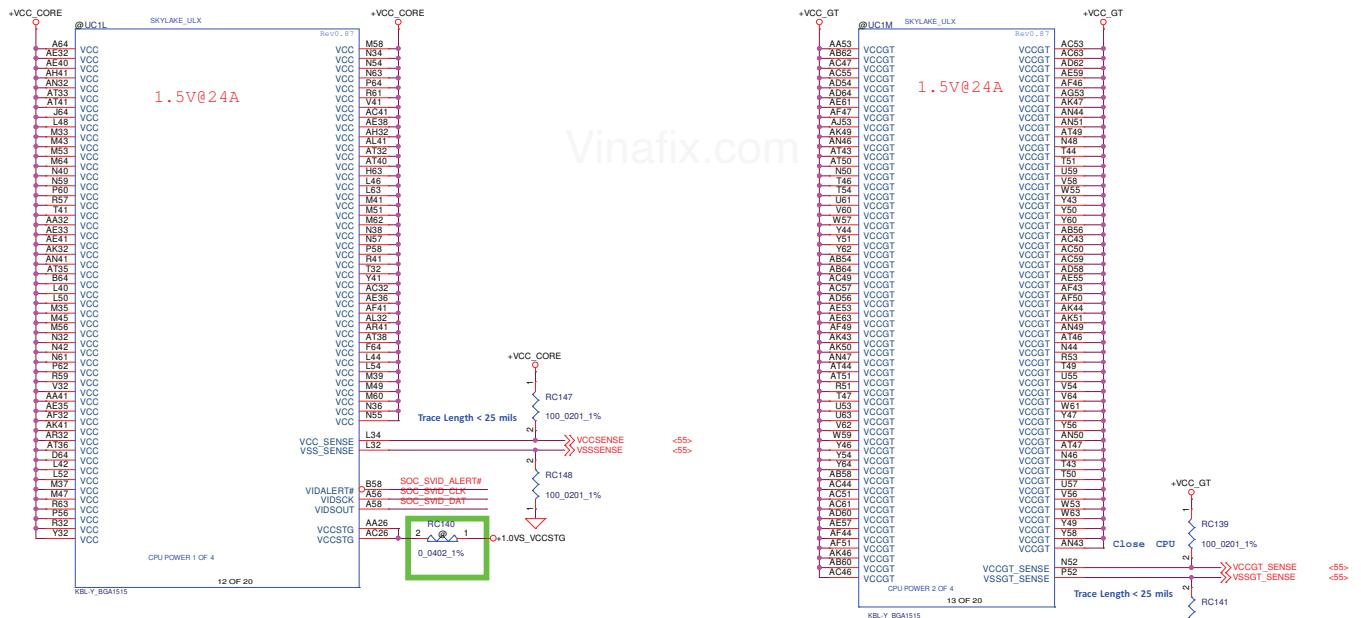
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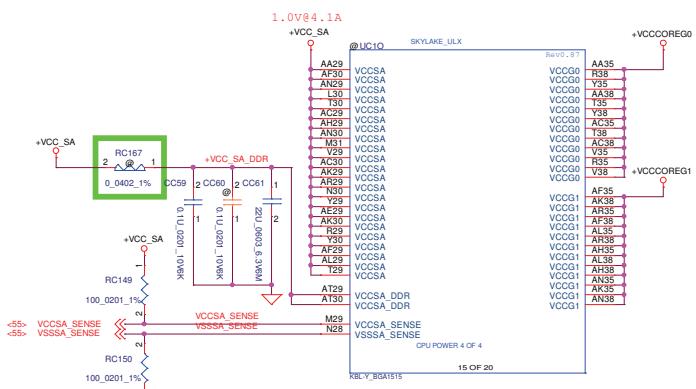
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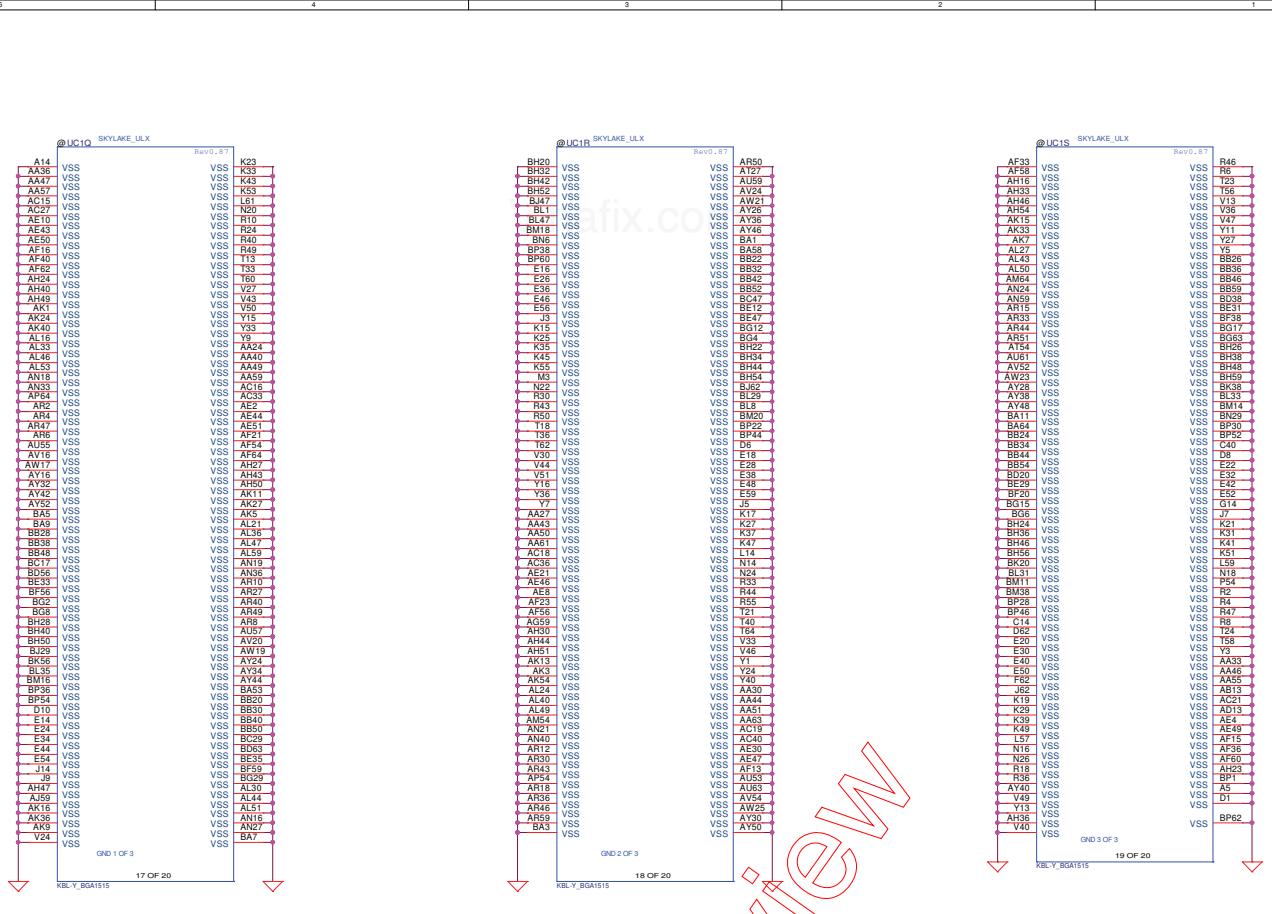
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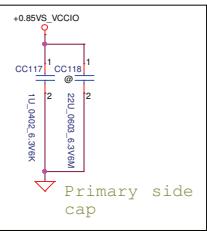
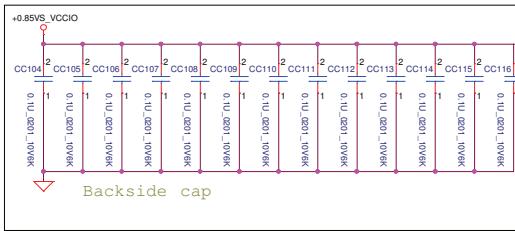
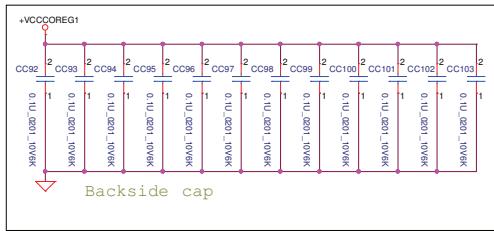
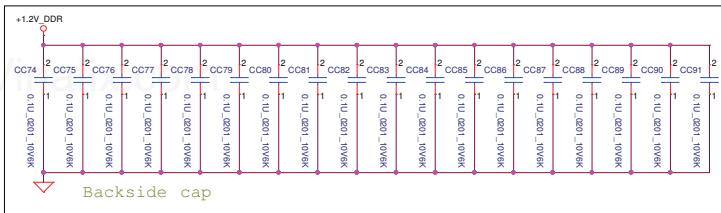
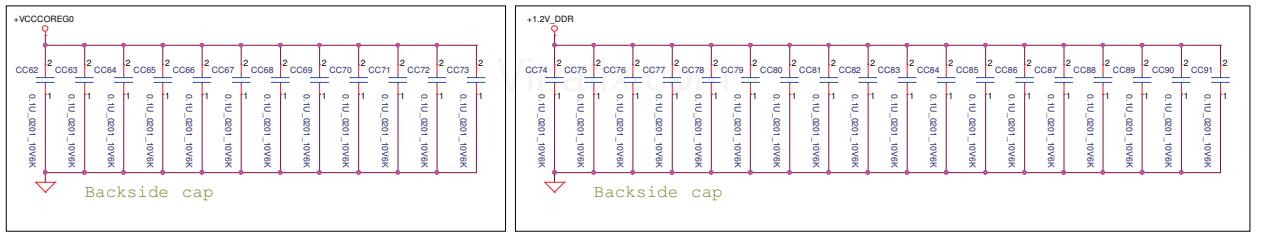


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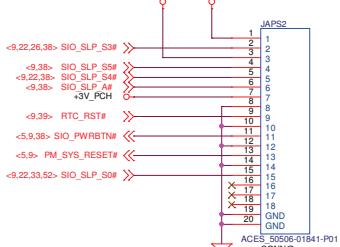
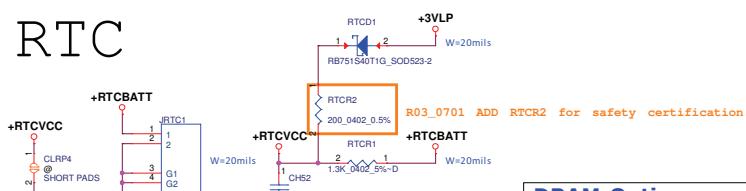
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RTC

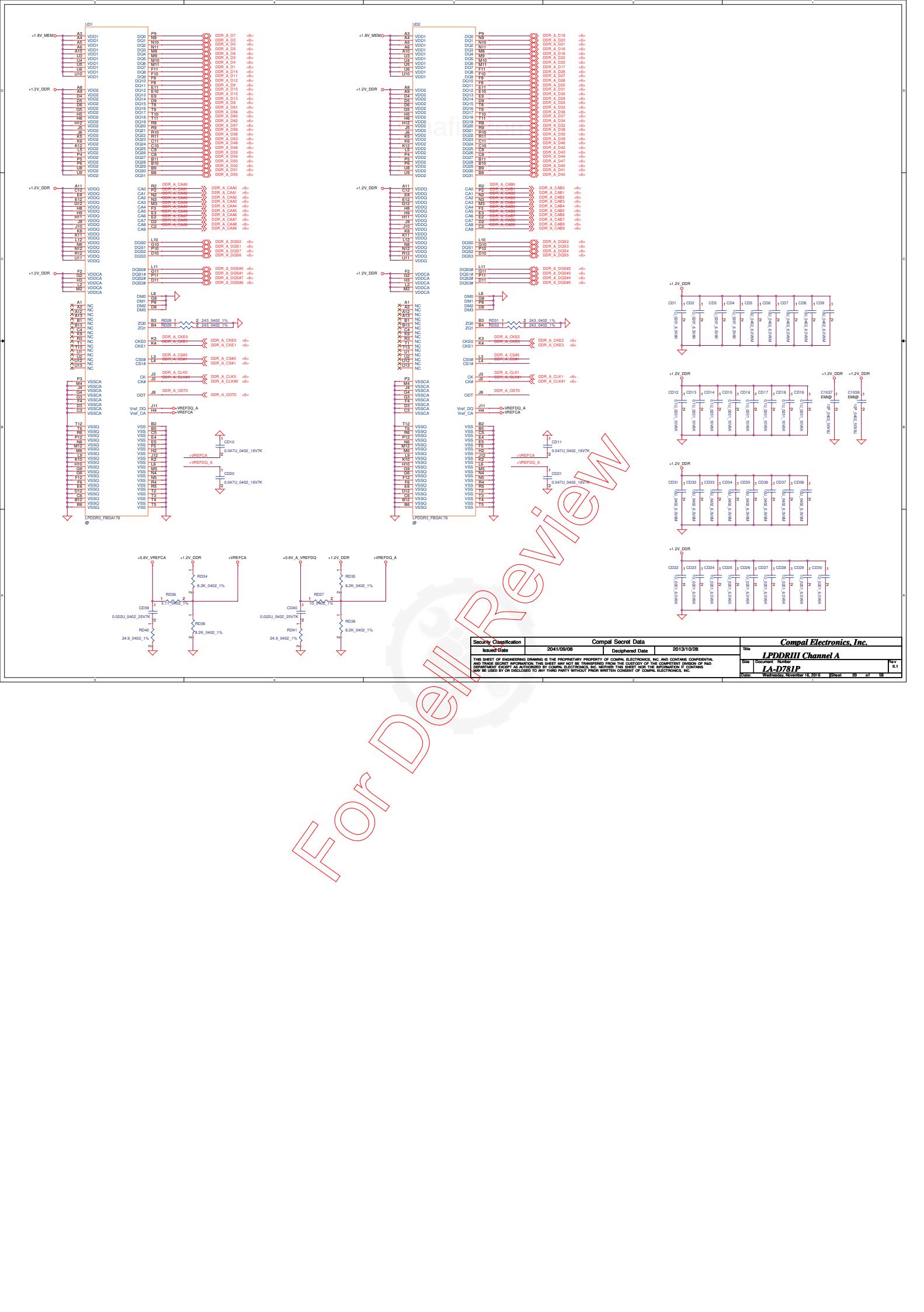
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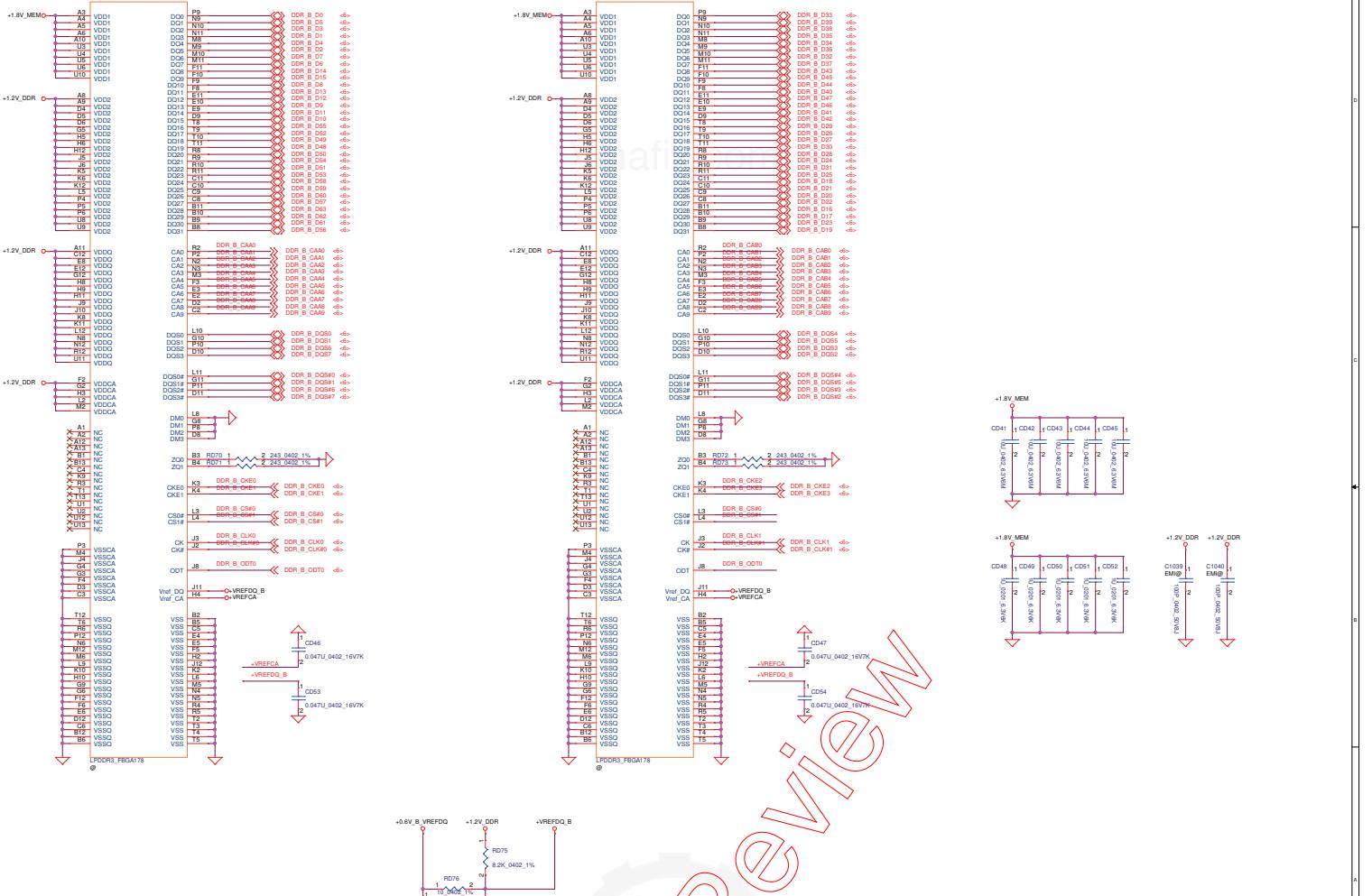
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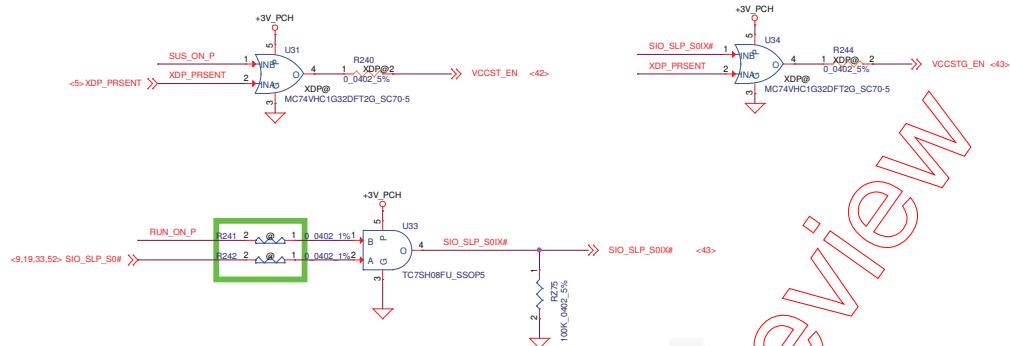
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Micron 8G/1866	X76_M8G@ UD1 MTS2L512M2D2DPF-107WT MTS2L512M2D2DPF-107WT MTS2L512M2D2DPF-107WT MTS2L512M2D2DPF-107WT SA00009JU0L SA00009JU0L SA00009JU0L SA00009JU0L	X76_M8G@ UD2 SA00009JU0L	X76_M8G@ UD3 SA00009JU0L	X76_M8G@ RH139 10K 0402 5% SD028100280	X76_M8G@ RH145 10K 0402 5% SD028100280	X76_M8G@ RH126 10K 0402 5% SD028100280	X76_M8G@ RH212 10K 0402 5% SD028100280	X7666031L06
Micron 16G/1866	X76_M16G@ UD1 SA00009XV0L	X76_M16G@ UD2 SA00009XV0L	X76_M16G@ UD3 SA00009XV0L	X76_M16G@ RH139 10K 0402 5% SD028100280	X76_M16G@ RH145 10K 0402 5% SD028100280	X76_M16G@ RH126 10K 0402 5% SD028100280	X76_M16G@ RH212 10K 0402 5% SD028100280	X7666031L09
Hynix 4G/1866	X76_H4G@ UD1 H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD SA00009G00L SA00009G00L SA00009G00L SA00009G00L	X76_H4G@ UD2 H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD SA00009U70L SA00009U70L SA00009U70L SA00009U70L	X76_H4G@ UD3 H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD H9CCNNN8GTMLAR-NUD SA00009U70L SA00009U70L SA00009U70L SA00009U70L	X76_H4G@ RH139 10K 0402 5% SD028100280	X76_H4G@ RH145 10K 0402 5% SD028100280	X76_H4G@ RH126 10K 0402 5% SD028100280	X76_H4G@ RH212 10K 0402 5% SD028100280	X7666031L01
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Samsung 16G/1866	X76_S16G@ UD1 KA4E8334EB-EGCF SA00009X11L	X76_S16G@ UD2 KA4E8334EB-EGCF SA00009X11L	X76_S16G@ UD3 KA4E8334EB-EGCF SA00009X11L	X76_S16G@ RH139 10K 0402 5% SD028100280	X76_S16G@ RH145 10K 0402 5% SD028100280	X76_S16G@ RH126 10K 0402 5% SD028100280	X76_S16G@ RH212 10K 0402 5% SD028100280	X7666031L08

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Size	Document Number	LA-D781P		
Date:	Wednesday, November 16, 2016	Sheet	19	of 58

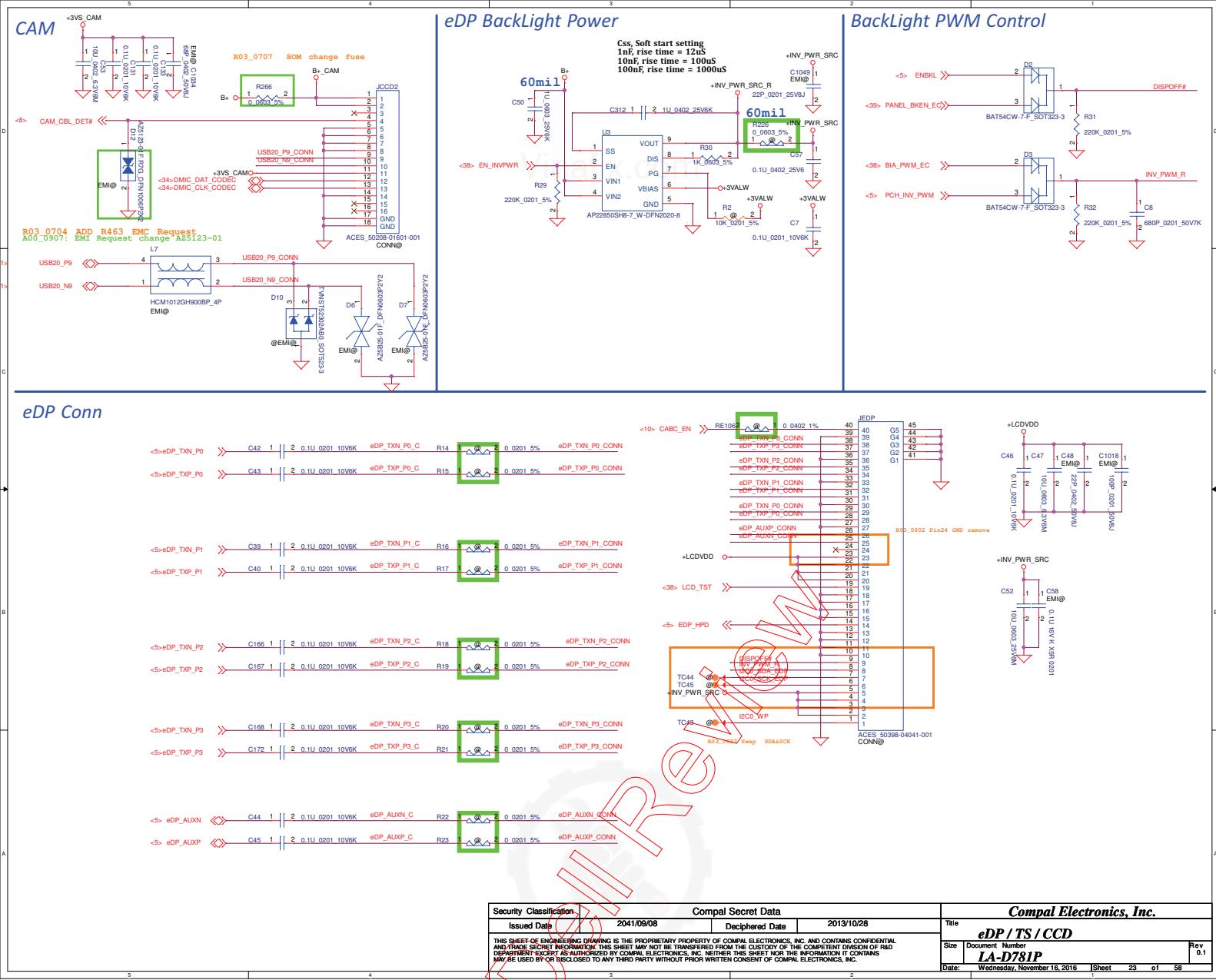


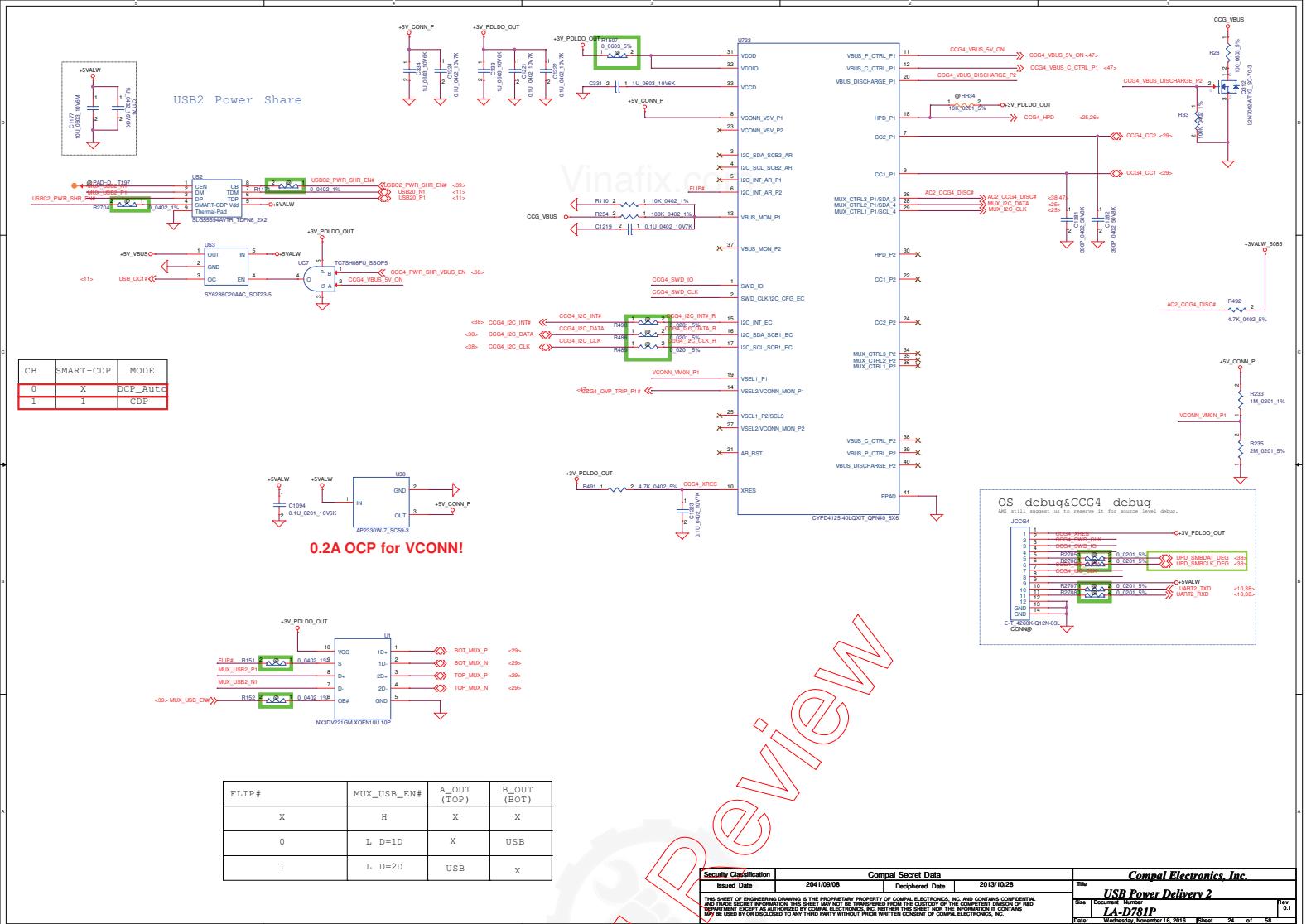


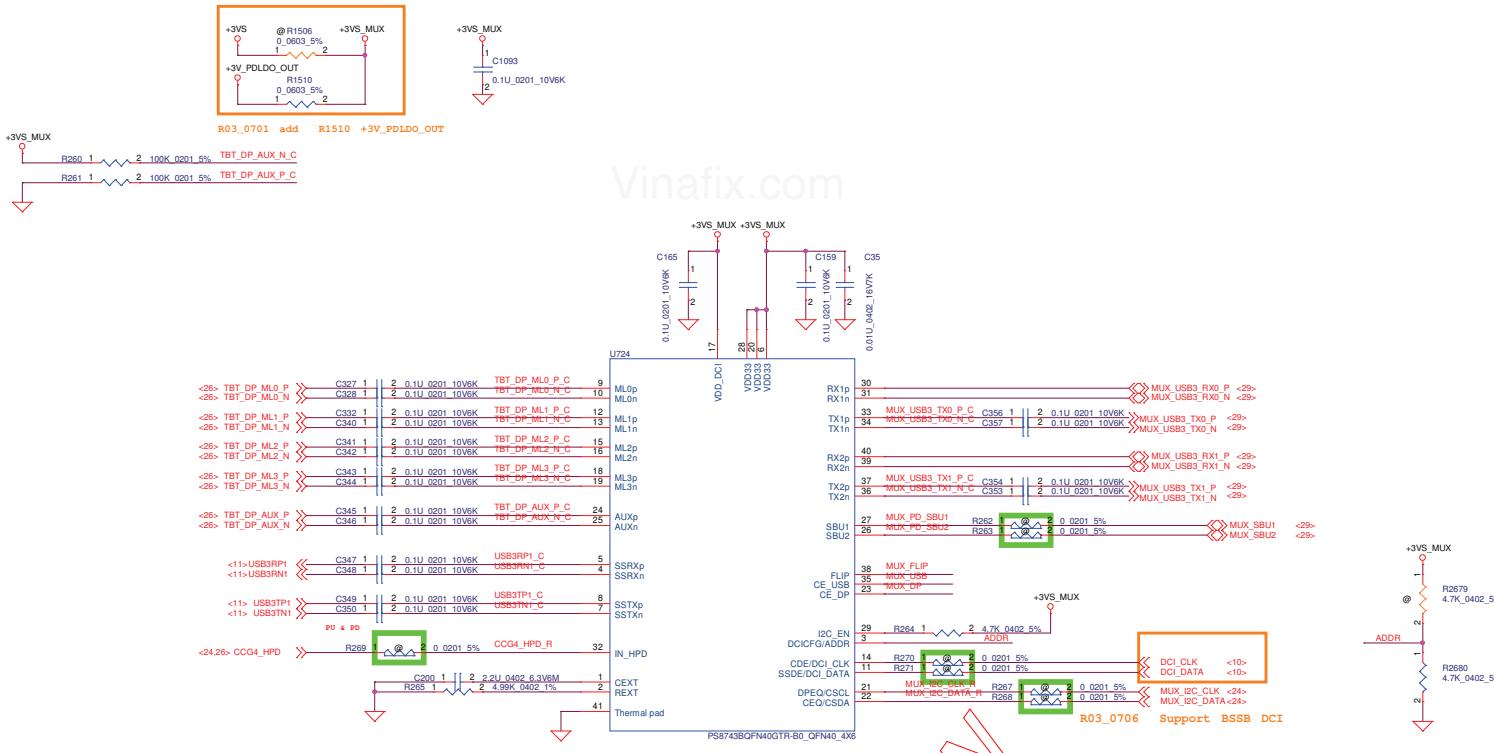
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	LA-D781P			
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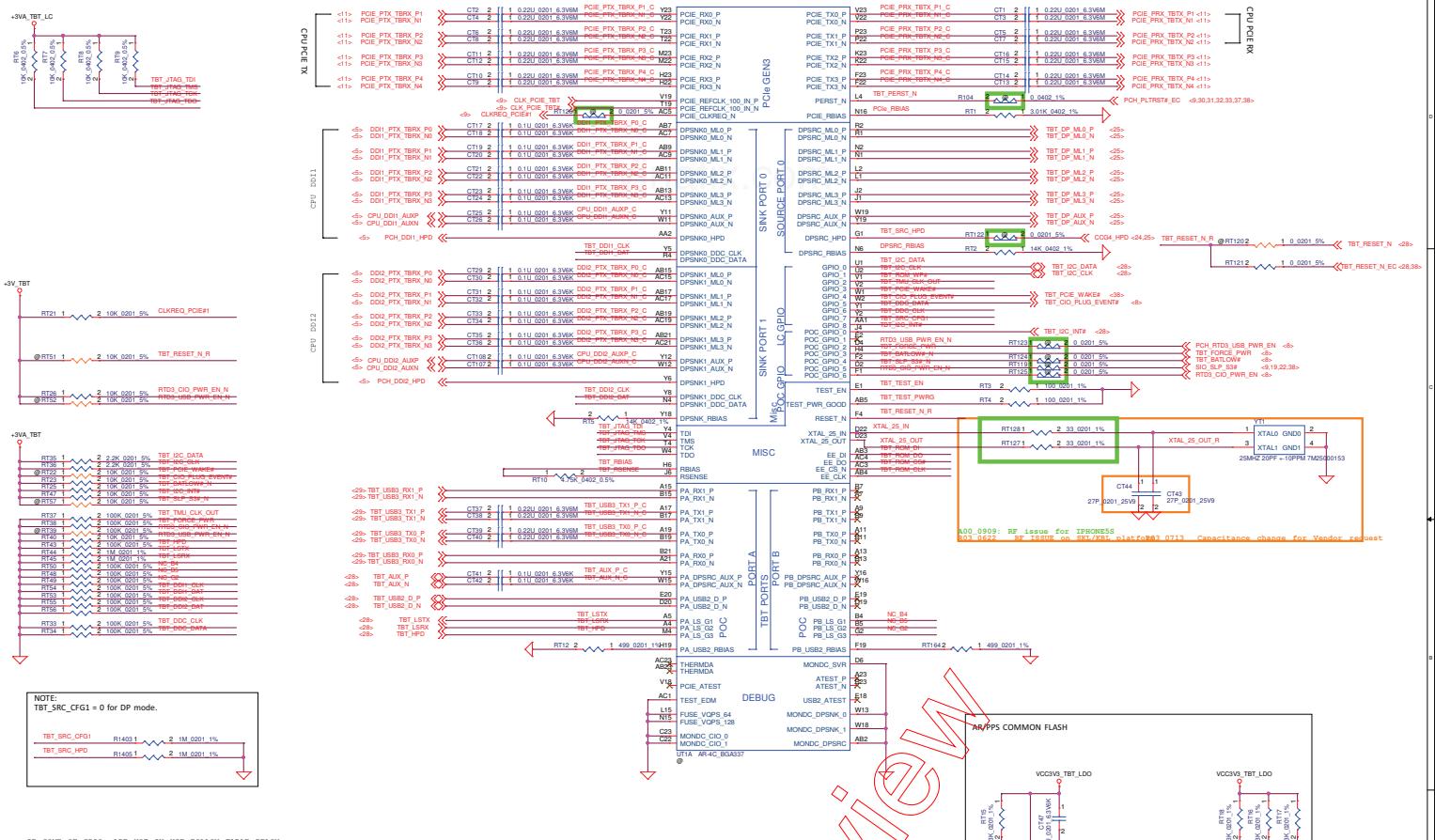


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			Size	Document Number	Rev.
			LA-D781P		0.1
			Date:	Wednesday, November 16, 2016	Sheet 25 of 58

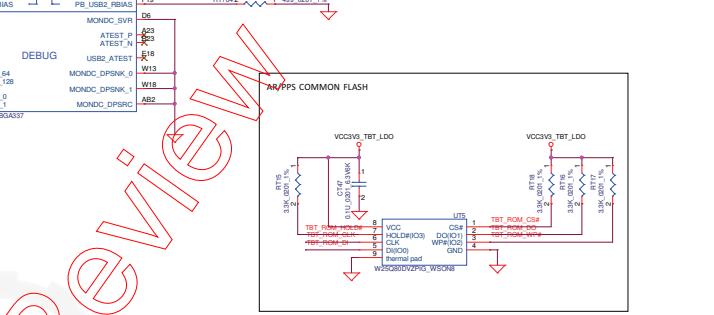


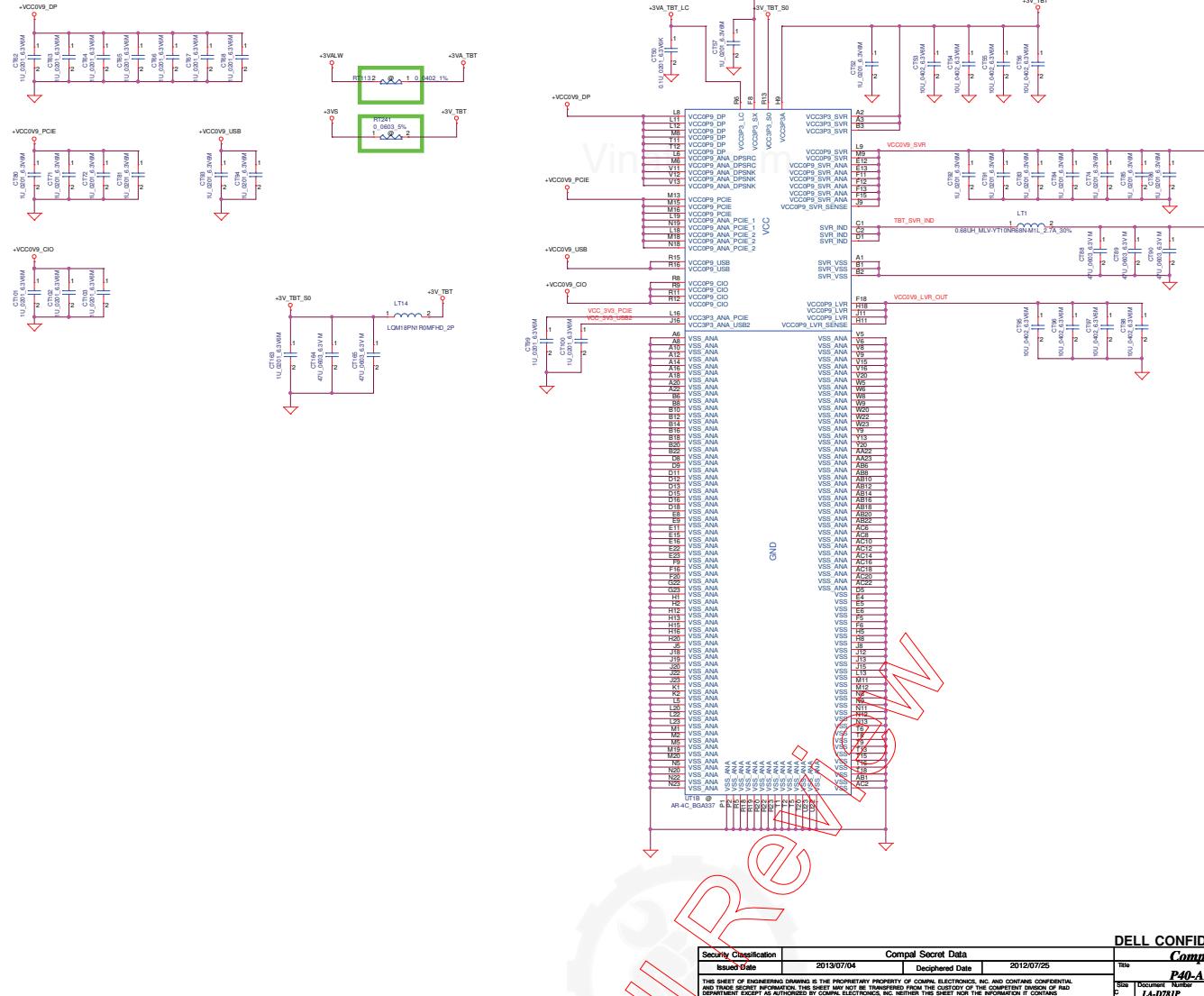
IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:
| GPIO | TERMINATION | Power Rail

GPIO	TERMINATION	Power Rail	DEBUG PINS:
GP1_0	10K PU	VCC3V3_LC	
GP1_1	10K PU	VCC3V3_LC	
GP1_2	10K PD		PIN _____ TERMINATION
GP1_3	100K PD		MONDC_SVR
GP1_4	10K PU	VCC3V3_LC	MONDC_DPSNK_0 GND
GP1_5	10K PU	VCC3V3_LC	MONDC_DPSNK_1 GND
GP1_6	100K PD		MONDC_GND
GP1_7	100K PD		MONDC_CIO_0 GND
GP1_8	100K PD		TEST_P
POC_GPT1_0	10K PU	VCC3V3_SK_TBT	TEST_N
POC_GPT1_1	10K PU	FUSE_VQPS_64	FUSE_VQPS_128
POC_GPT1_2	100K PD		TEST_JTAG
POC_GPT1_3	100K PD		ATEST_F/N
POC_GPT1_4	10K PU	VCC3V3_SK_TBT	FLOATING
POC_GPT1_5	10K PU	VCC3V3_SK_TBT	USB2_ATTEST
POC_GPT1_6	100K PD		PGIR_ATTEST

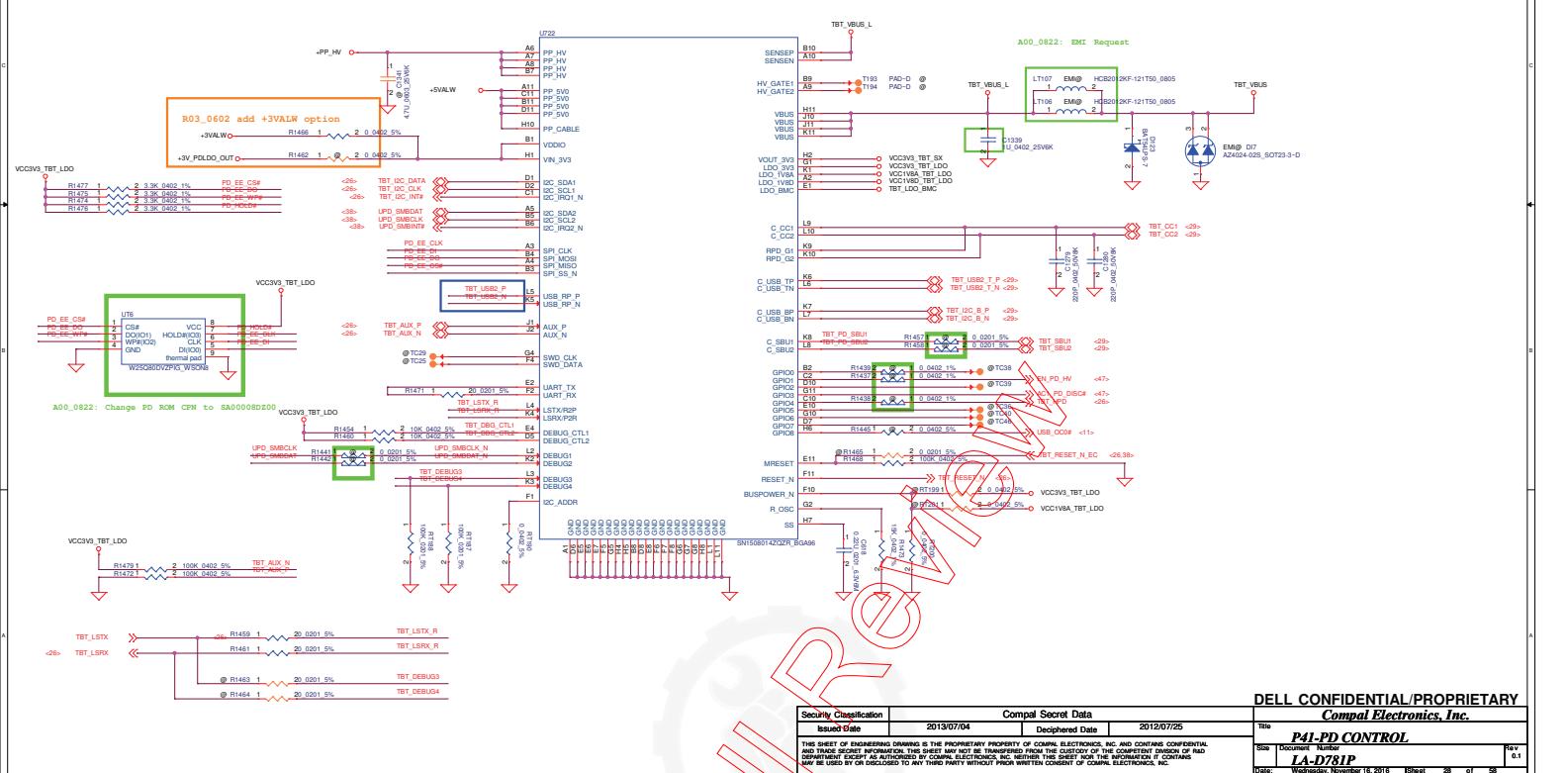
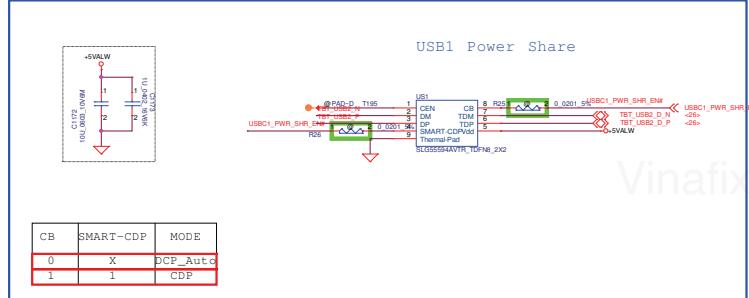
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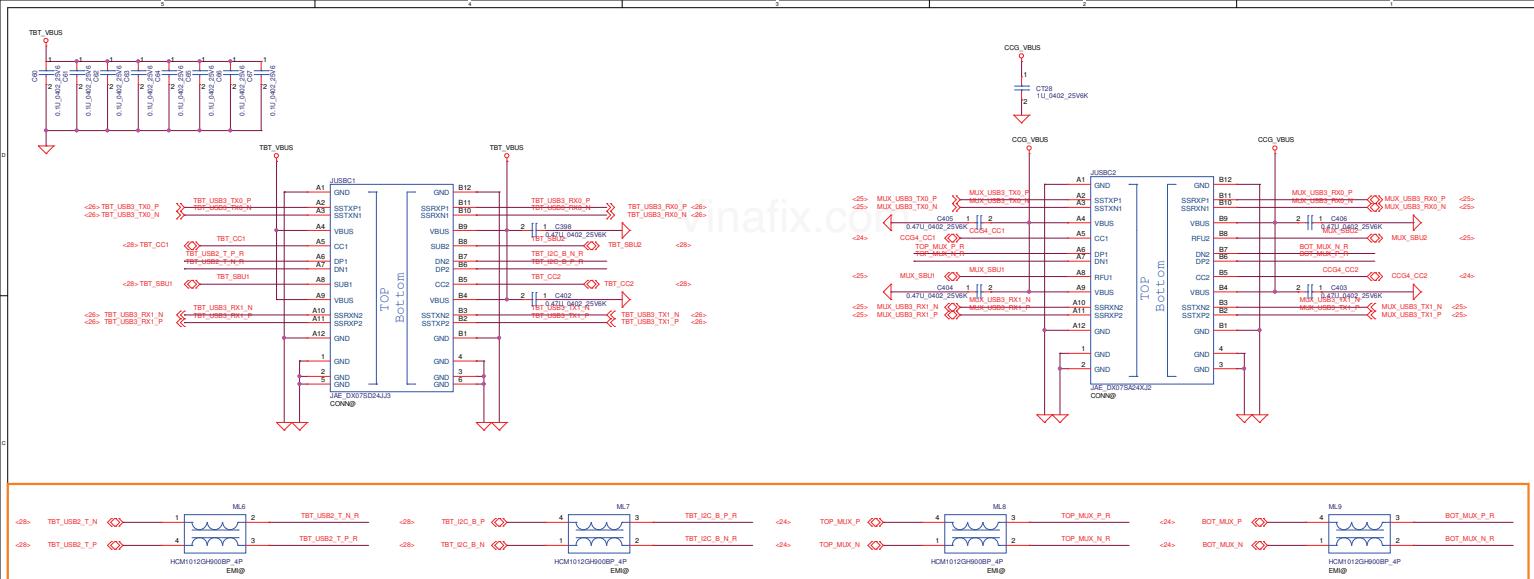
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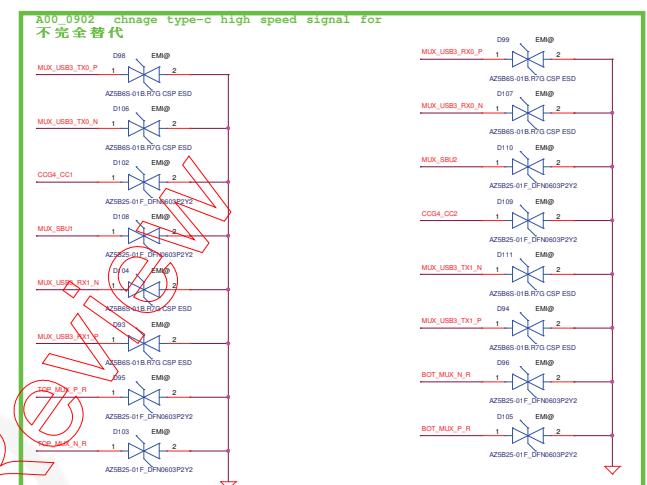
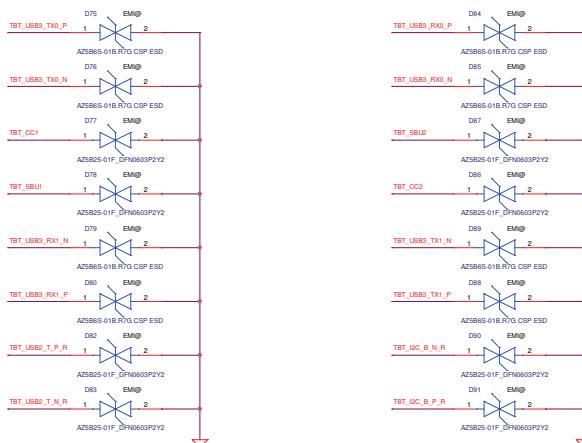


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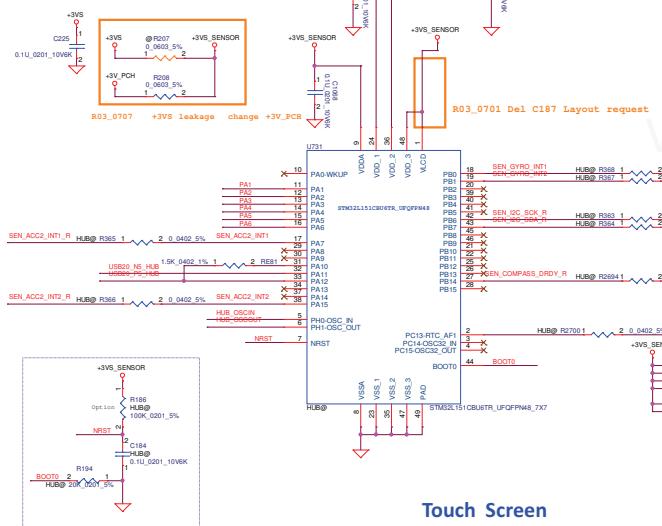


R03_0622 remove co-lay R03_0627 Pin3/Pin2 swap; Pin4/Pin1 swap

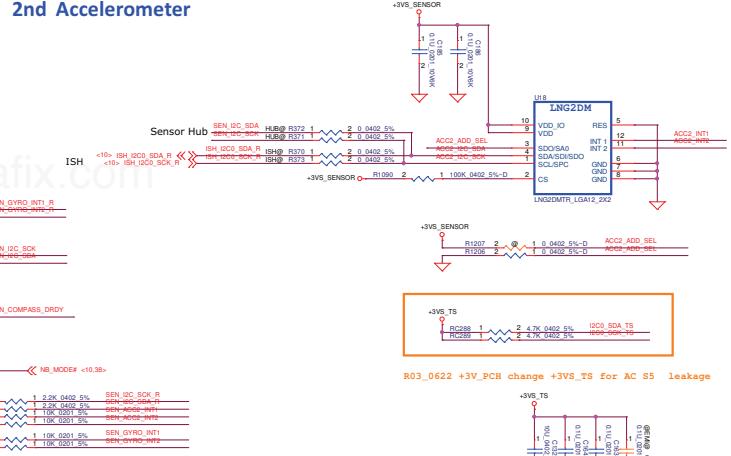


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Date	Wednesday, November 16, 2016

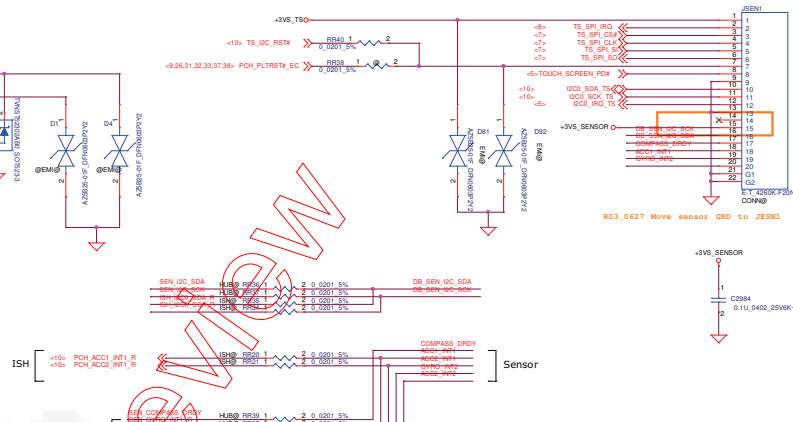
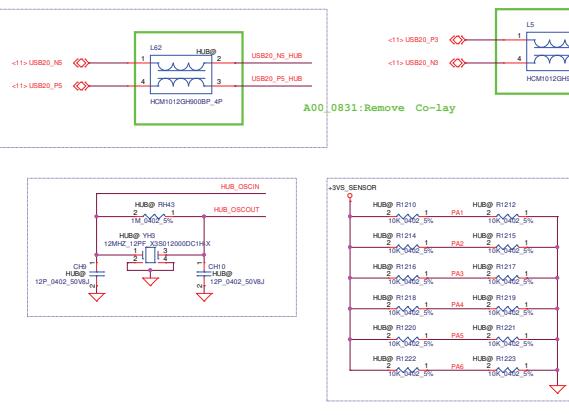
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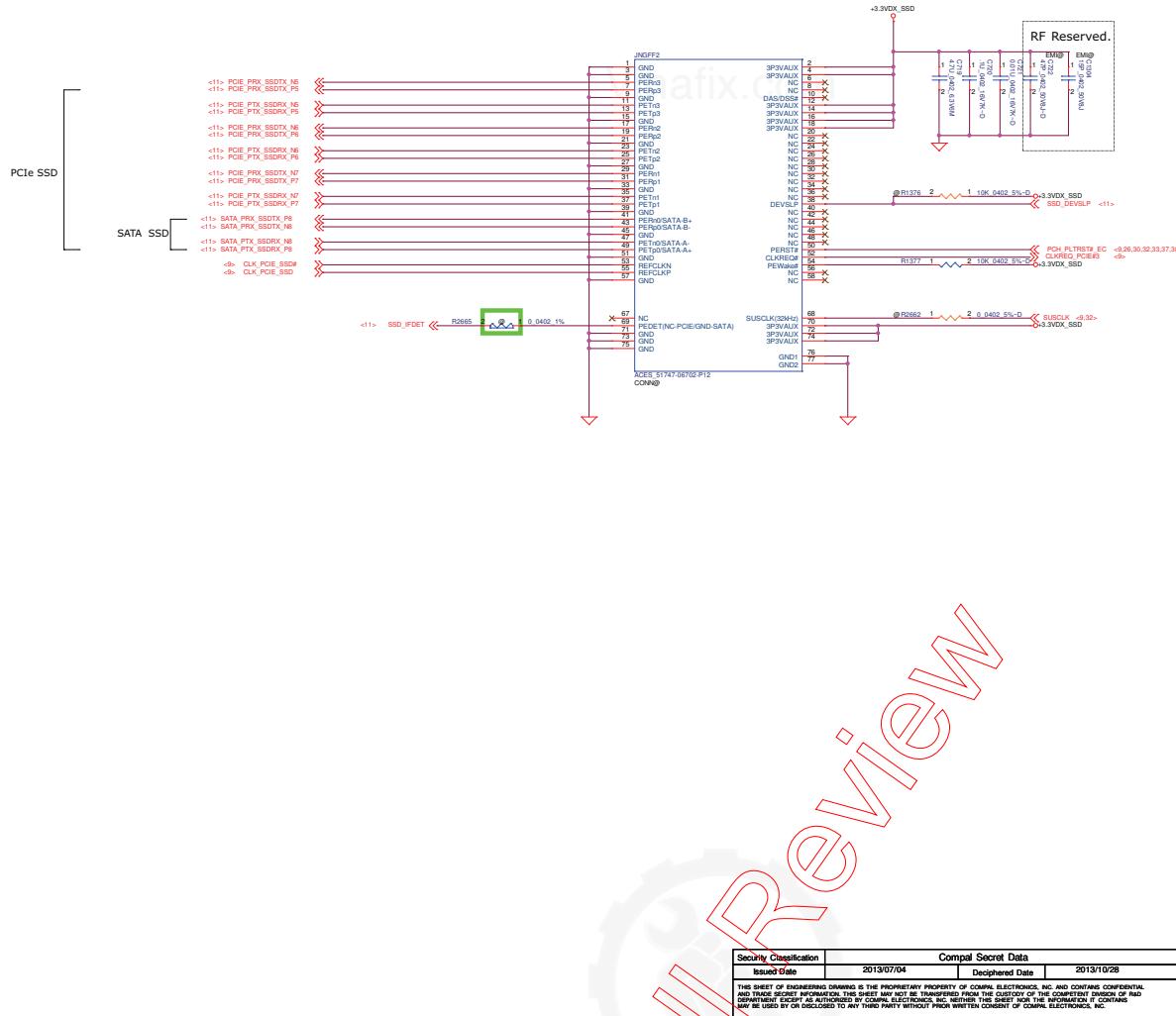
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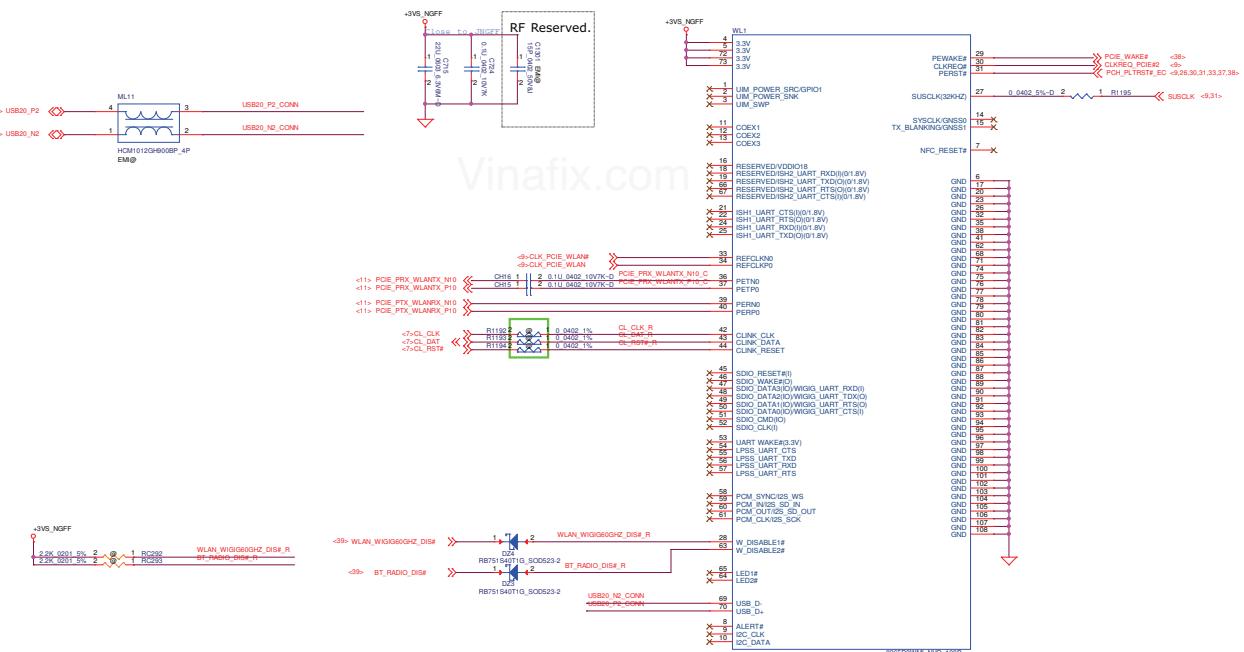
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Date: Wednesday, November 16, 2016			

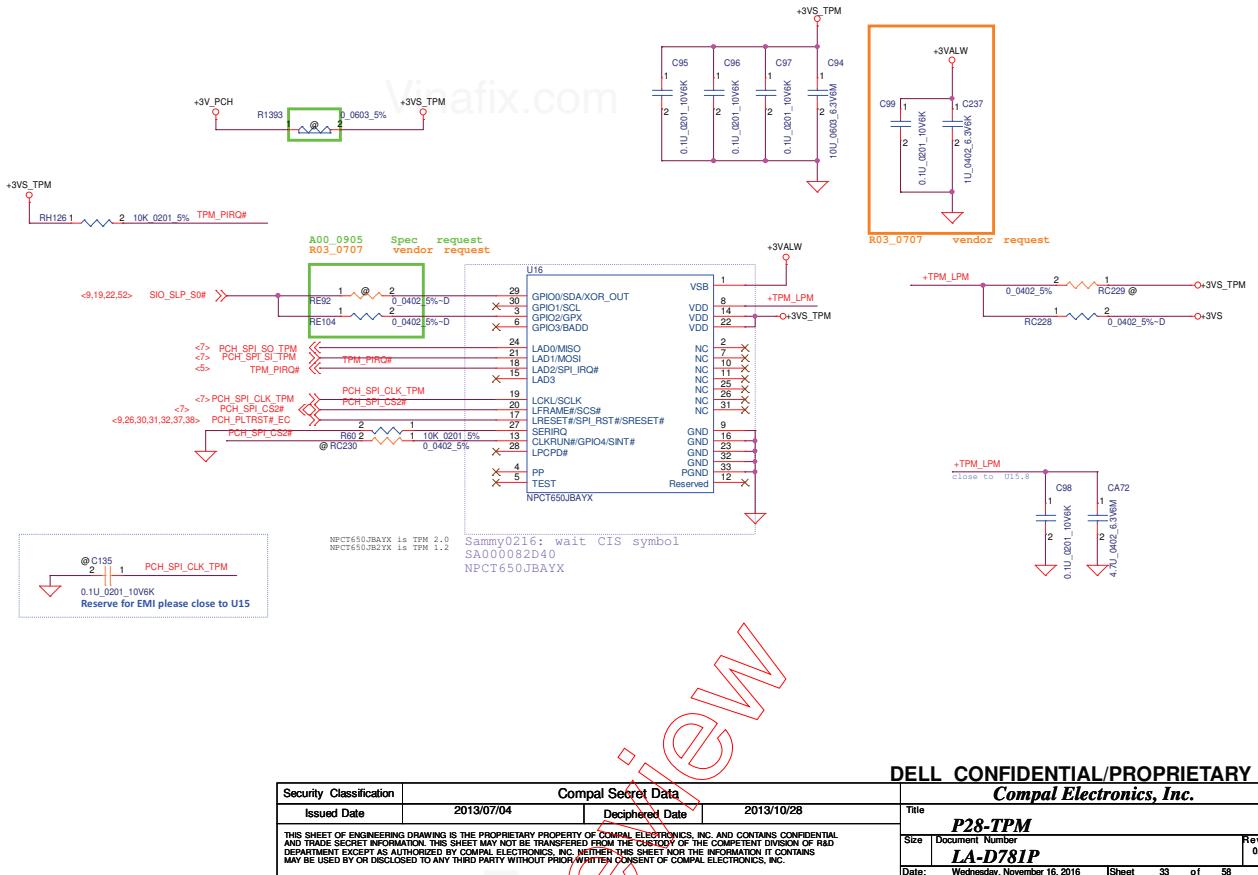


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Size	Document Name
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32	ct
58	sb

For Dell Review

TPM

NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins



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NPCT650JBAYX is TPM 1.2

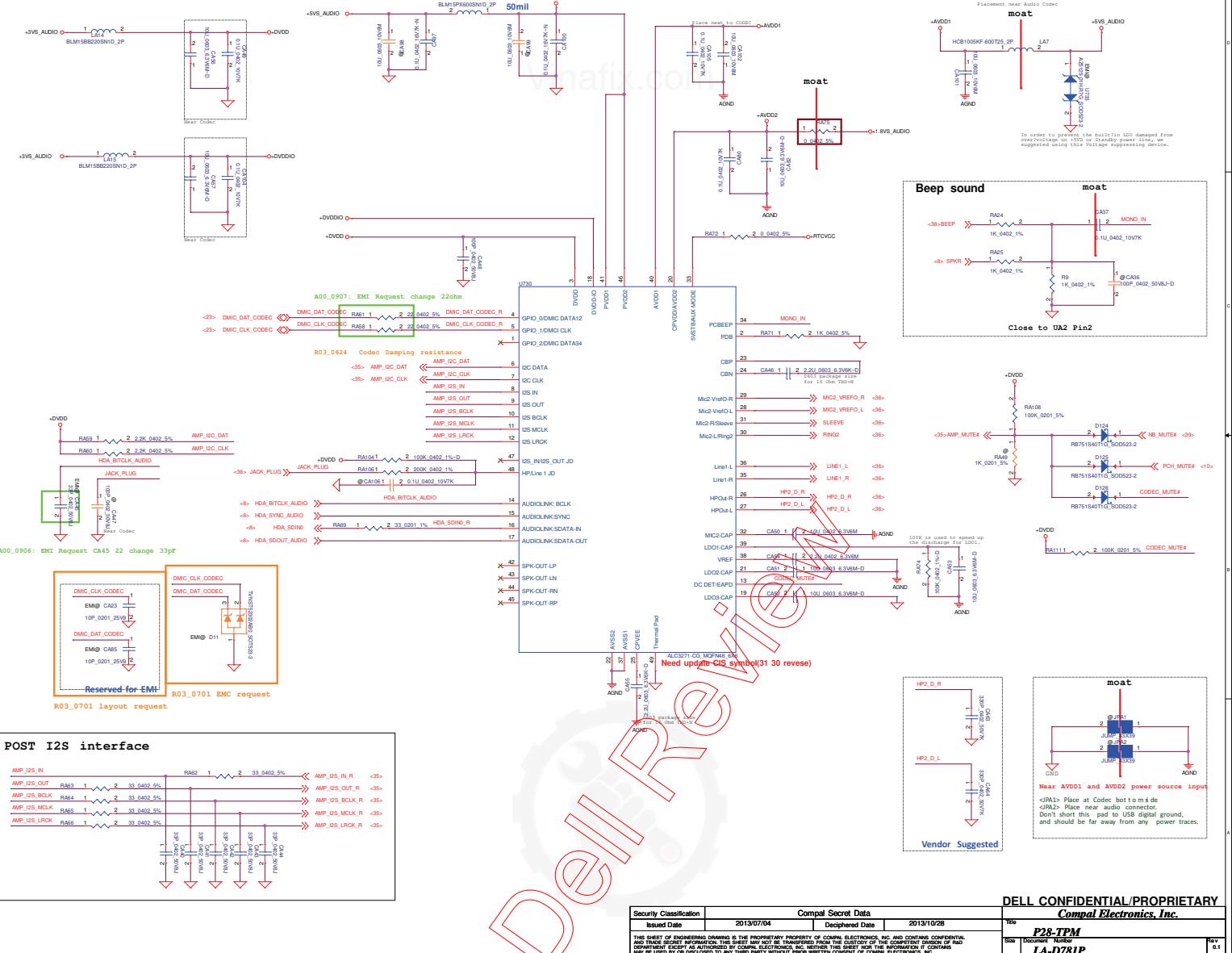
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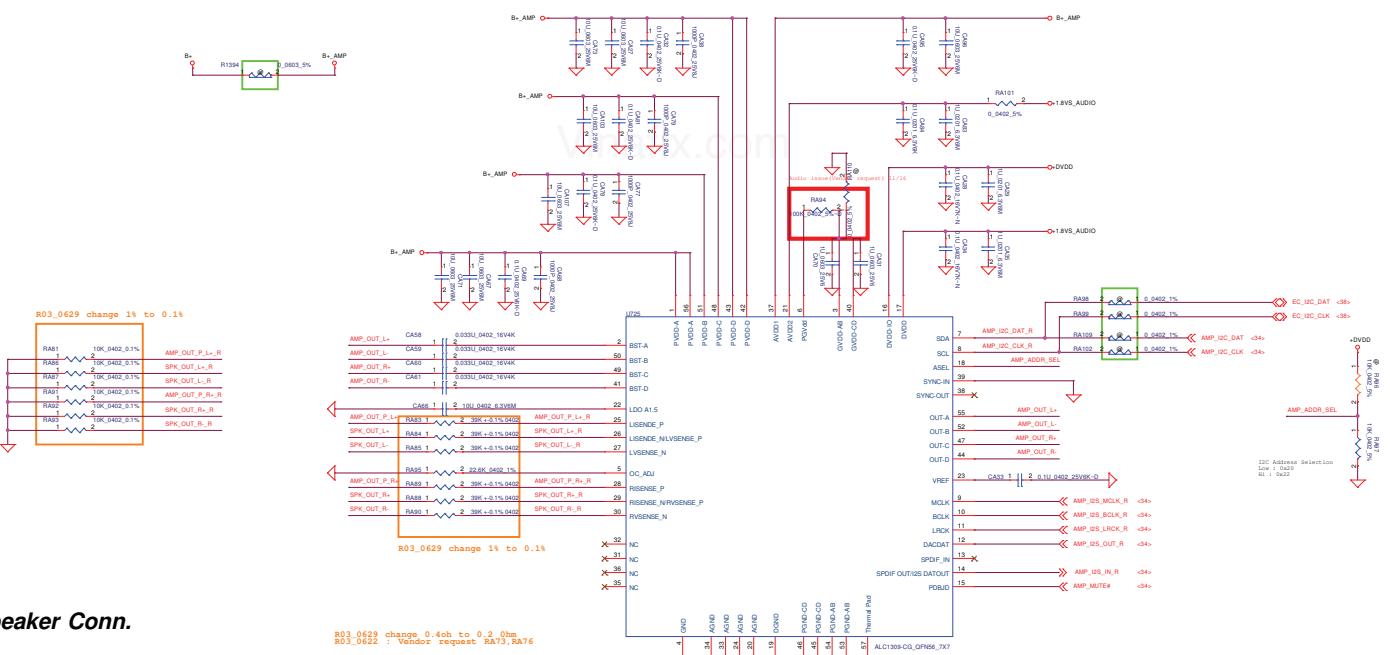
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HD Audio Codec

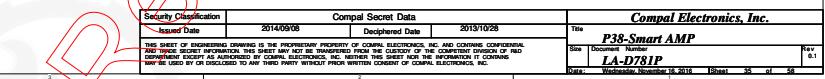
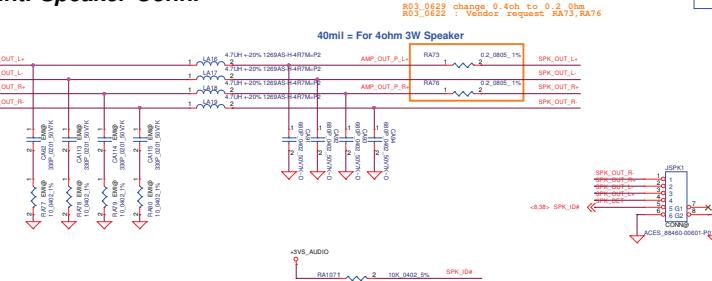


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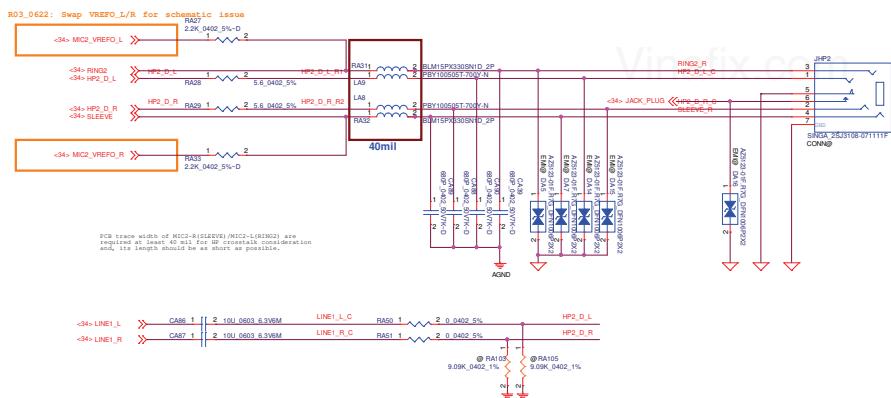
SMART AMP



Int. Speaker Conn.



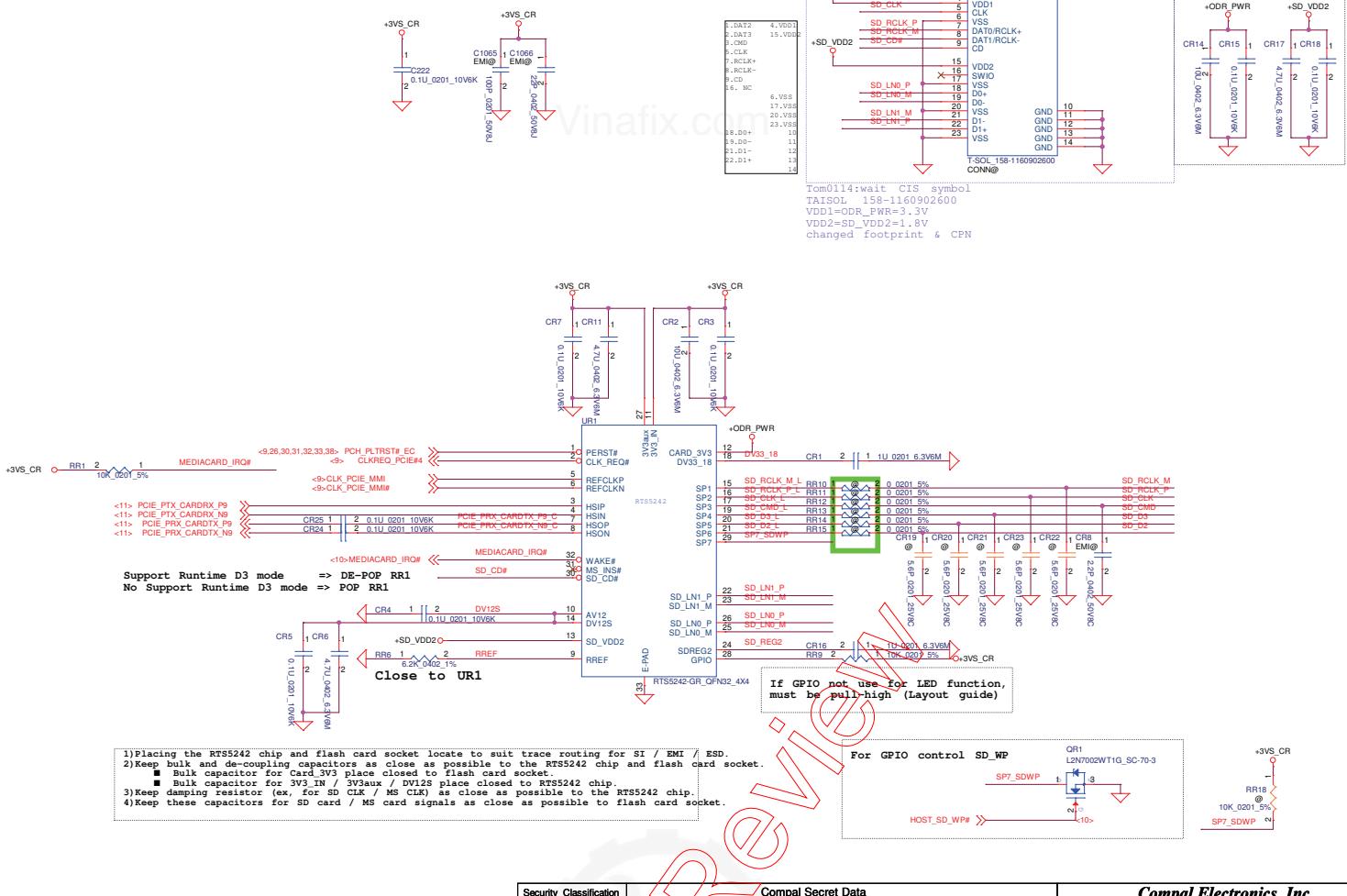
Universal Audio Jack



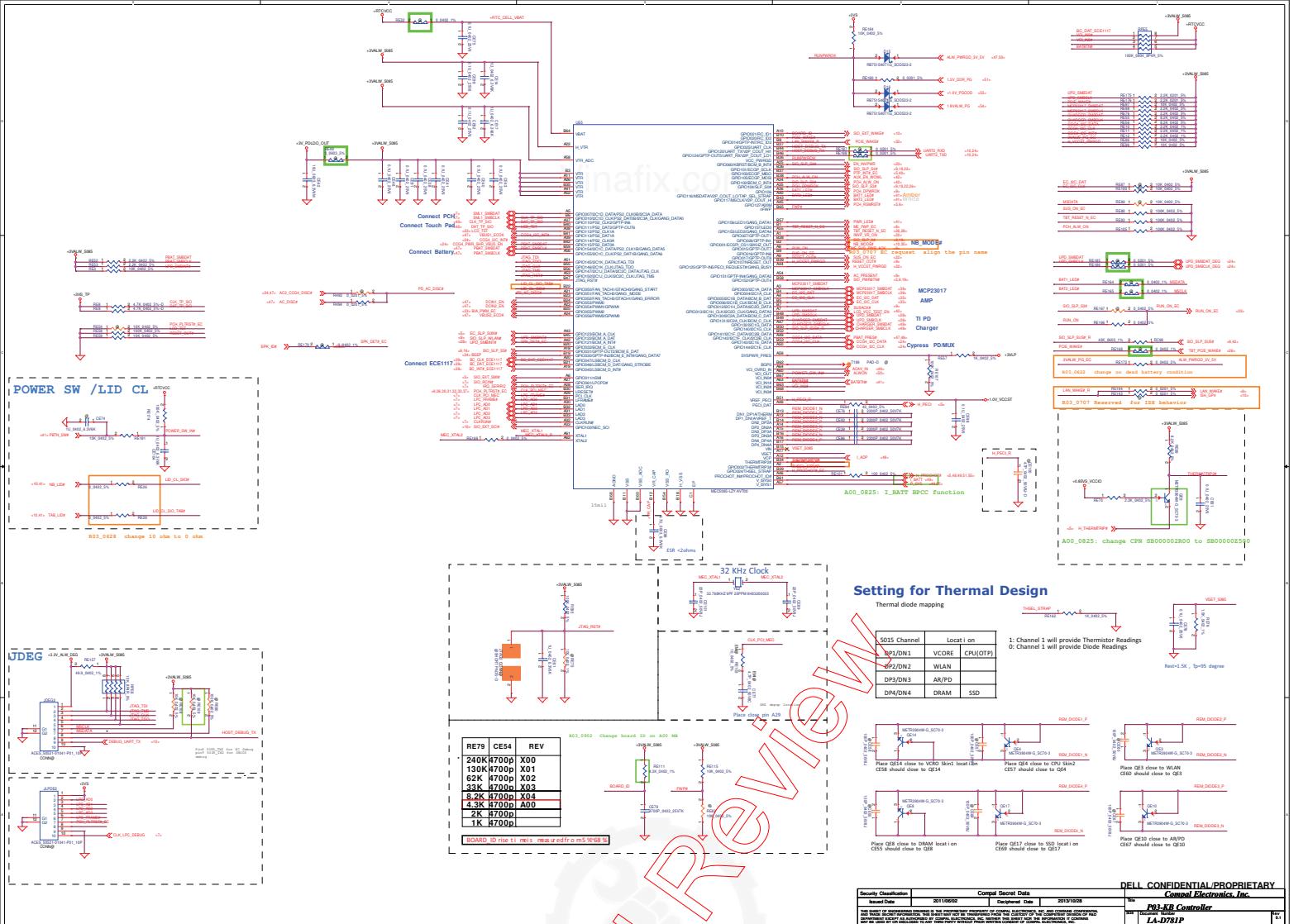
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	LA-D78IP			
Date:	Wednesday, November 8, 2017	Start	36	ct 58

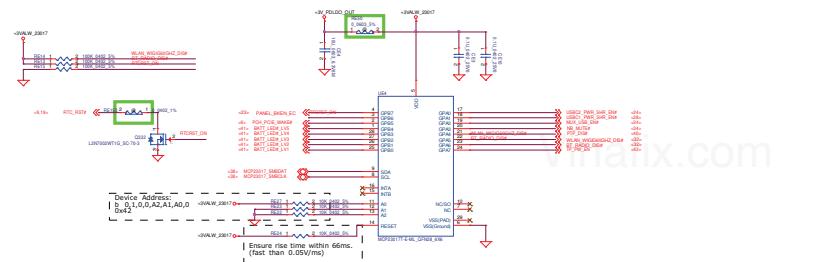
FOR DRAFT REVIEW

Card Reader

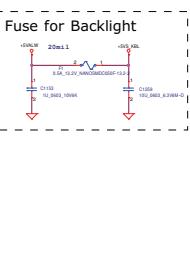
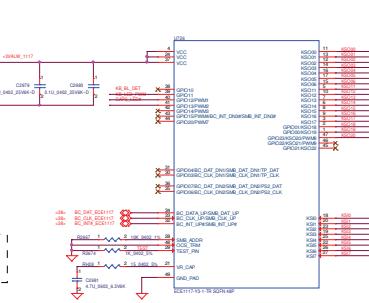


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				Rev 0.1	Date: Wednesday, November 16, 2016

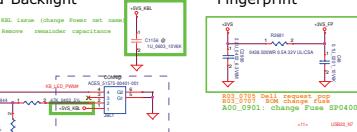




Connector Pin	Keyboard Signal	Pin Name
1	GND	
2	NC	
3	NC	
4	CapLock LED	GPIO3
5	KSO10	KSO14
6	KSO11	KSO15
7	KSO12	KSO13
8	KSO14	KSO18
9	KSO13	KSO17
10	KSO15	KSO19
11	KSO16	KSO20
12	KSO12	KSO16
13	KSO10	KSO14
14	KSO2	KSO2
15	KSO1	KSO1
16	KSO3	KSO3
17	KSO8	KSO12
18	KSO6	KSO6
19	KSO7	KSO11
20	KSO4	KSO8
21	KSO5	KSO5
22	KSO10	KSO10
23	KSI3	KSI3
24	KSI1	KSI1
25	KSI5	KSI5
26	KSI2	KSI2
27	KSI4	KSI4
28	KSI6	KSI6
29	KSI7	KSI7
30	Diag_Loop	

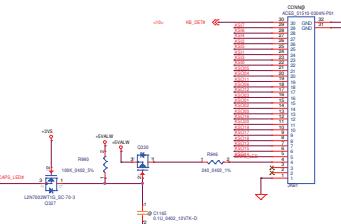
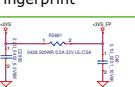


Connector for Keyboard Backlight



A00_0321: add PD for Backlight light issue
A00_0321: Keyboard Brightness display too dark.

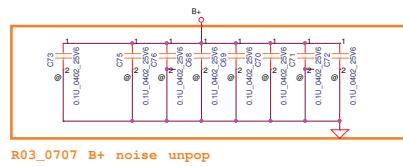
Fingerprint



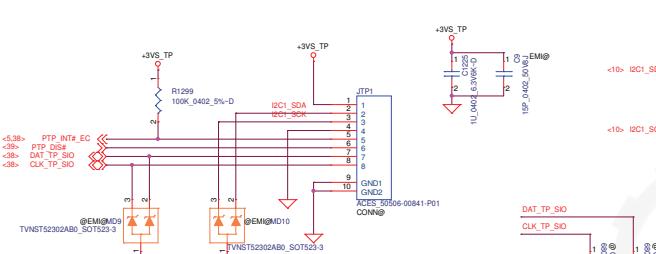
Security Classification	Control Serial Data	Compaq Electronics, Inc.	
Issued Date	2011/06/02	Document Date	2013/10/08
Rev	00	Ver	00

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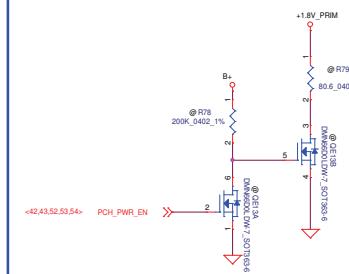
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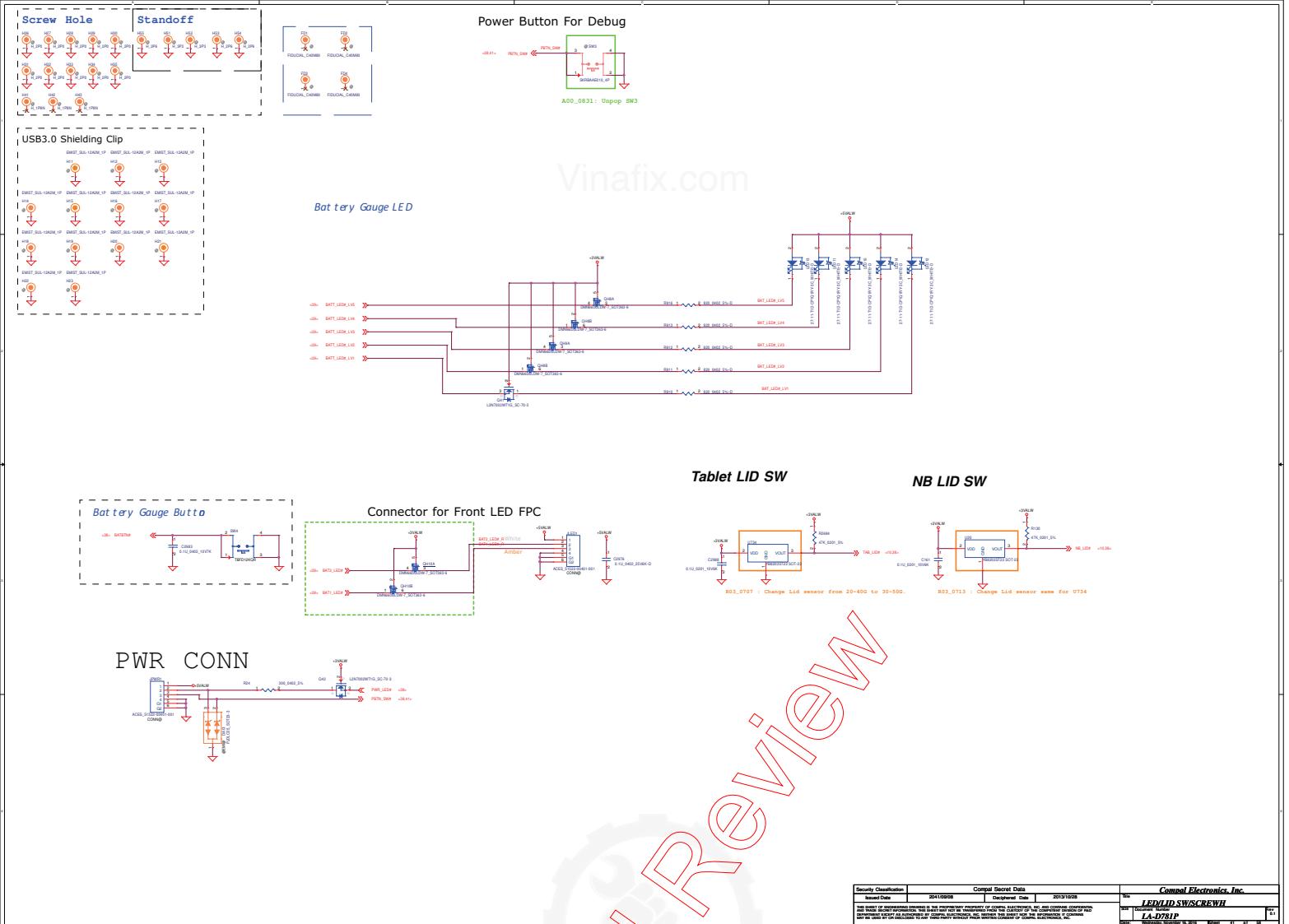
Touchpad CONN

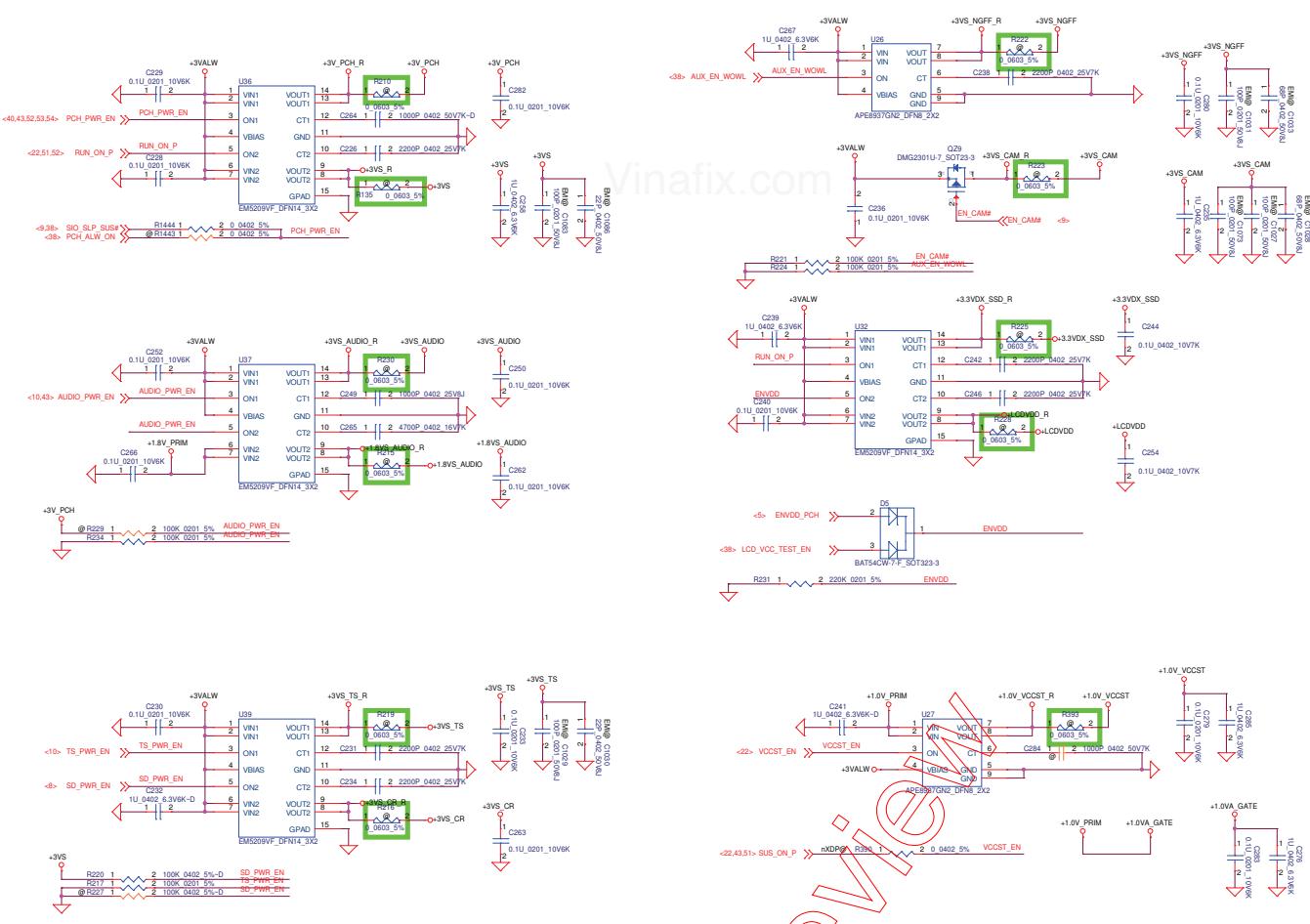


+1.8VA Discharge



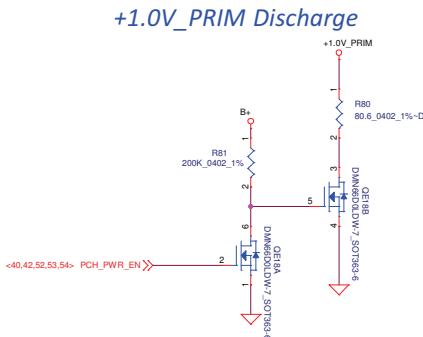
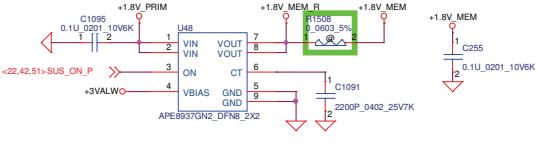
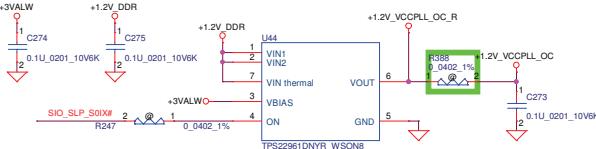
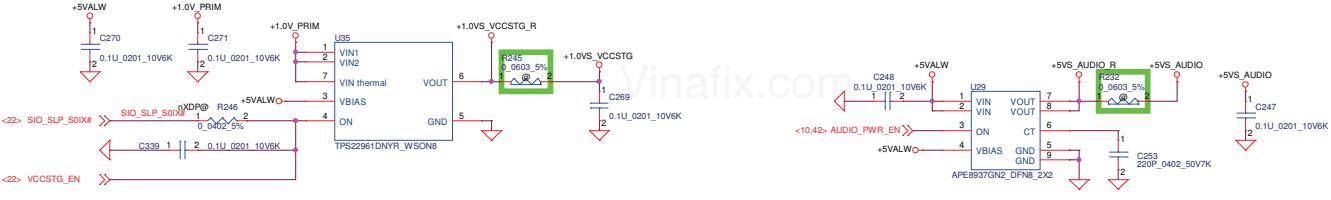
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		Size	Document Number
			LA-D781P
		Date	Wednesday, November 16, 2016
		Sheet	40 of 58
			Rev 0.1



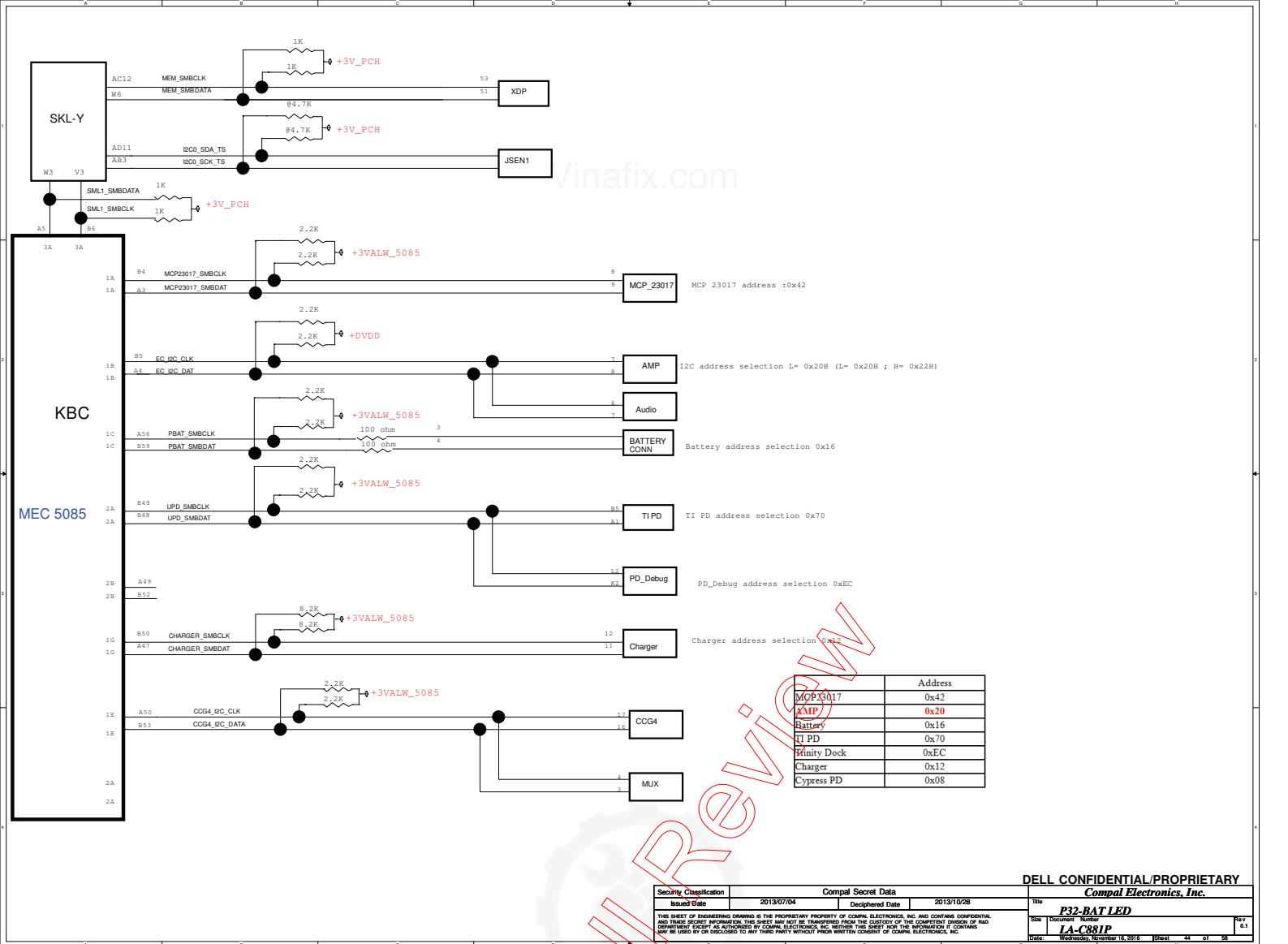


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Size	Document Number		Rev		
	LA-D311P		0.1		
Date:	2013-10-15, 2016		Sheet	42	01



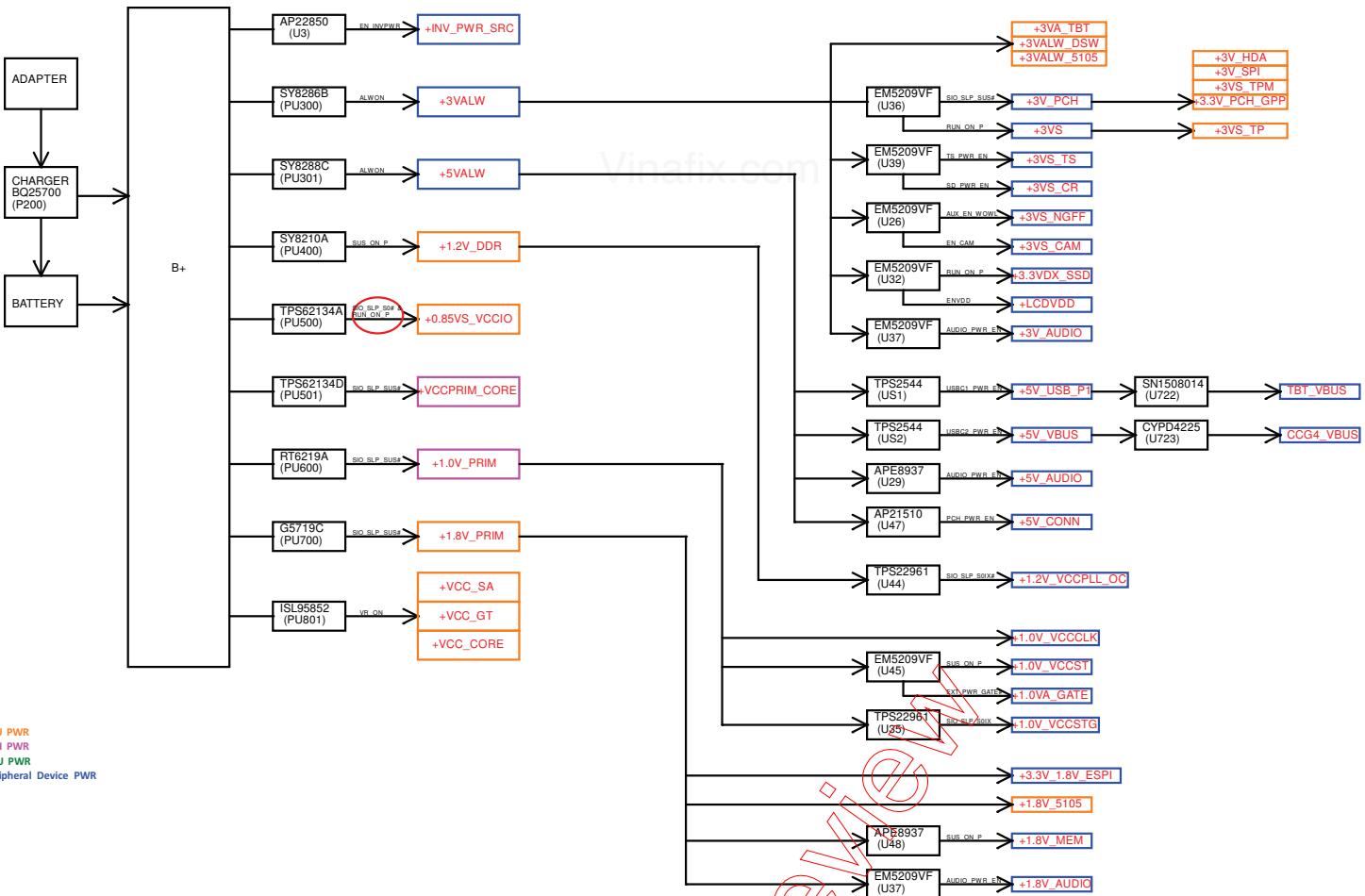
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	DC/DC Interface 2
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Size	Document Number				Rev 0.1
LA-D311P					
Date:	Wednesday, November 16, 2016	Sheet:	43	of	58



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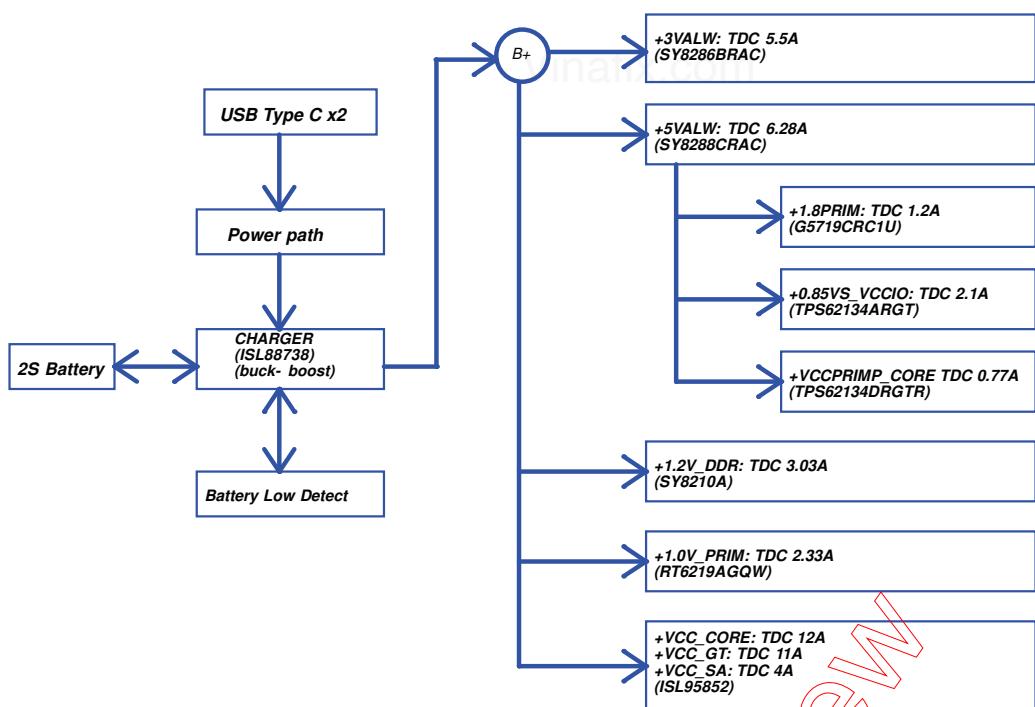
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Issued Date	2013/07/04
Deciphered Date	2013/10/28
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Ref	0.1
Doc ID:	P32-BATLED
Rev	0.1
Date:	Wednesday, November 8, 2017
Start	44
End	58

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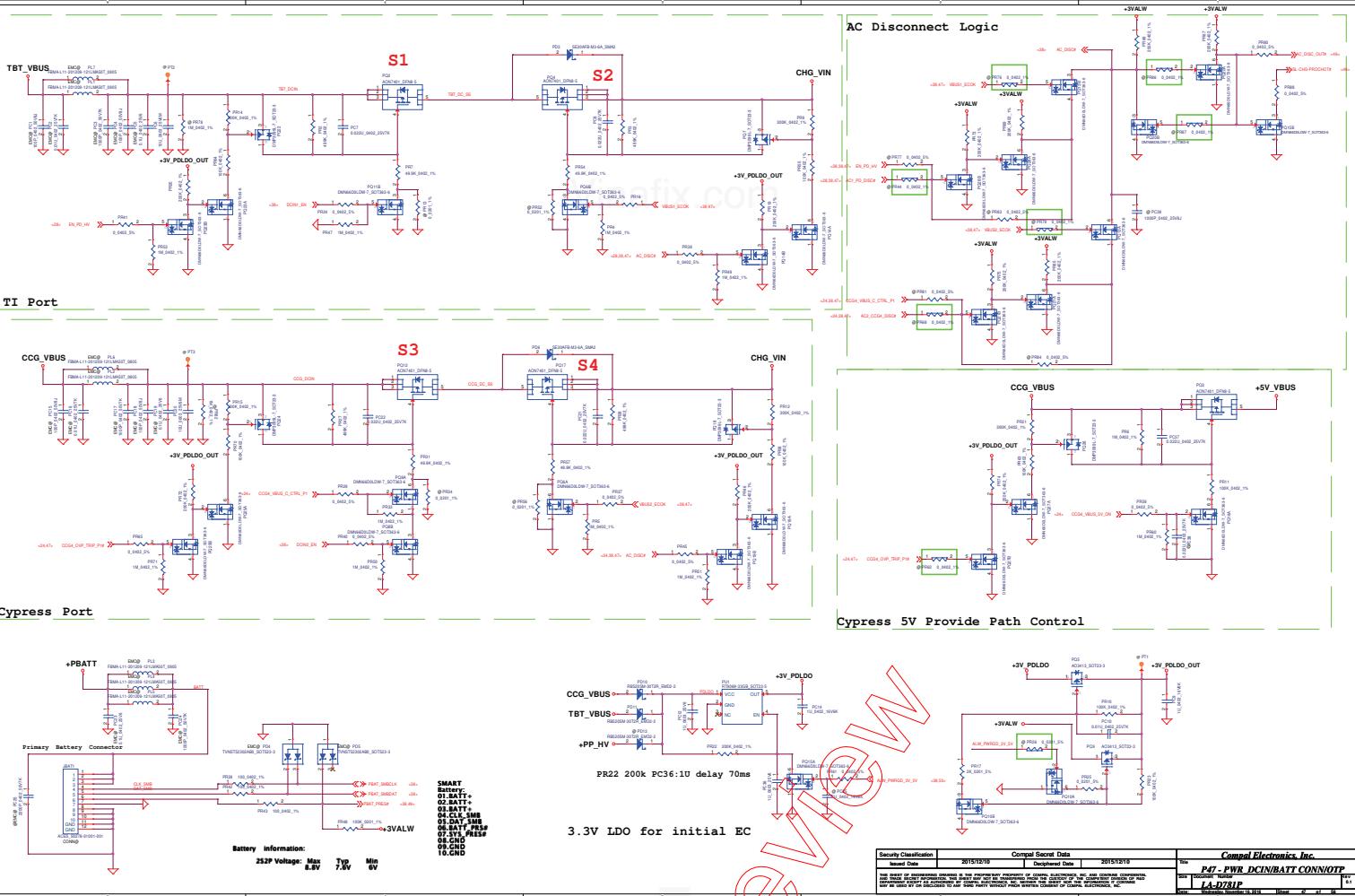
CPU PWR
PCH PWR
GPU PWR
Peripheral Device PWR

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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Rev	0.1
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Site	Document Number	PS5-PWR_PIR-1		Rev	0.1
Date	LA-C881P	Wednesday, November 16, 2016	Sheet	45	of 58



Compal Electronics, Inc.			
<i>P46 - PWR POWER BLOCK DIAGRAM</i>			
Security Classification	Compal Secret Data		
Issued Date	2015/12/10	Deciphered Date	2015/12/10
Size	Document Number	Rev	
	LA-D781P	0.1	
Date:	Wednesday, November 16, 2016	Sheet 46 of 56	

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Security Classification	Compel Secret Data
Initial Date	2015/12/15
Declassified Date	2015/12/15
Site	P47 - PWR DCIN/BATT CONN/OTP
Document Name	LA-D781P
Page	02 of 41

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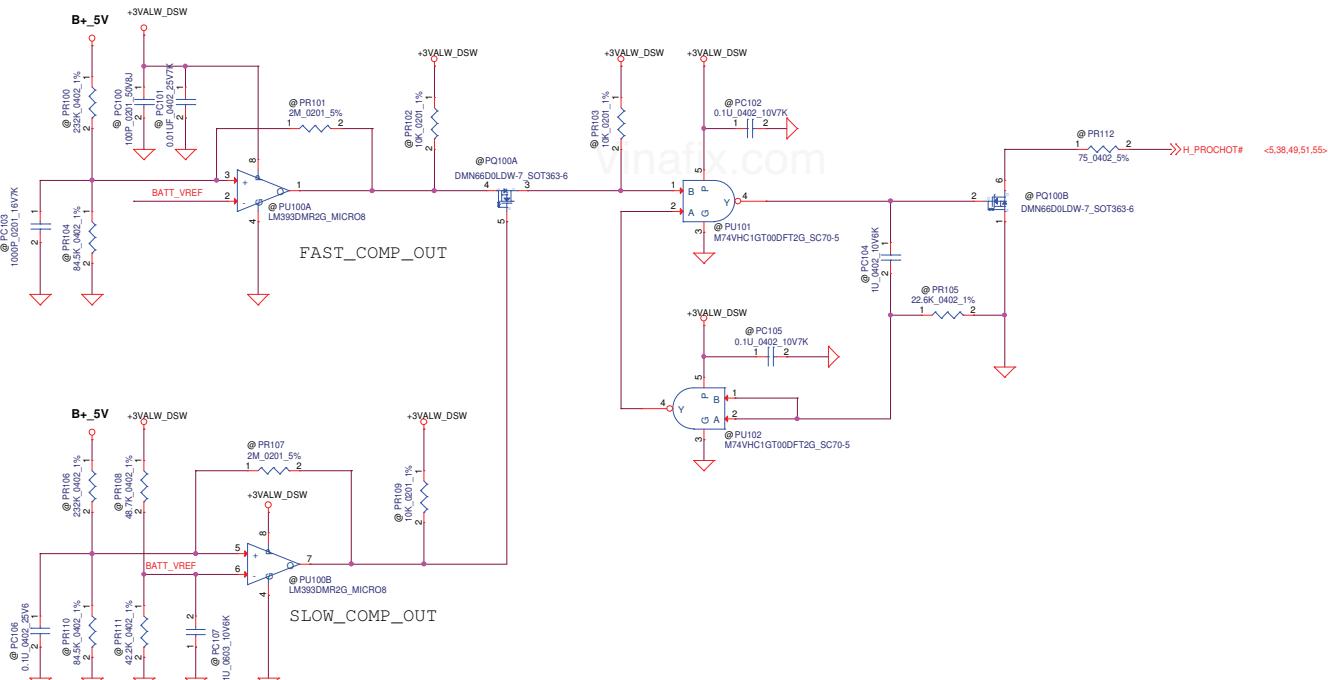
SMART
BATTERY:
01_BATT*
02_BATT*
03_BATT*
04_BATT*
05_BATT*
06_BATT*
07_BATT*
08_BATT*
09_GND
10_GND

Battery Information:
2S2P Voltage Max 8.8V Min 6V

PR22 200k PC36:1U delay 70ms

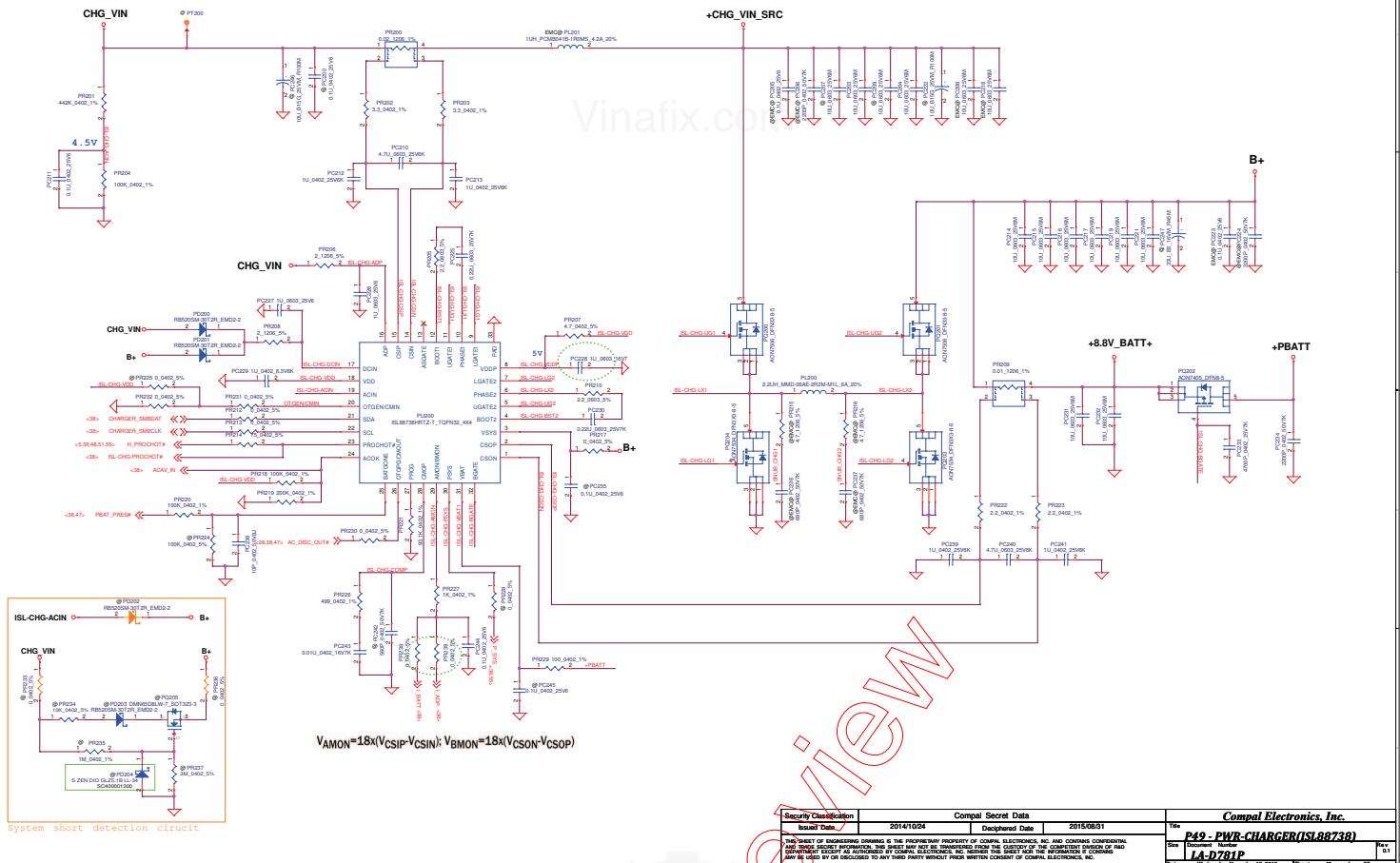
3.3V LDO for initial EC

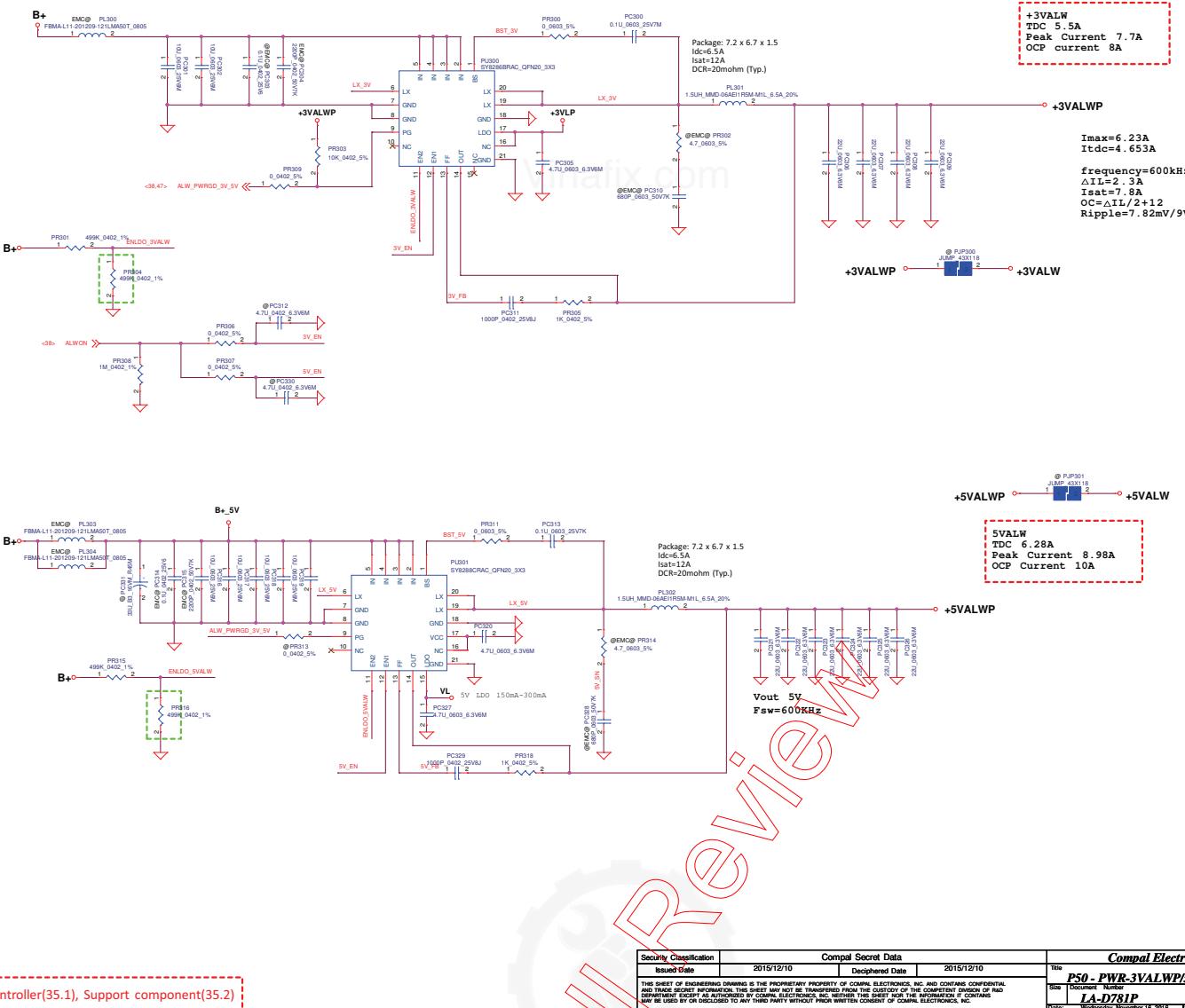
BATT low voltage detect



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Issued Date	2015/12/10	Deciphered Date	2015/12/10	Title
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Size	Document Number	P48 - PWR DIS BAT PROCHOT#		
	LA-D781P	Rev 0.1		
Date:	Wednesday, November 16, 2016	Sheet	48	of 56

For Dell Review

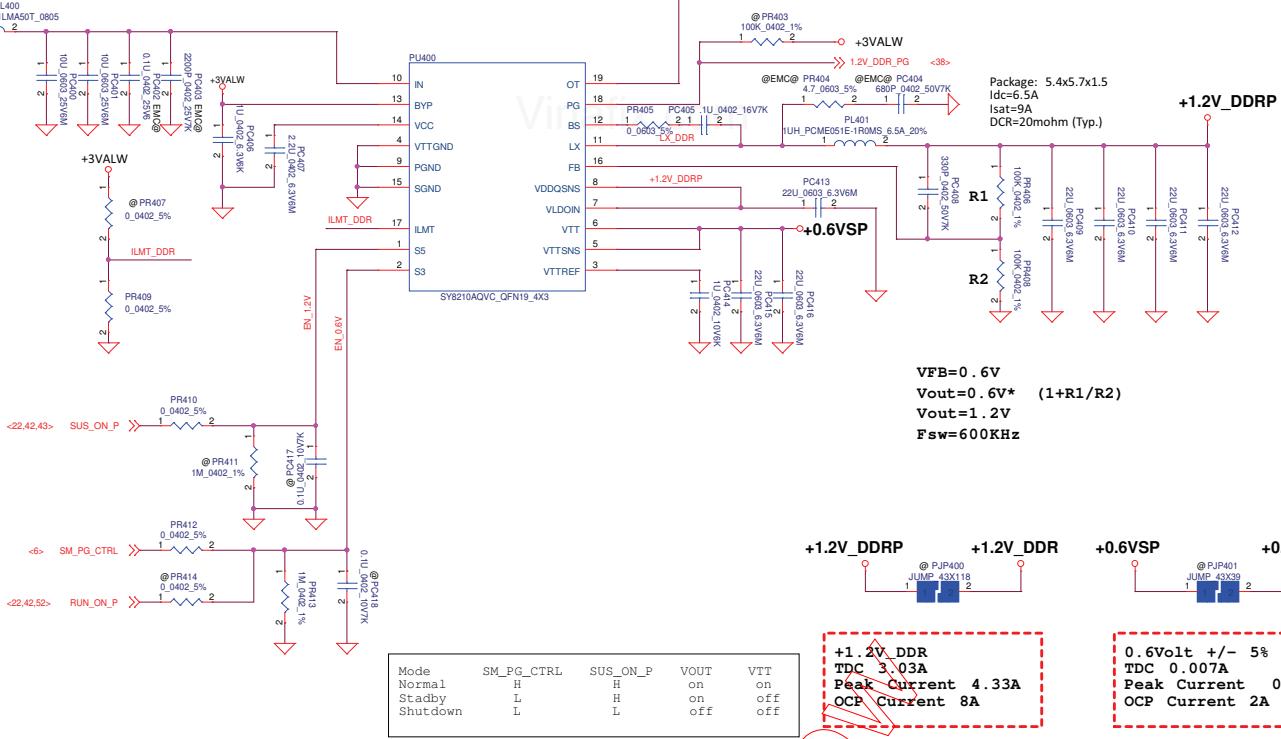




B+

EMC@ PL400

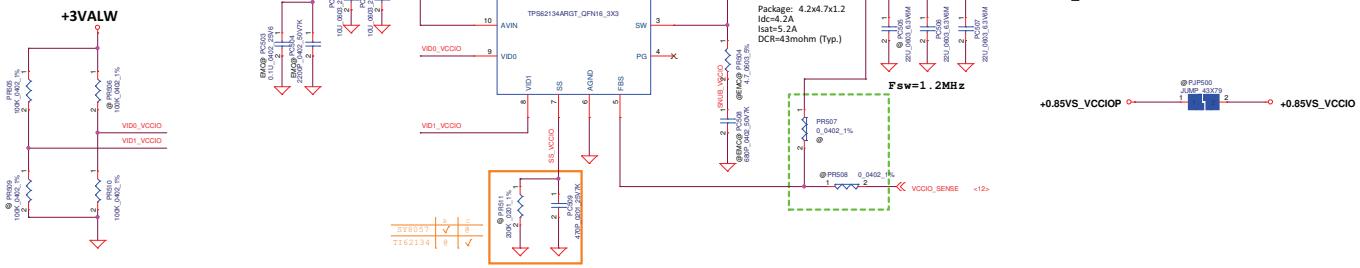
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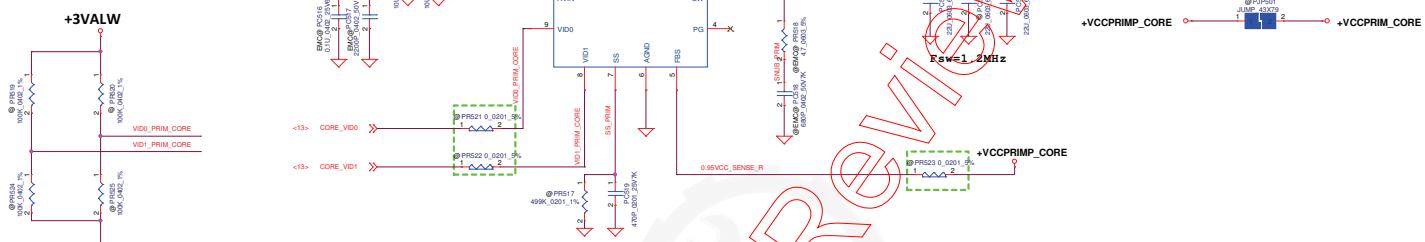
DDR controller(35.3), Support component(35.4)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	Deciphered Date	2015/12/10	2015/12/10	Title	P51 - PWR +1.2V DDR/0.6VS
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Size	Document Number	LA-D781P	Rev 0.1	Date:	Wednesday, November 16, 2016
					1 Sheet 51 of 56

TPS62134A			
LP	VID1	VID0	Vout(V)
0	X	X	0.00
1	0	0	0.850
1	0	1	0.875
1	1	0	0.950
1	1	1	0.975

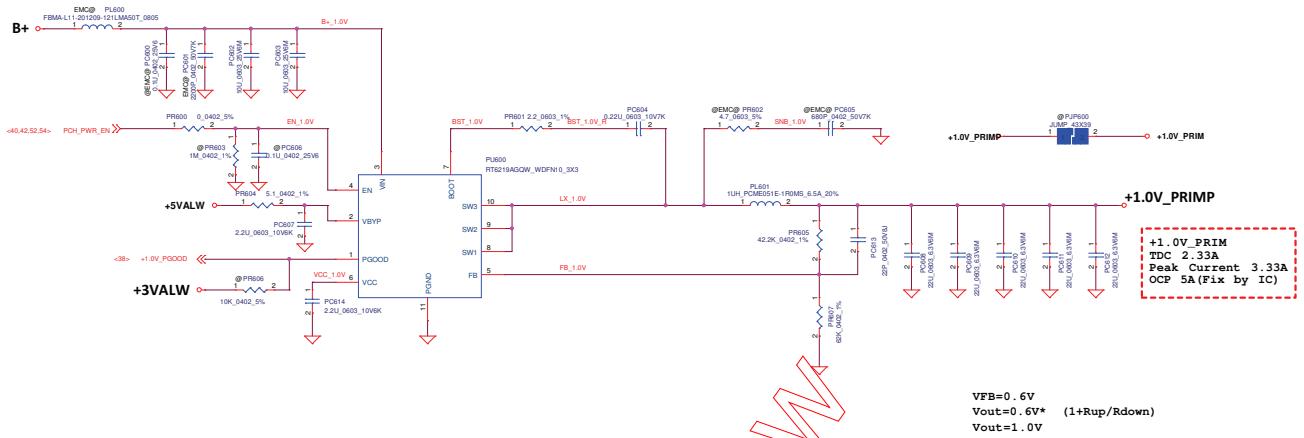


TPS62134D			
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1	0	0	0.850
1	0	1	0.900
1	1	0	0.950
1	1	1	1.000



For Dell

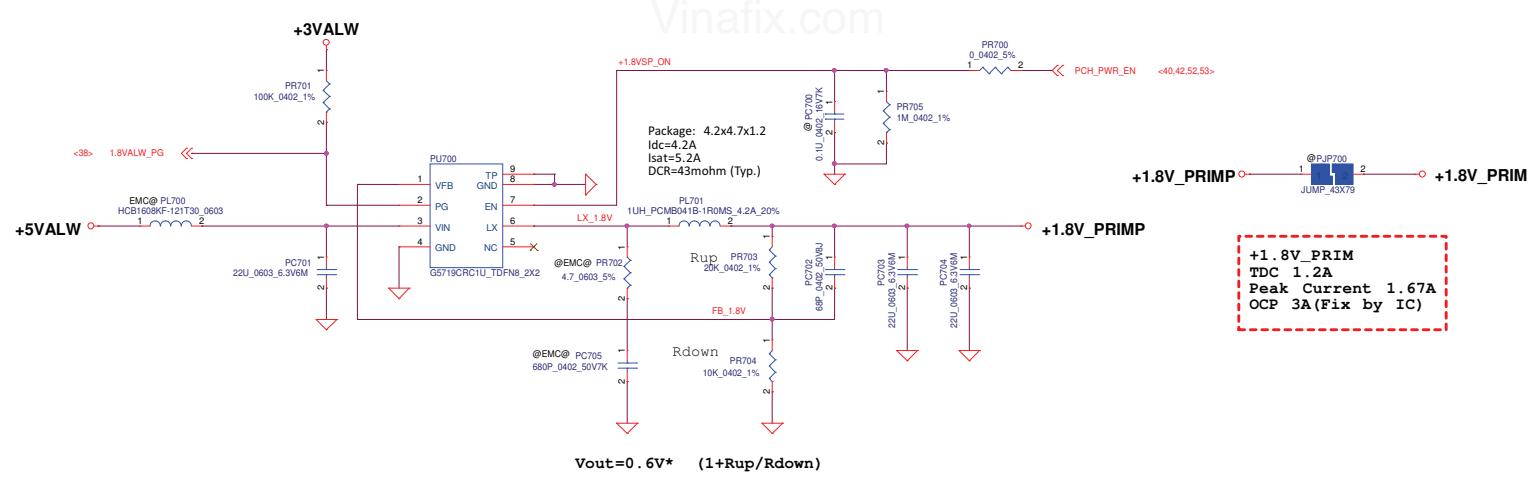
Security Classification	Compal Secret Data			Compal Electronics, Inc.					
Issue Date	2015/12/10	Deciphered Date	2015/12/10	Title	P52 - PWR VCCIO/PRIM CORE				
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				DB-1942P					



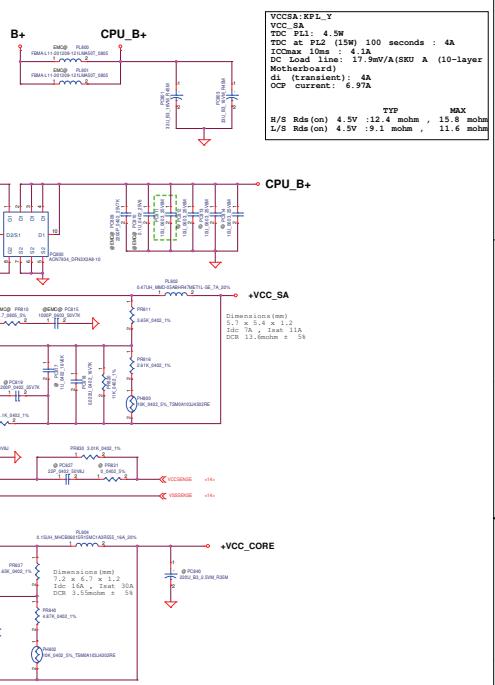
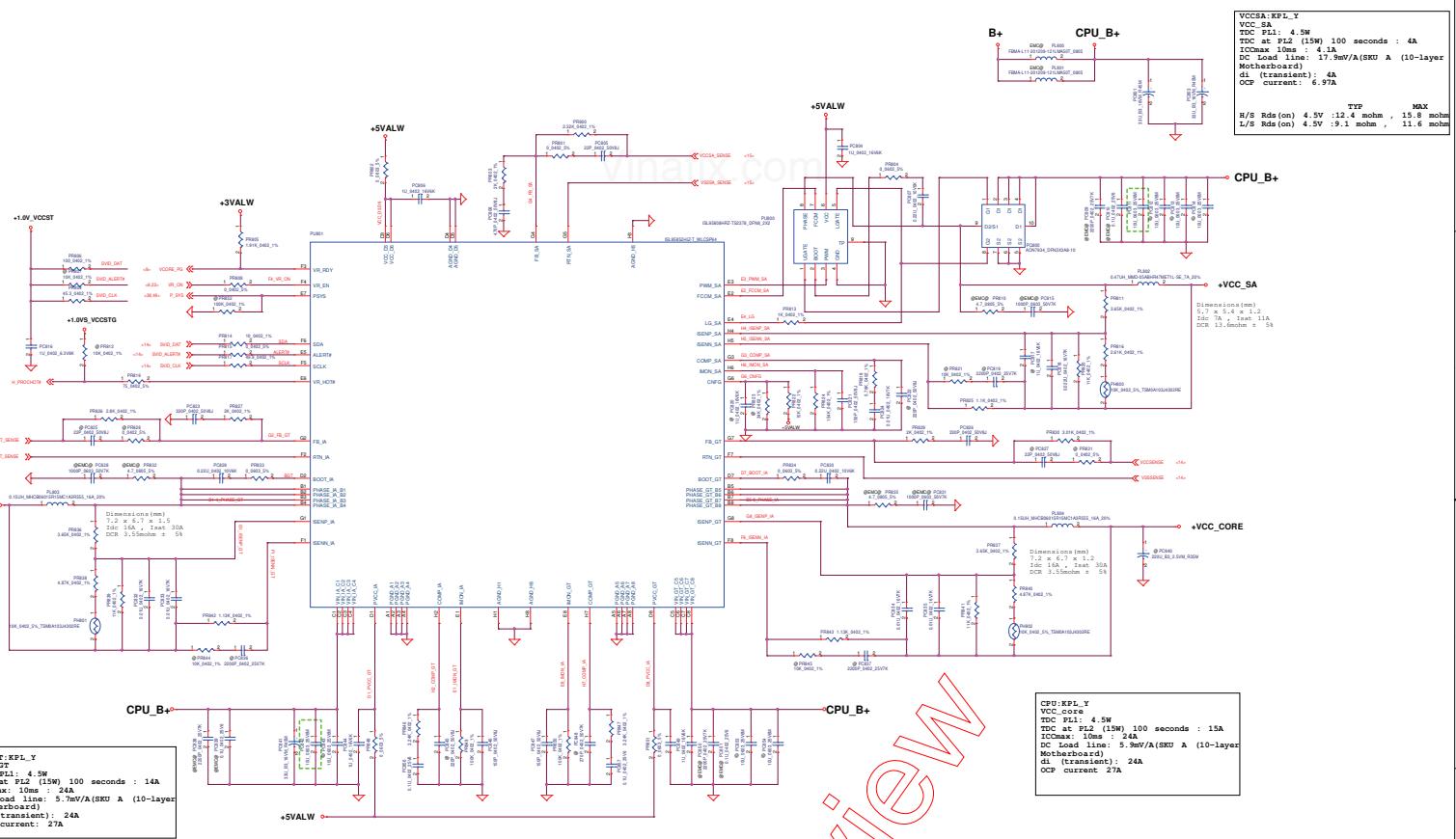
VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.0V

+1.0V_PRIM
TDC 2.33A
Peak Current 3.33A
OCP 5A (Fix by IC)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/12/10	Deciphered Date	2012/12/10
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Printed Name	P52 - PWR +1.0V PRIM	Rev	0.1
Date	LA-D781P	Sheet	53
	Wednesday, November 8, 2017	Page	56



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	2015/12/10	LA-D781P	0.1
		Date: Wednesday, November 16, 2016	Sheet 54 of 56



Security Classification	Compaq Secret Data	Compaq Electronics, Inc.
Issued Date	2015/12/16	Declassified Date
		2015/12/16
		PS5 - PWR VCORE/SA/GT 1A-D781P

VCC_CORE

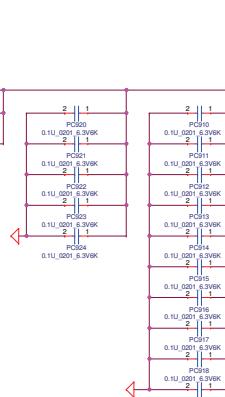
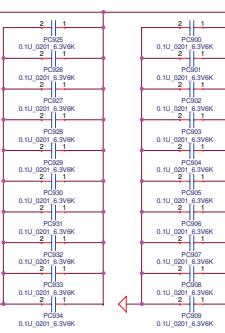
0.1U_0201 * 28 pcs +IU_0201*6 pcs+1IU_0402*9pcs+47U_0603*10pcs

VCC_GT

0.1U_0201 * 15 pcs +IU_0201*6 pcs+1IU_0402*4pcs+1IU_0402*2pcs+47U_0603*13pcs

+VCC_CORE

Back side



VCC_CORE output cap (36.4)

TOP side

VCC_SA output cap (36.6)

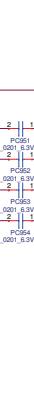
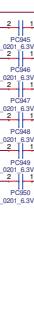
TOP side

VCC_GT output cap (36.5)

TOP side

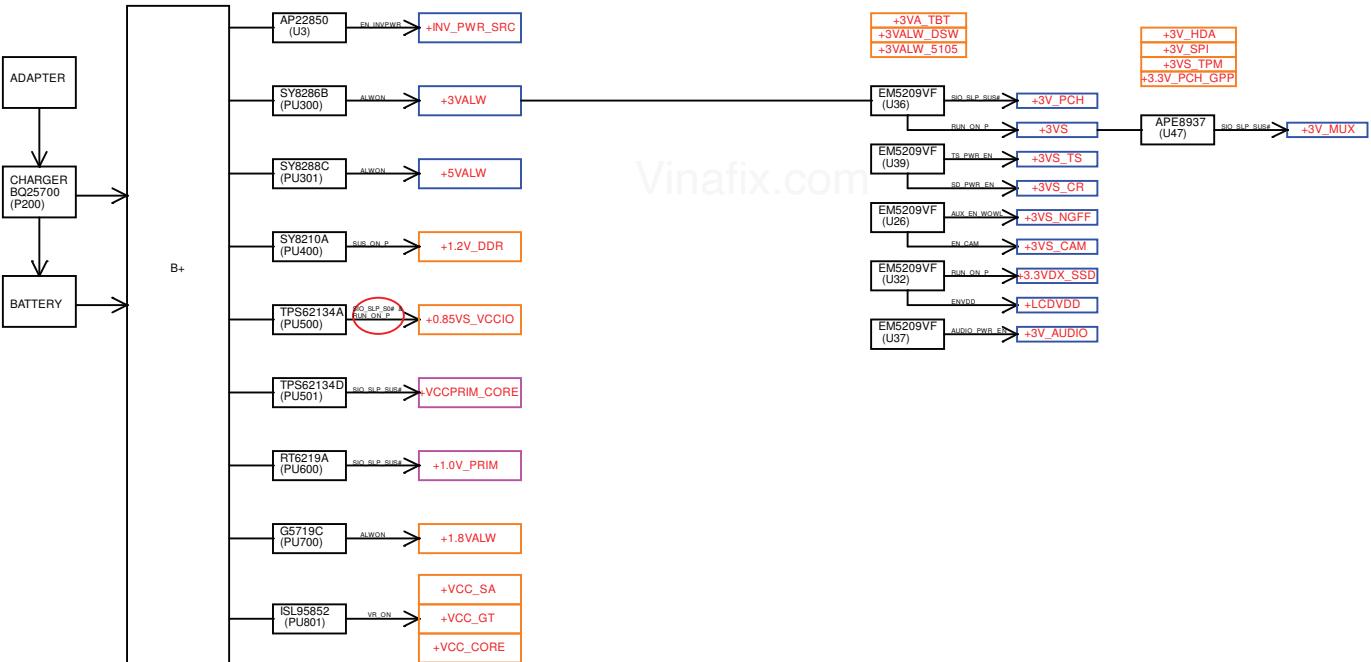
+VCC_SA

Back side

VCC_SA
0.1U_0201 * 5 pcs +47U_0603*11 pcs

TOP side

Serial Classification	Config Set of Data	Config Set of Data	Comment Electronics, Inc.
Issue Date	2015/12/10	Deployment Date	2017/12/10
PCB Description			
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Date: 14/12/2015 Rev: 01			
PCB Revision: LA-D771P			



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Date	14-C861P	Page No.	16/21

