

SUSTAINABLE LOW POWER AI ACCELERATOR DESIGN AND OPTIMISATION USING CADENCE

-BY CADENCECRACKERS

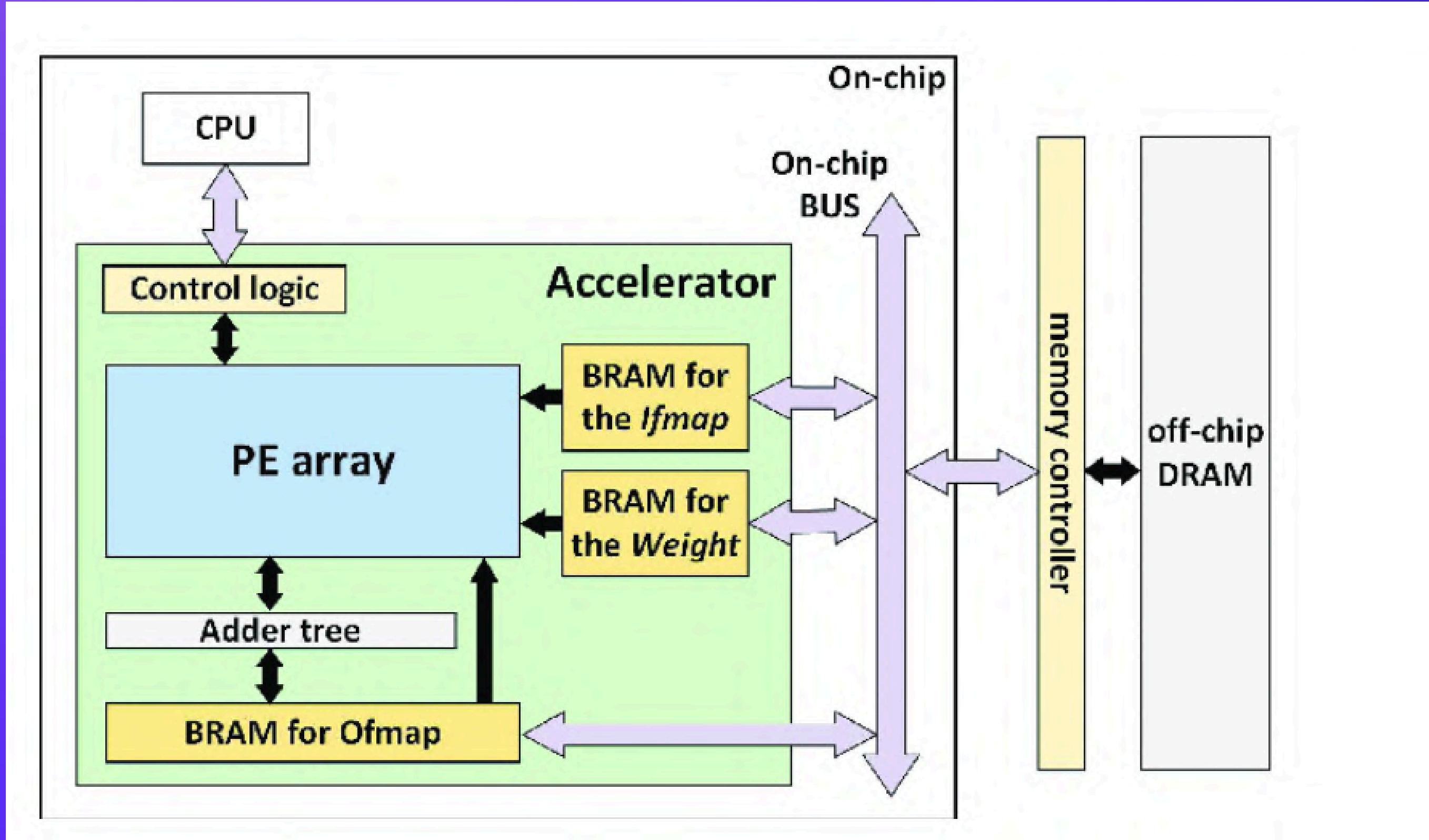


PROJECT INTRODUCTION

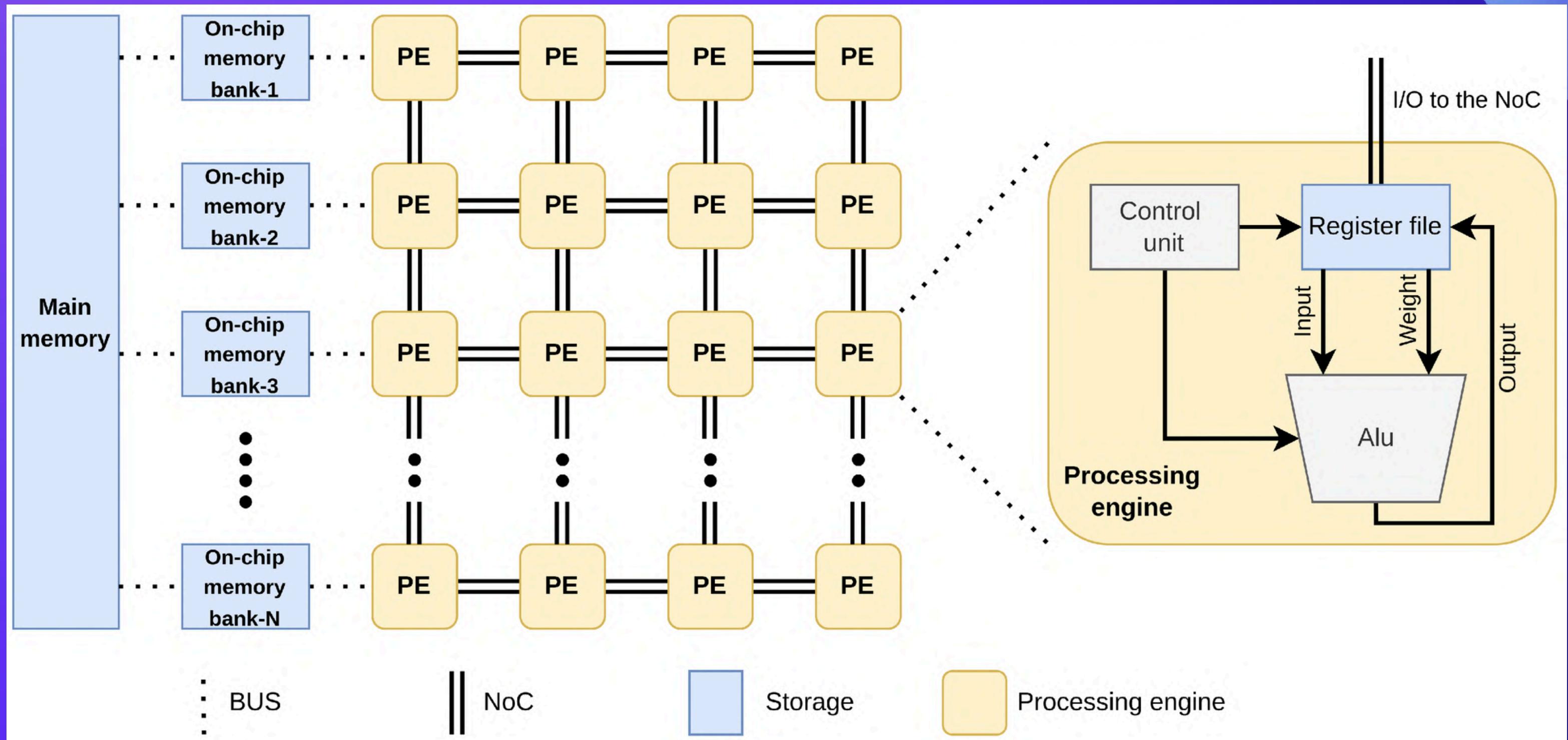
THE PROJECT AIMS TO MINIMIZE THE ENVIRONMENTAL IMPACT OF AI HARDWARE BY OPTIMIZING ARITHMETIC LOGIC UNITS (ALUS). TWO APPROACHES, CONVENTIONAL CMOS AND INNOVATIVE PASS TRANSISTOR LOGIC (PTL), WERE EXPLORED TO BALANCE POWER CONSUMPTION AND COMPUTATIONAL EFFICIENCY. THROUGH METICULOUS DESIGN AND OPTIMIZATION, THE PROJECT DEVELOPS AI ACCELERATORS THAT EXCEL IN PERFORMANCE WHILE PRIORITIZING SUSTAINABILITY. THE REPORT PROVIDES DETAILED METHODOLOGIES, ALU DESIGN INTRICACIES, OPTIMIZATION STRATEGIES, AND EXPERIMENTAL RESULTS.



AI PROCESSING CHIP ARCHITECTURE

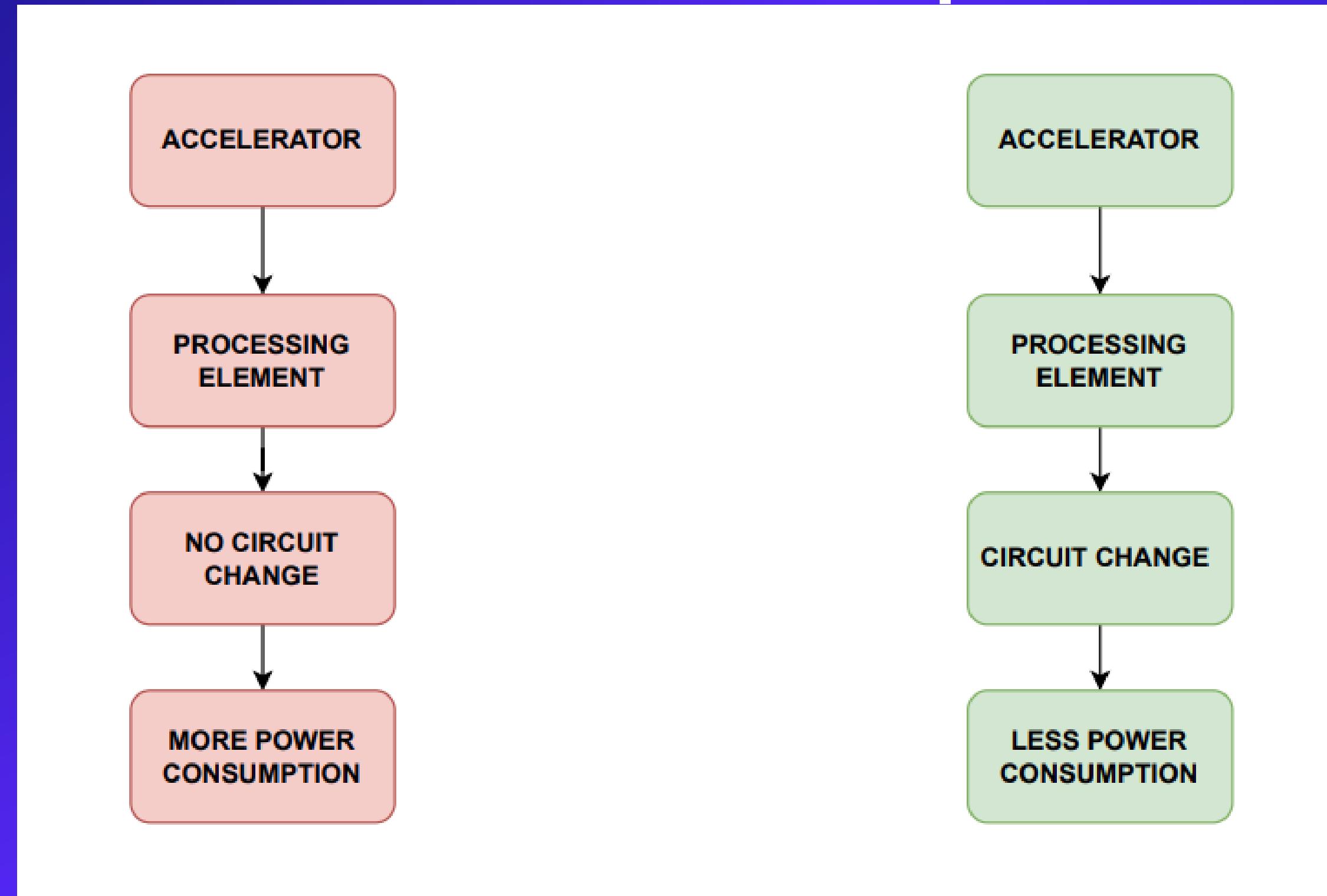


AI ACCELERATOR ARCHITECTURE

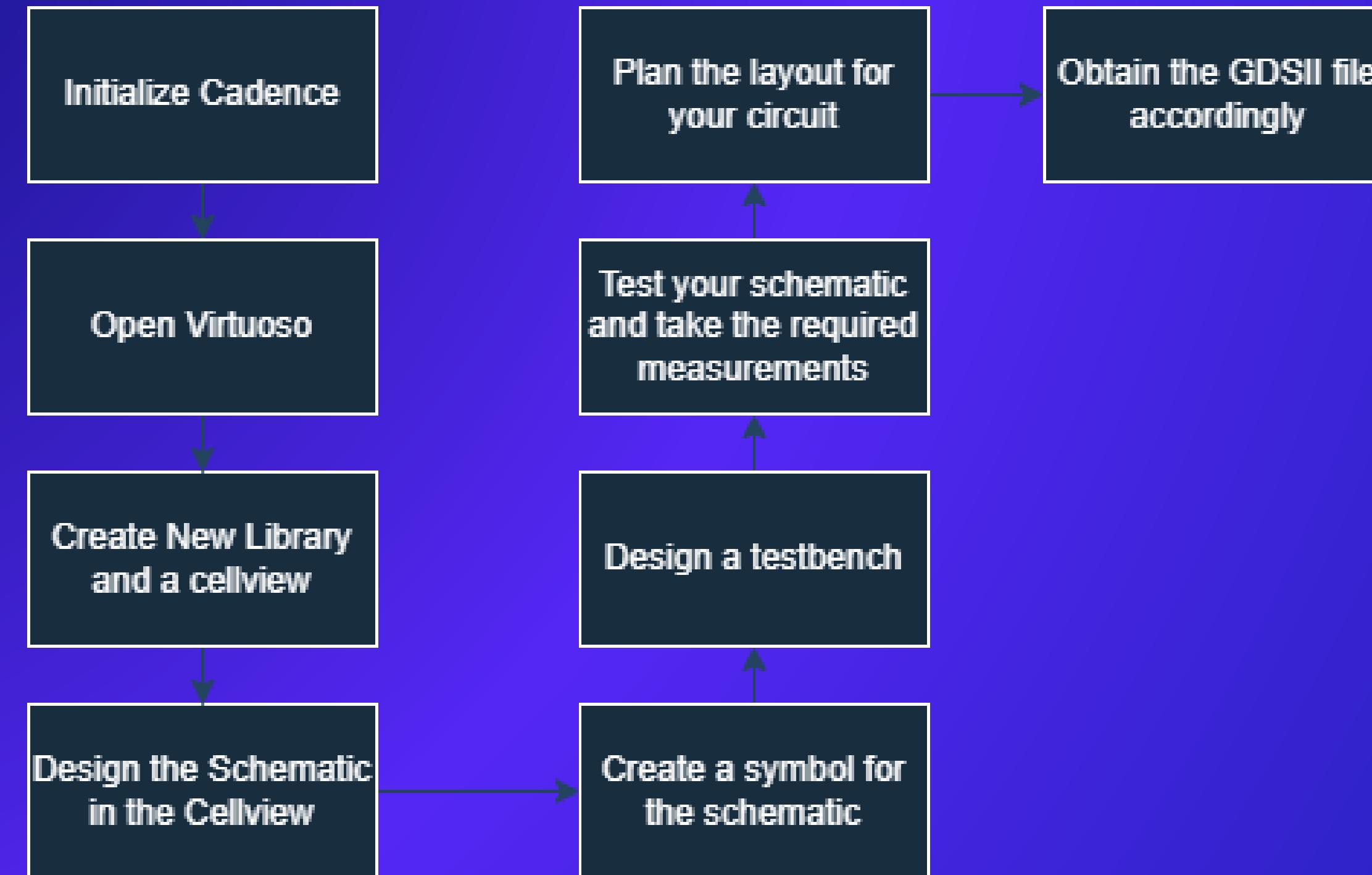


IDEA FLOW

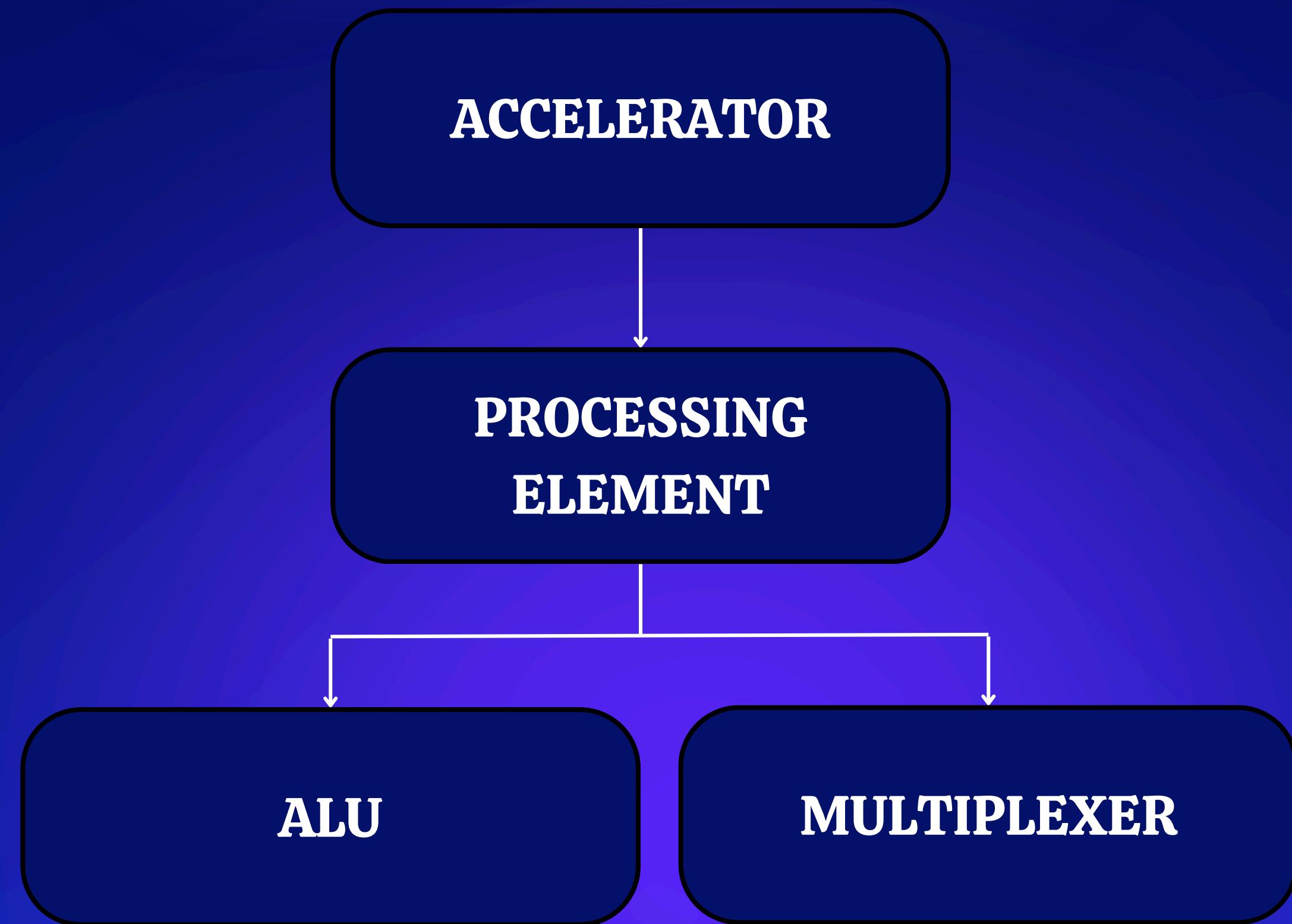
General Flow



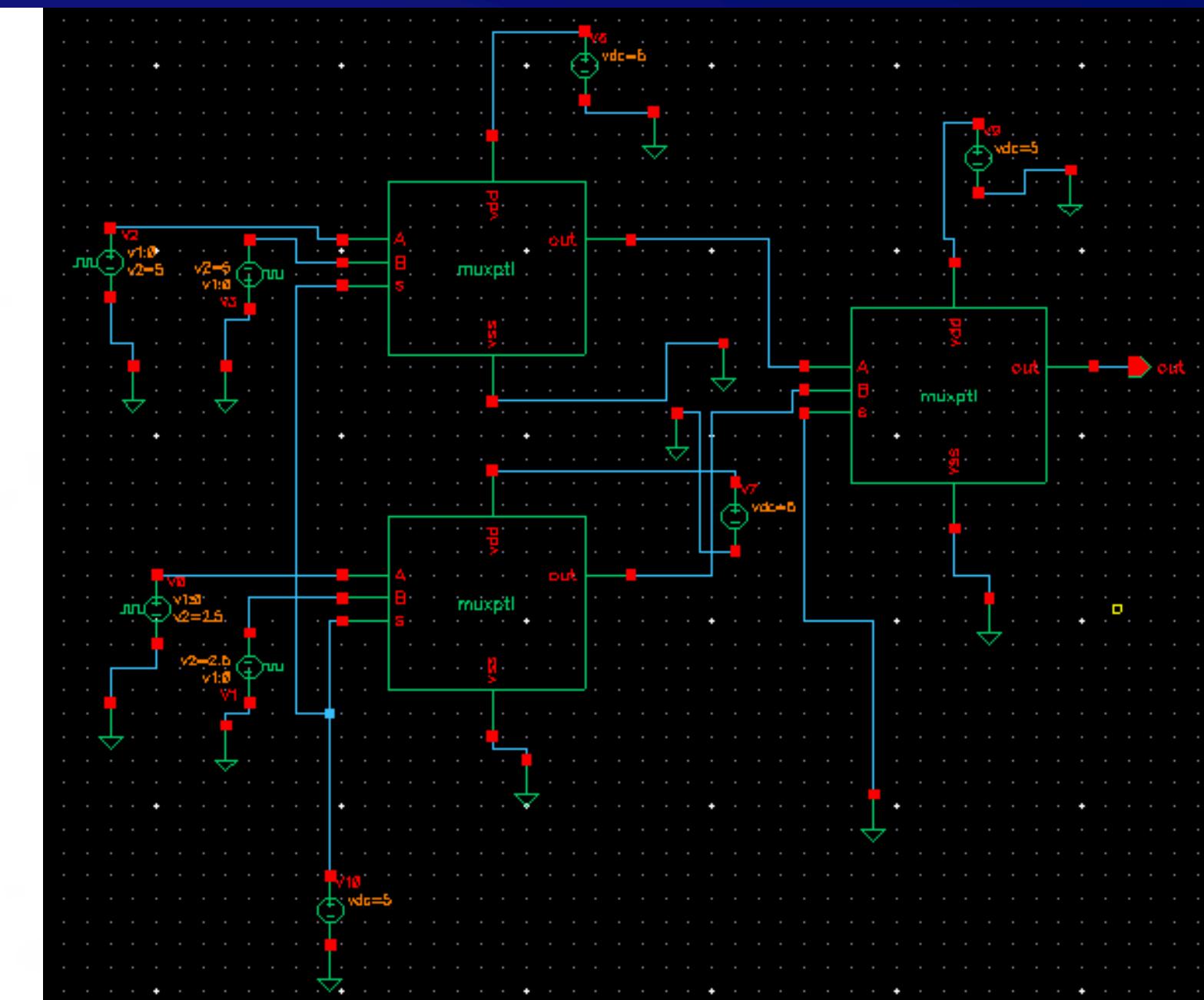
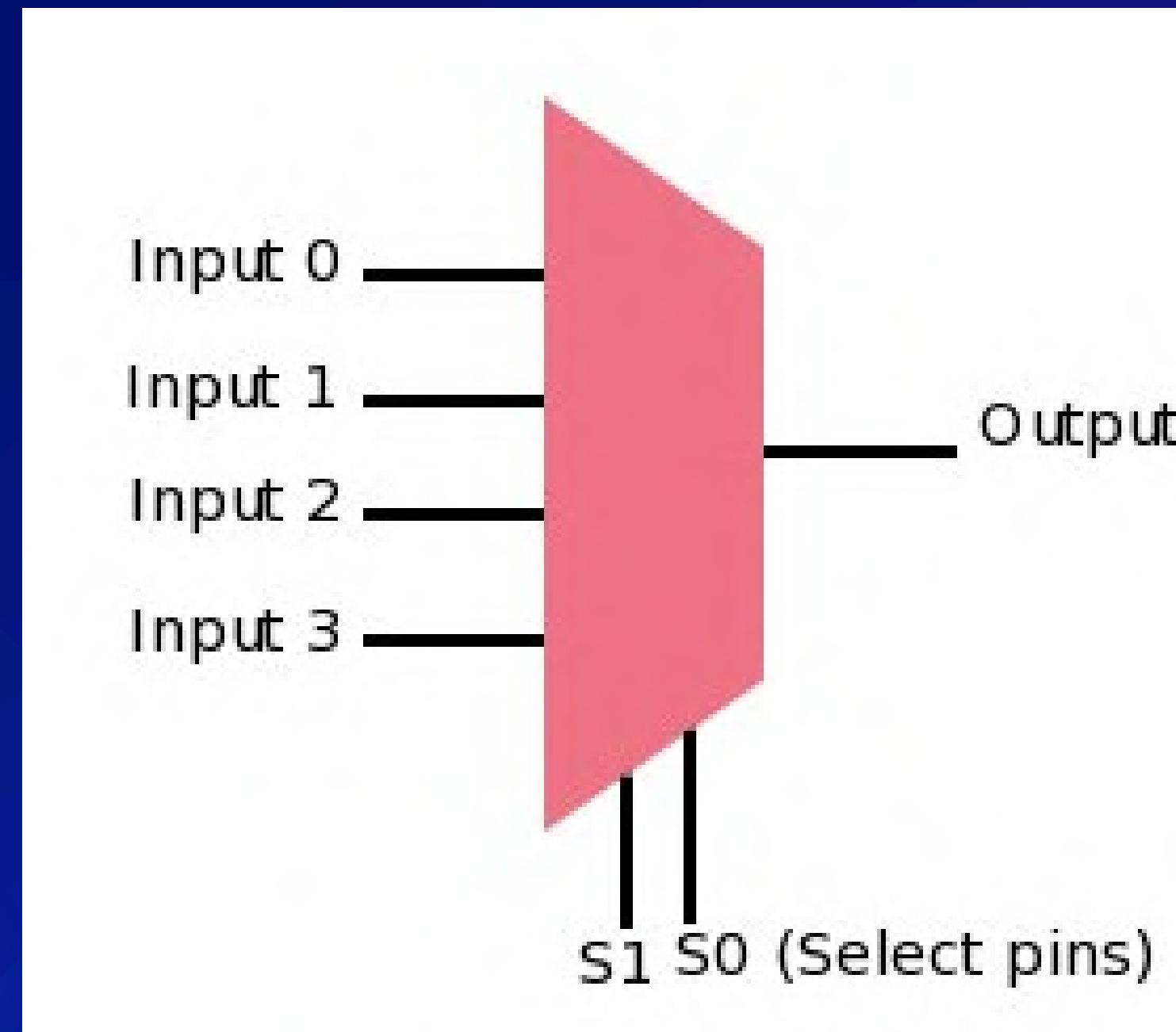
CANDENCE WORK FLOW



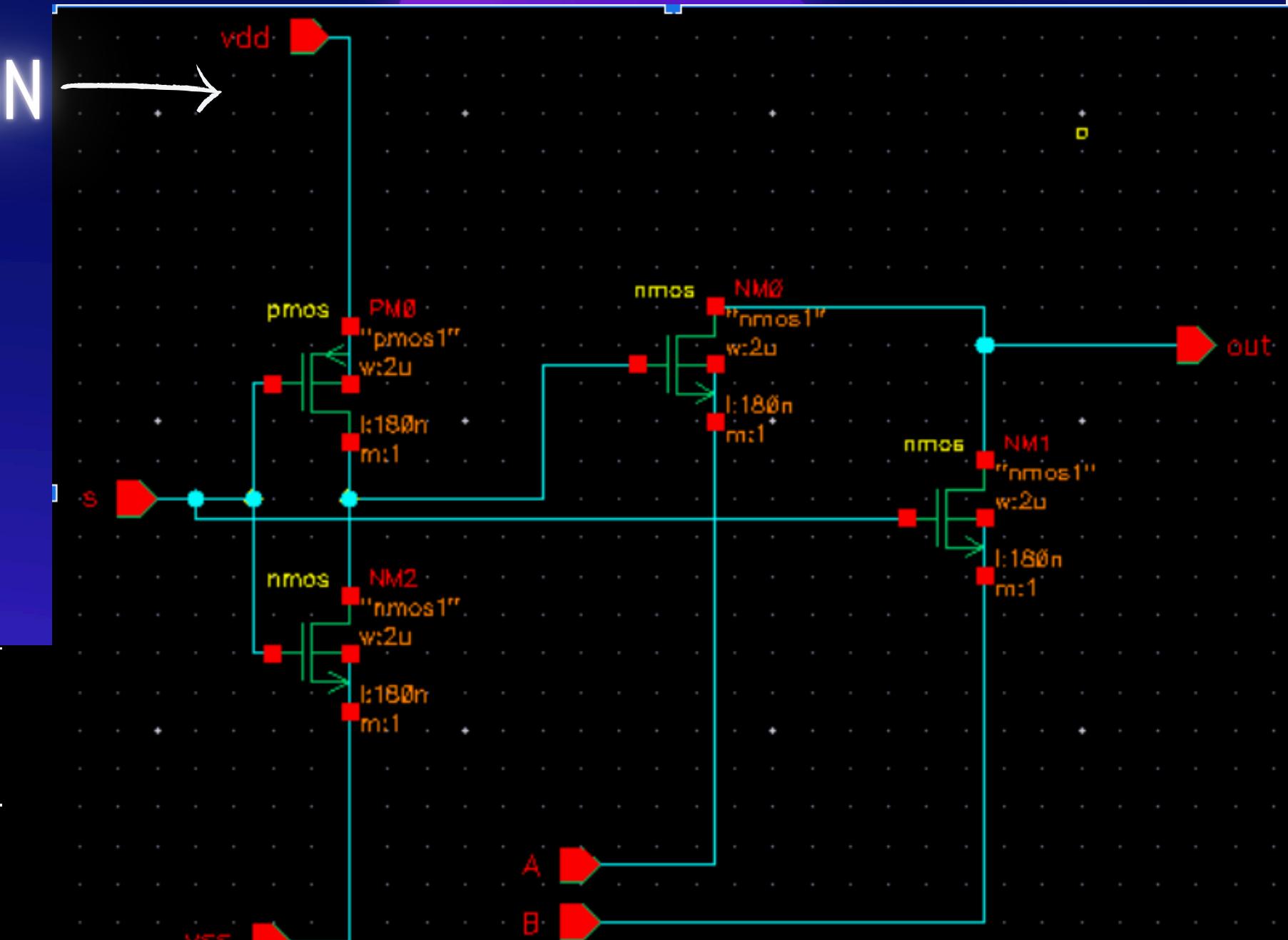
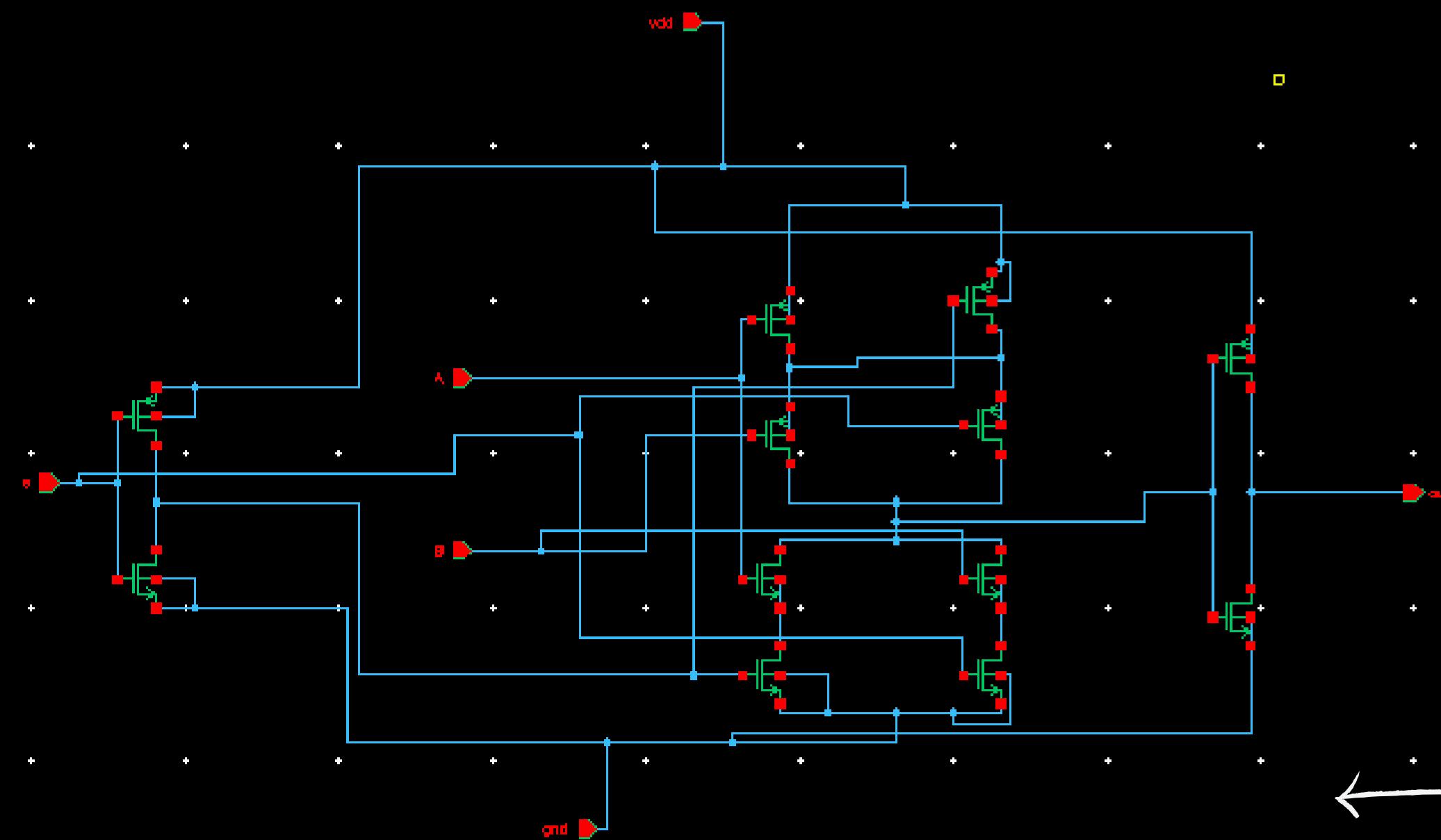
ACCELERATOR FLOW



MULTIPLEXER BLOCK DIAGRAM

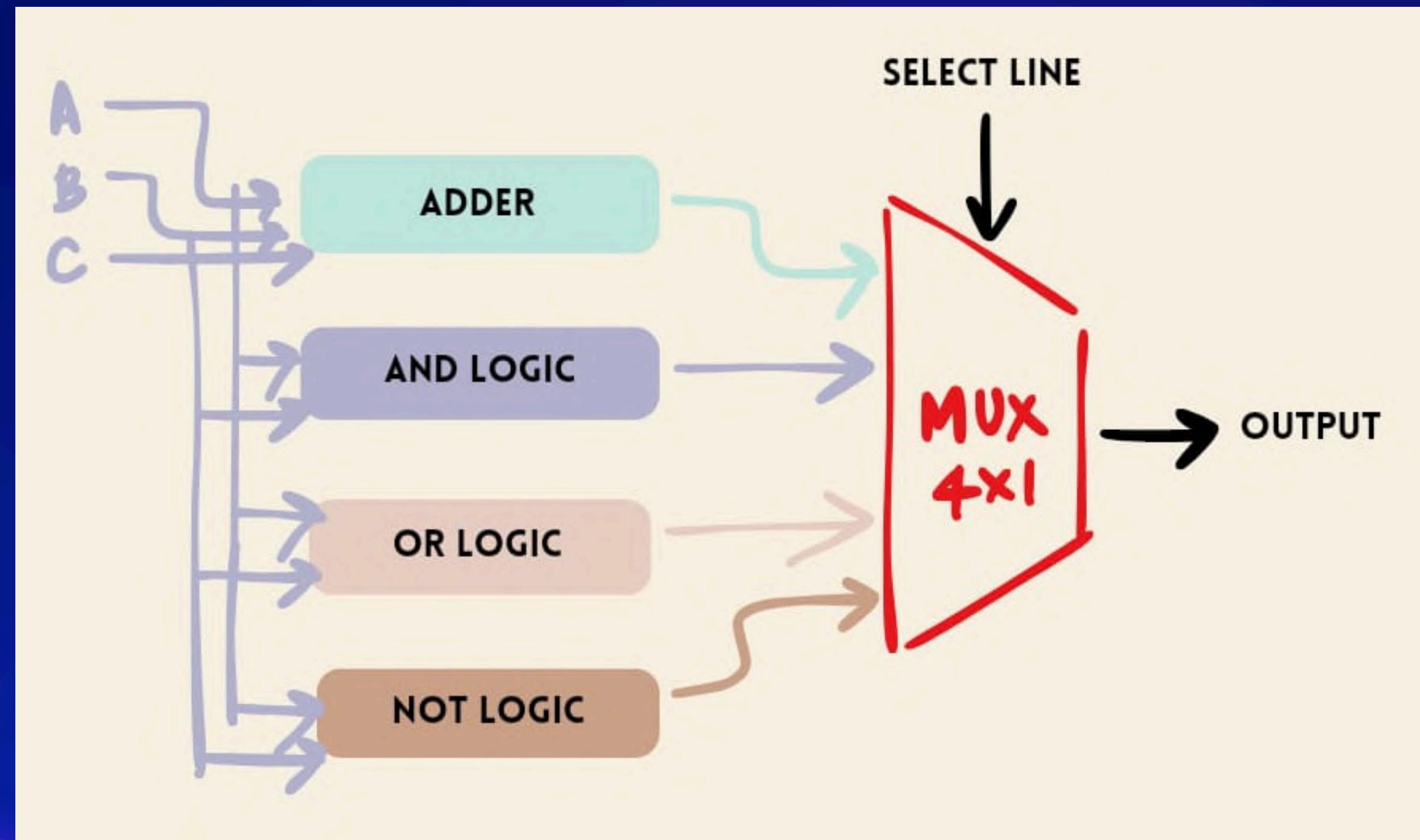


PASS TRANSISTOR MULTIPLEXER DESIGN

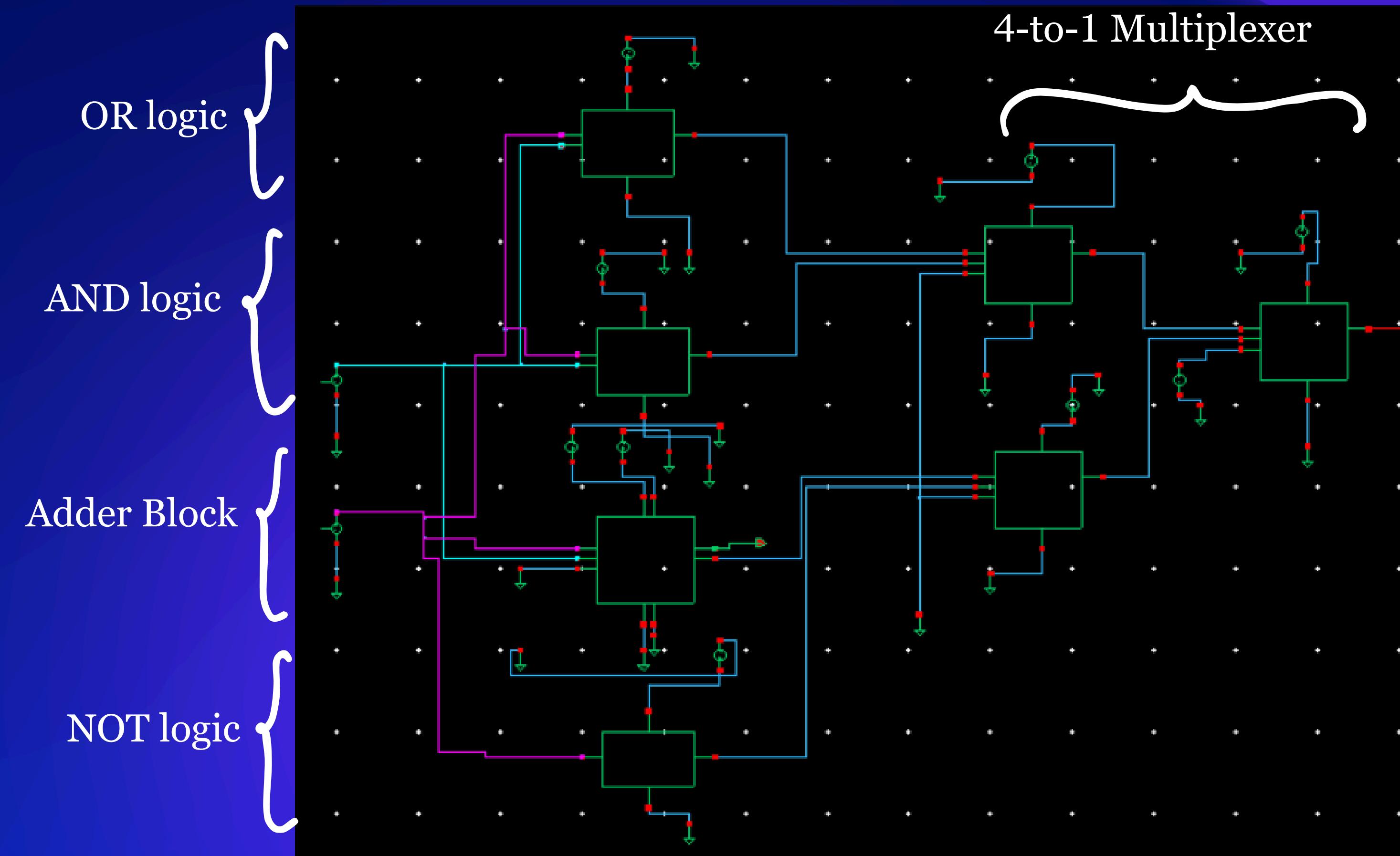


CMOS MULTIPLEXER DESIGN

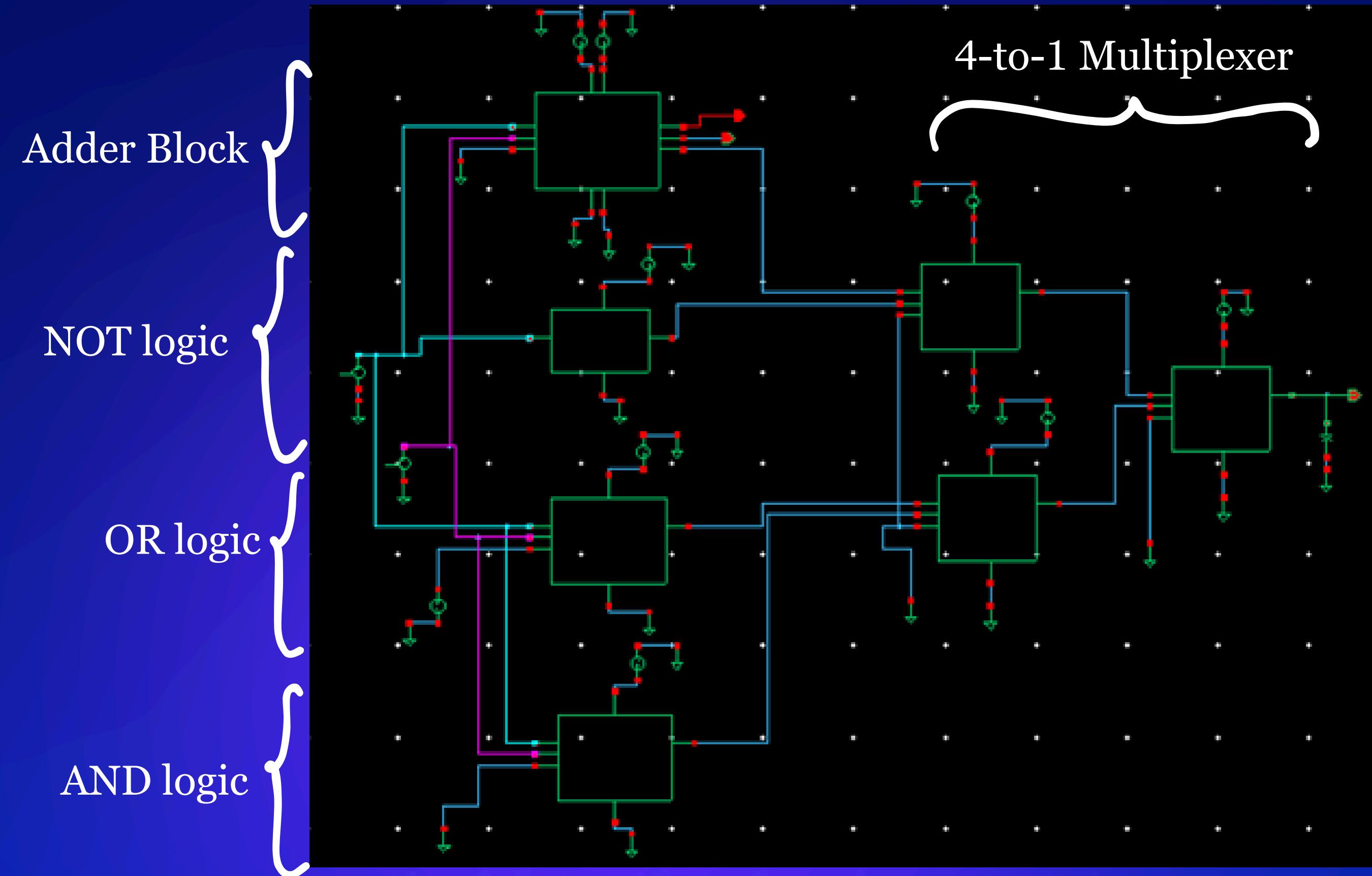
ALU BLOCK DIAGRAM



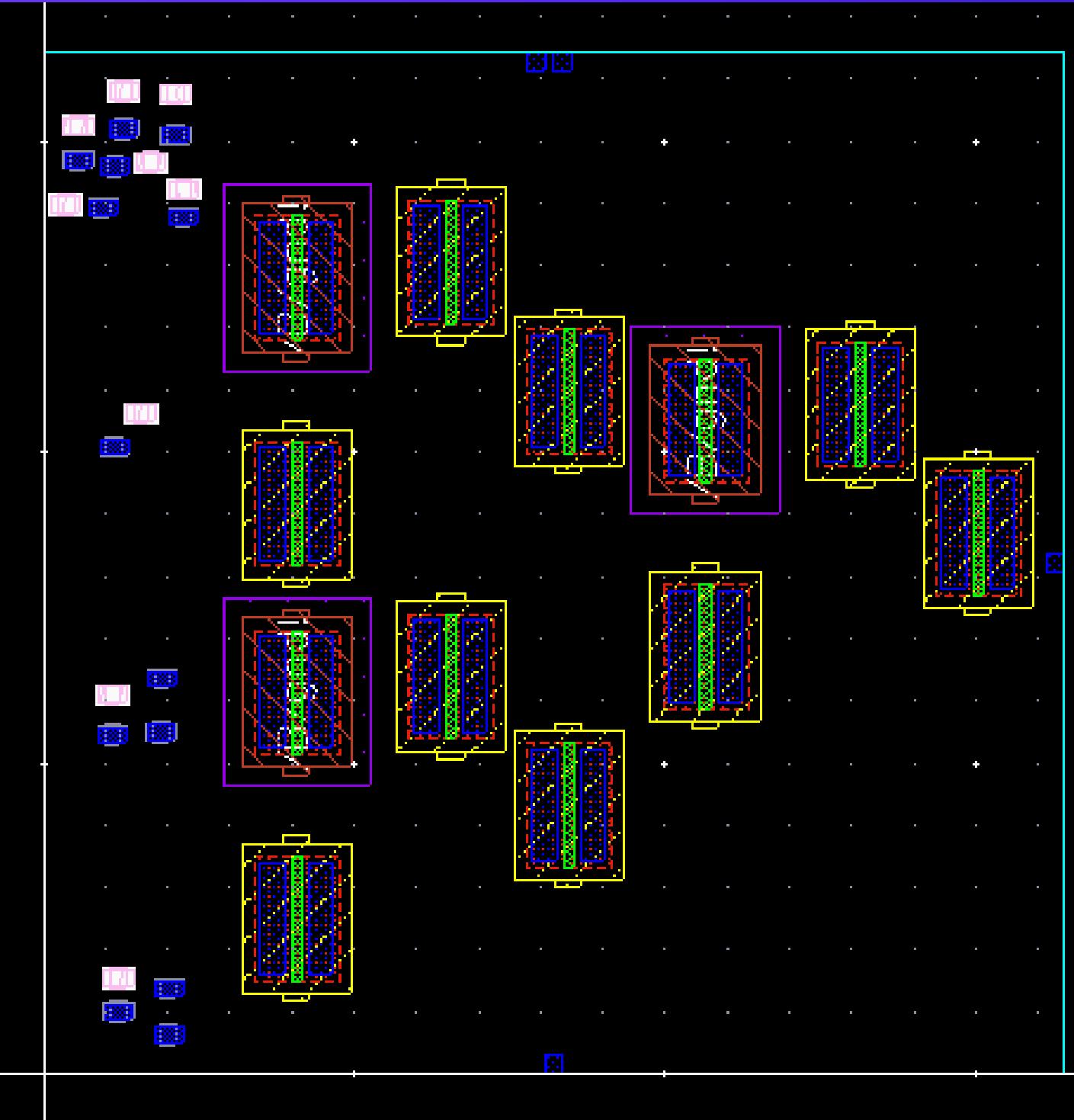
ALU CIRCUIT DIAGRAM COVENTIONAL



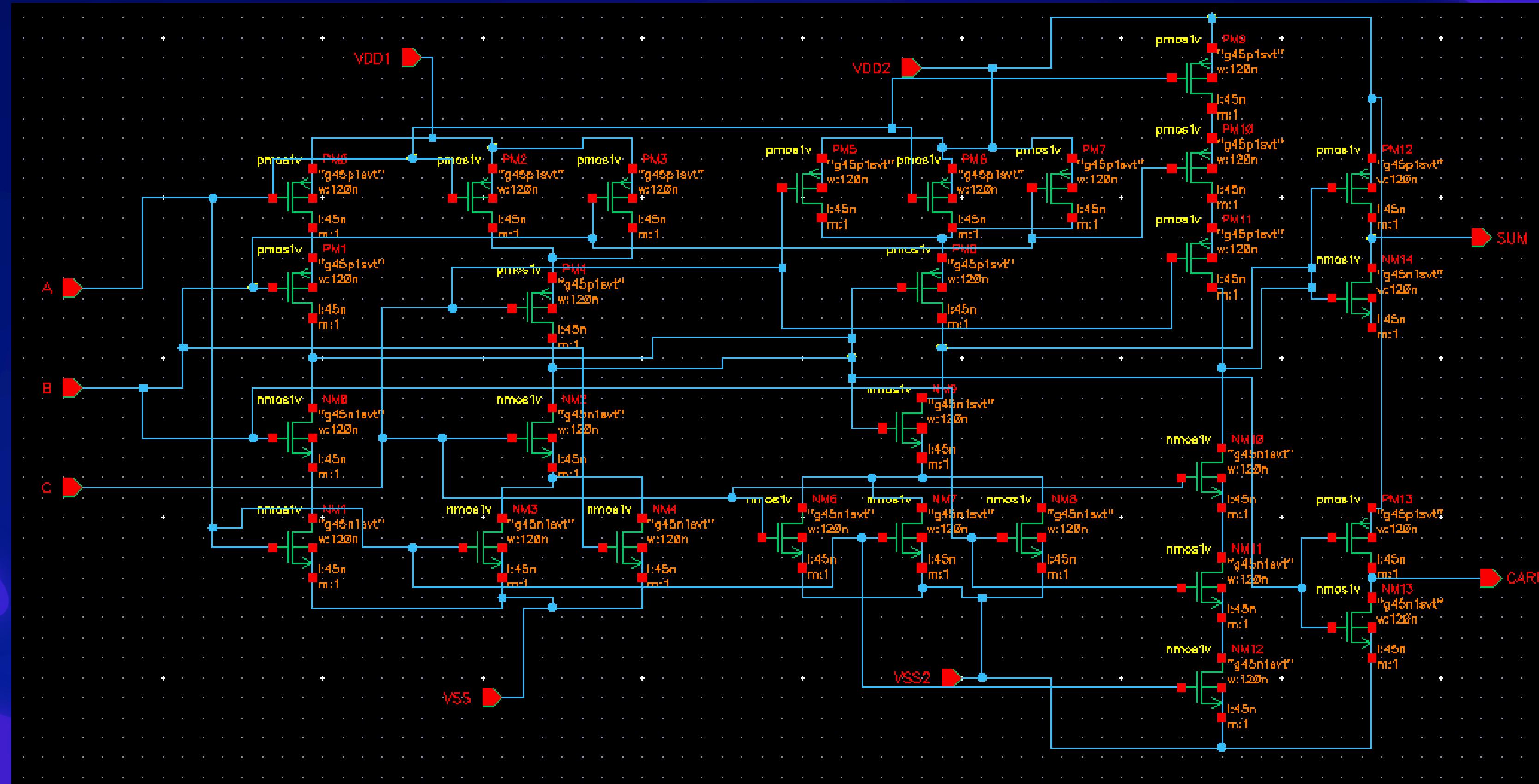
ALU CIRCUIT DIAGRAM NEW DESIGN



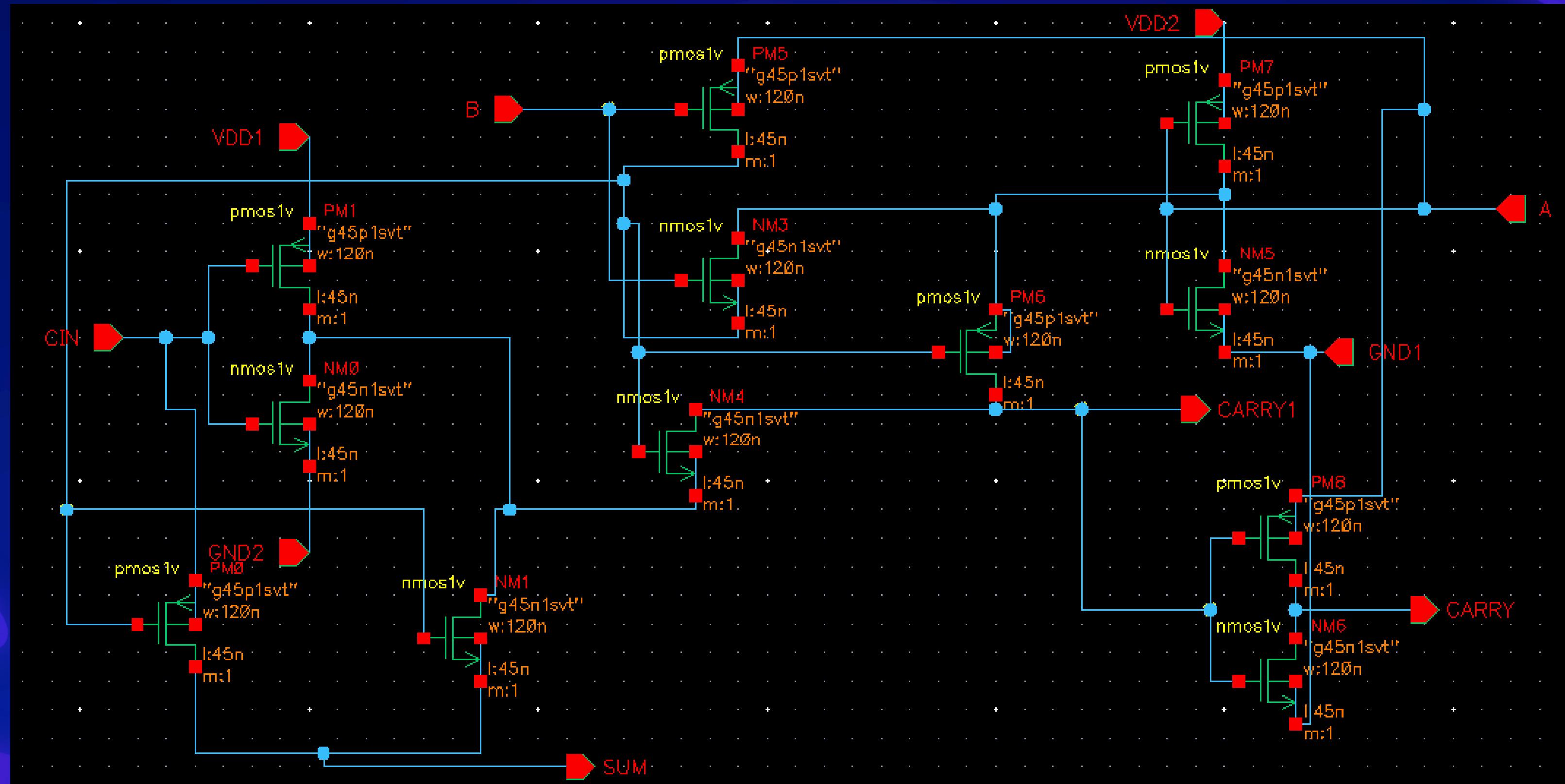
Floor Plan:



CMOS CONVENTIONAL ADDER



ADDER USING PASS TRANSISTOR



RESULTS OF CADENCE CIRCUITS



CADENCE RESULTS SCREENSHT

Virtuoso (R) Visualization & Analysis XL Tab			
File	Edit	View	Tools
delayMeasure(i"/I0/V1/PLUS" ?resu... X			
Expression	Value	Expression	Value
1 delayMeasure(i... -1.839E-3		average(clipX(v"/... 3.497	

Conventional Method

Virtuoso (R) Visualization & Analysis XL Tab			
File	Edit	View	Tools
average(v"/OUT" ?result "tran") de... X			
Expression	Value	Expression	Value
average(v"/OUT... 4.917		delayMeasure(v... 491.2E-6	

Virtuoso (R) Visualization & Analysis XL Tab			
File	Edit	View	Tools
average(v"/out" ?result "tran") X			
Expression	Value	Expression	Value
1 average(v"/out"... 1.939			

PTL Design Method

Virtuoso (R) Visualization & Analysis XL Tab			
File	Edit	View	Tools
average(v"/VOUT" ?result "tran") de... X			
Expression	Value	Expression	Value
1 average(v"/VOU... 2.502		delayMeasure(v... -979.8E-6	

POWER ANALYSIS OF CIRCUITS

CIRCUIT NAME	POWER OF NORMAL CIRCUIT (in mW)	POWER OF LOW POWER CIRCUITS (in mW)
ALU	4.89 mW	2.5 mW
MULTIPLEXER	3.497 mW	1.99 mW

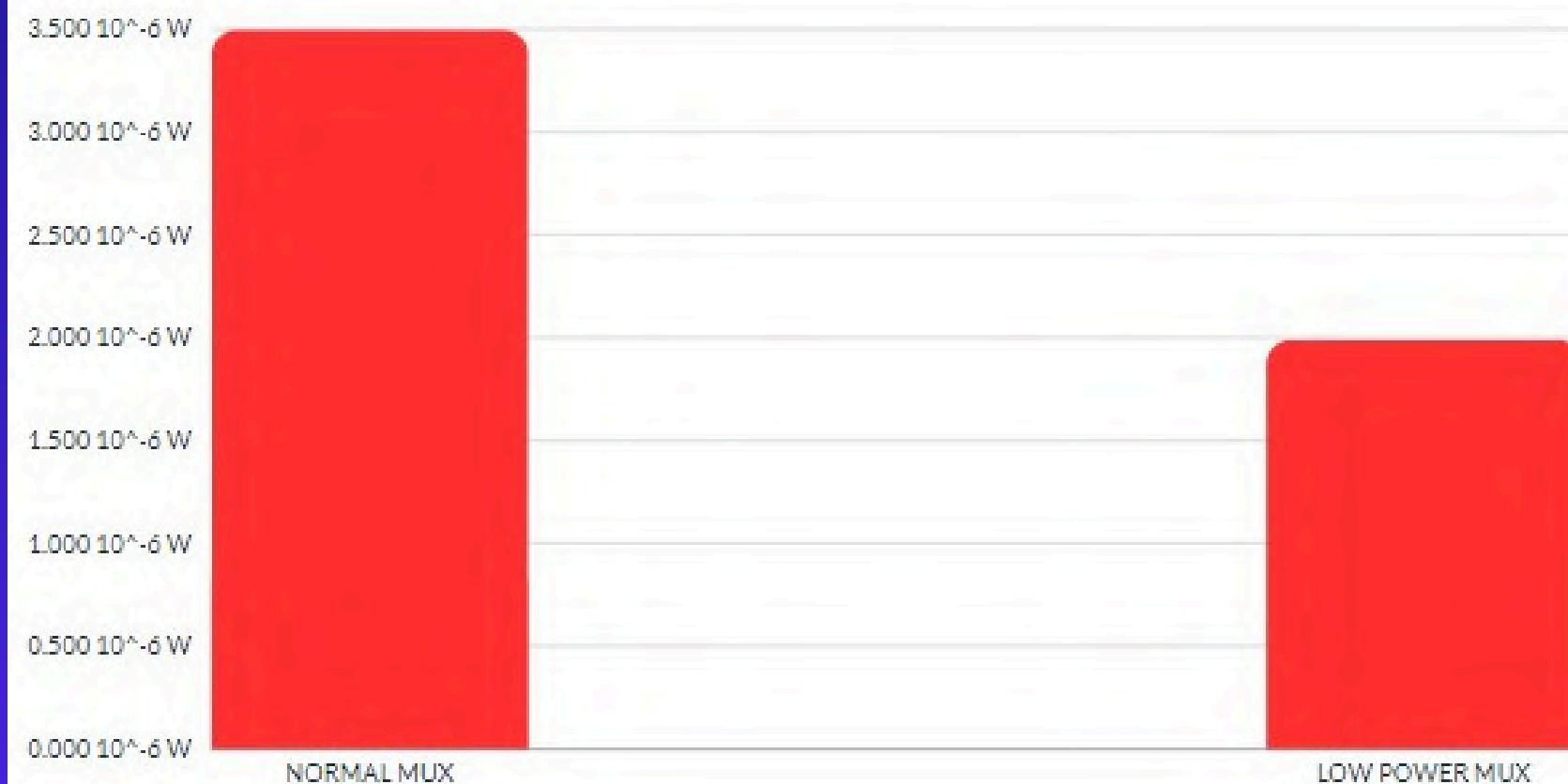
DELAY ANALYSIS OF CIRCUITS

CIRCUIT NAME	DELAY OF NORMAL CIRCUIT (in Sec)	DELAY OF LOW POWER CIRCUITS (in Sec)
ALU	6 Sec	799×10^{-3} Sec
MULTIPLEXER	1.839×10^{-3} Sec	132.5×10^{-6} Sec

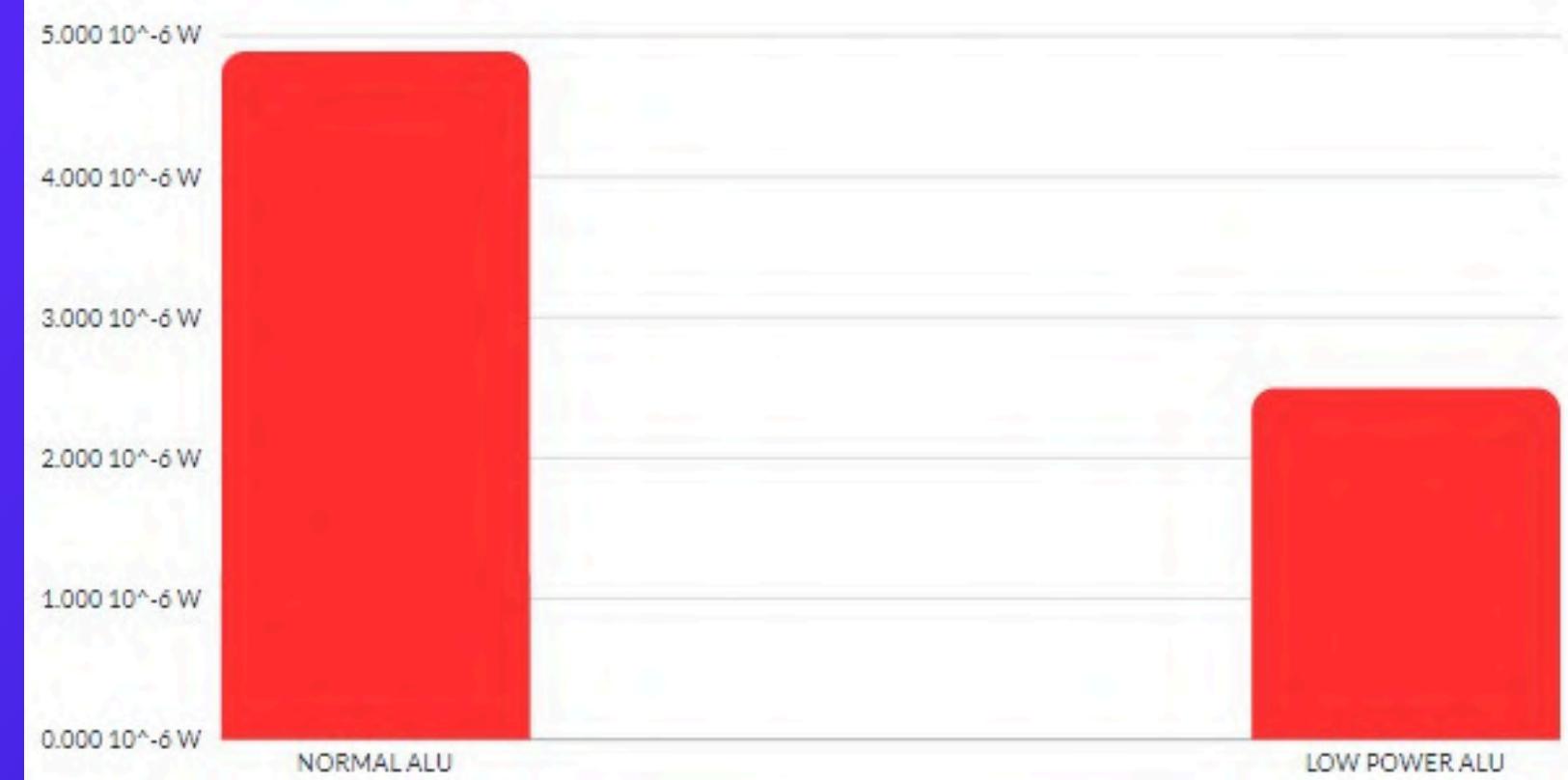
OBTAINED GRAPHS

GRAPHS ANALYSIS

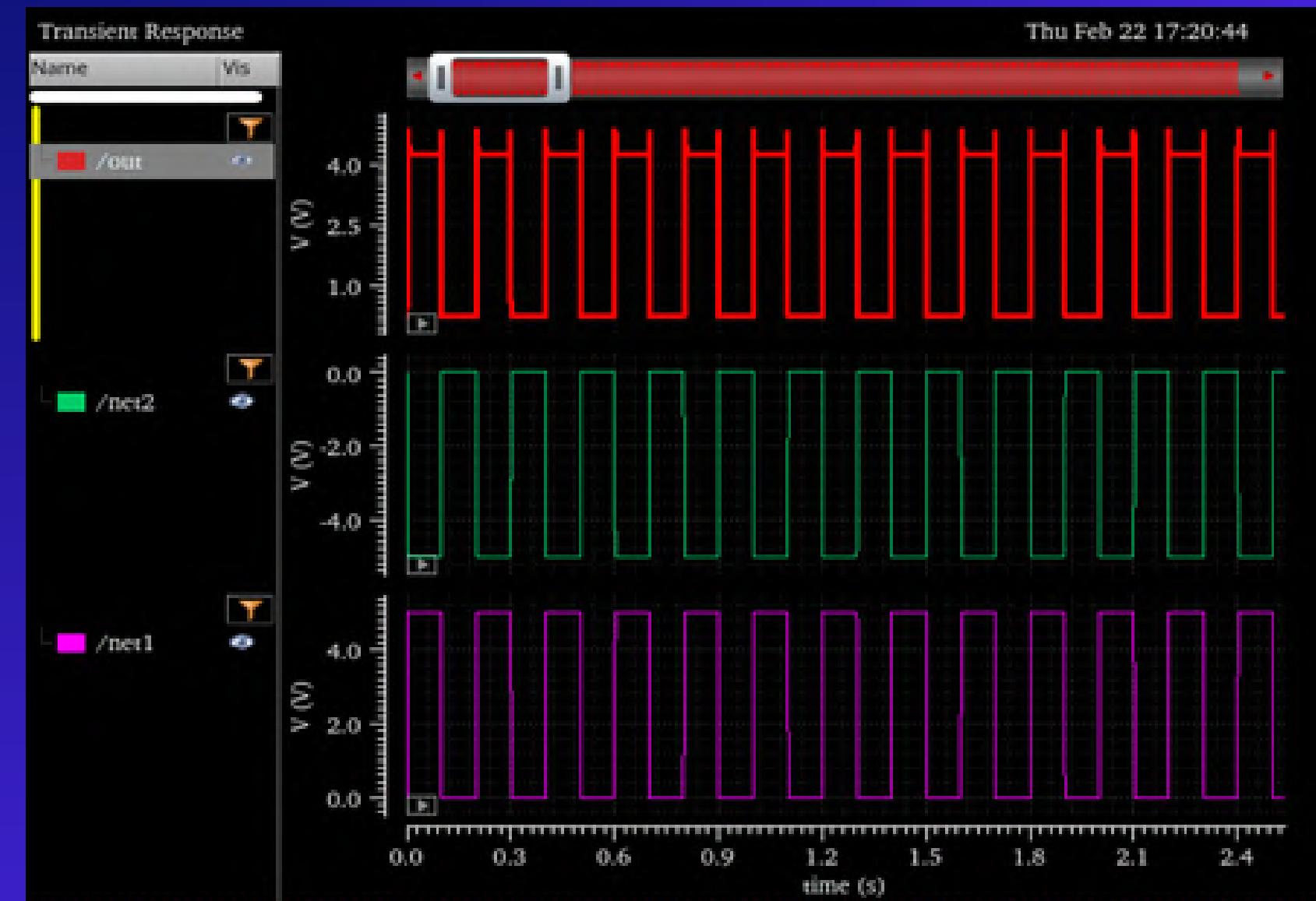
POWER ANALYSIS OF MUX



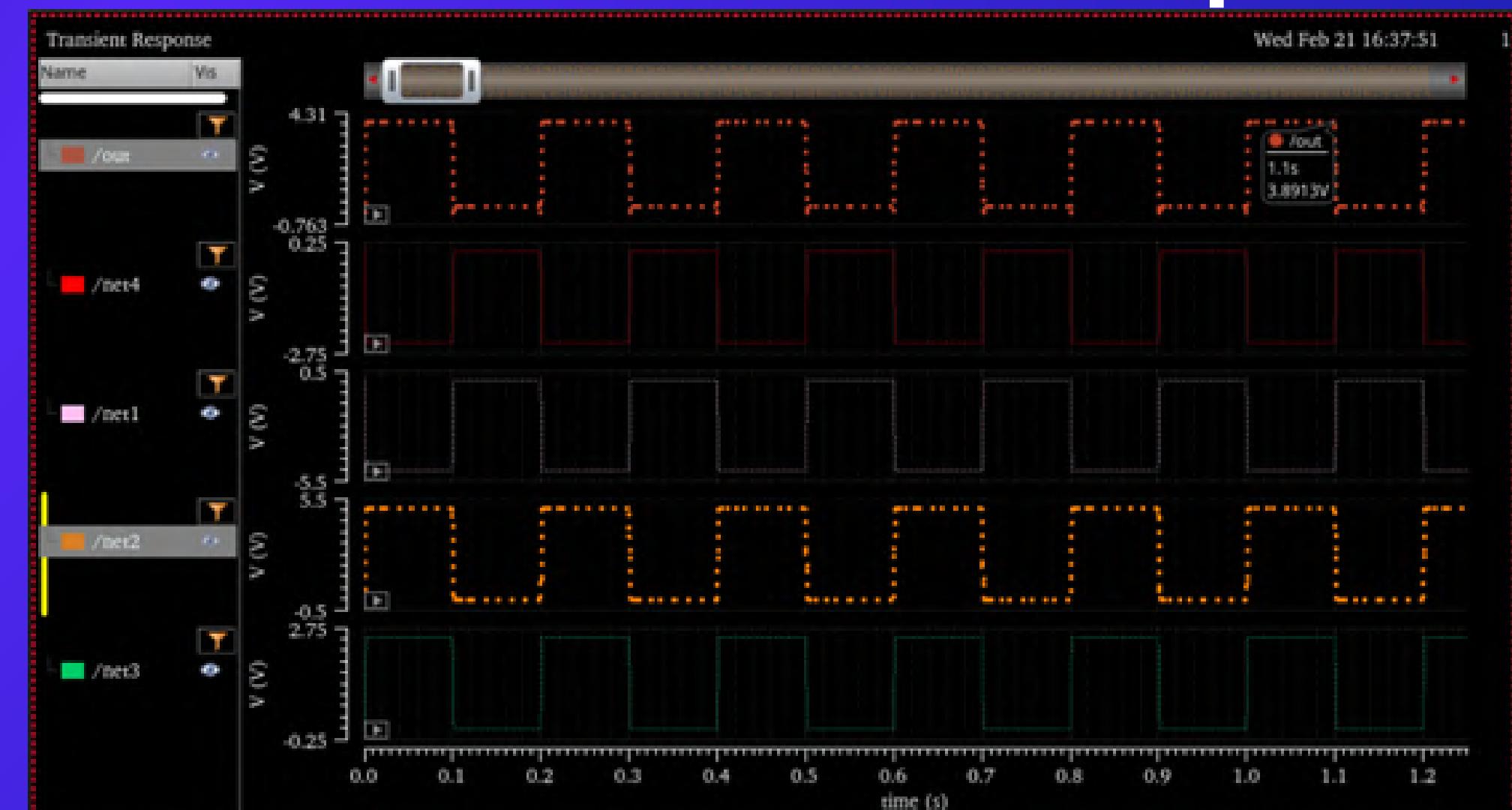
POWER ANALYSIS OF ALU



GRAPHS

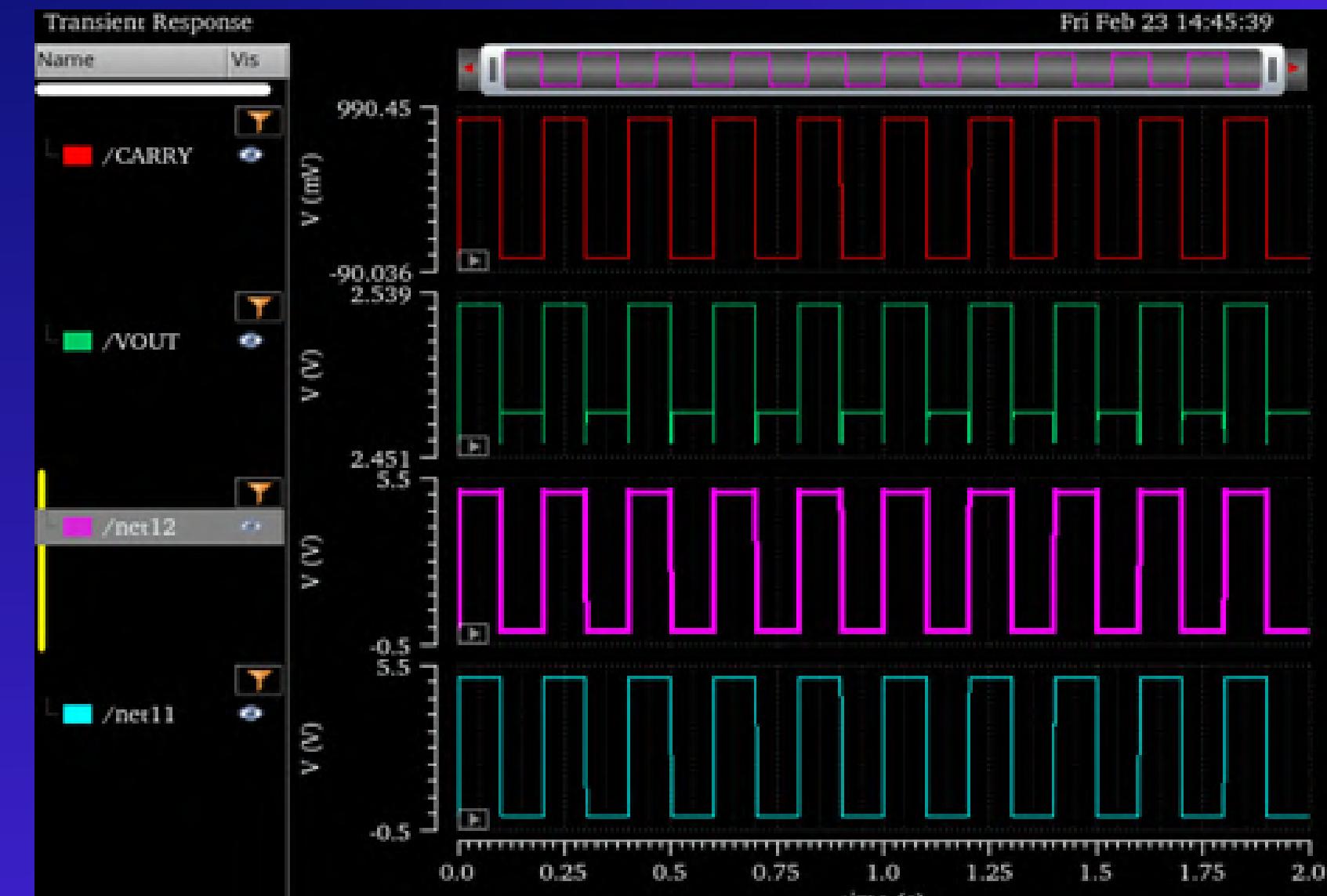


Conventional Multiplexer

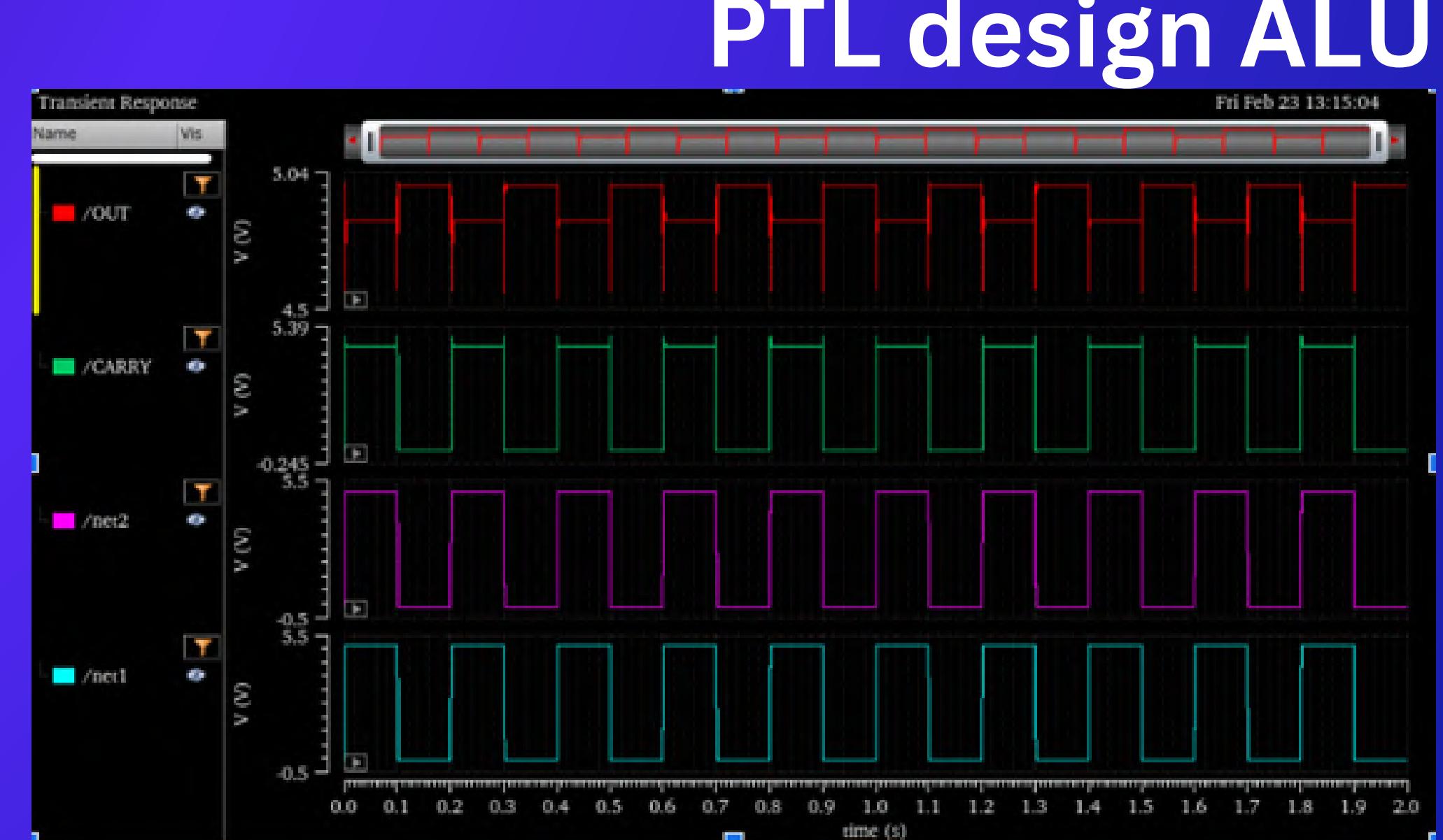


PTL Multiplexer

GRAPHS

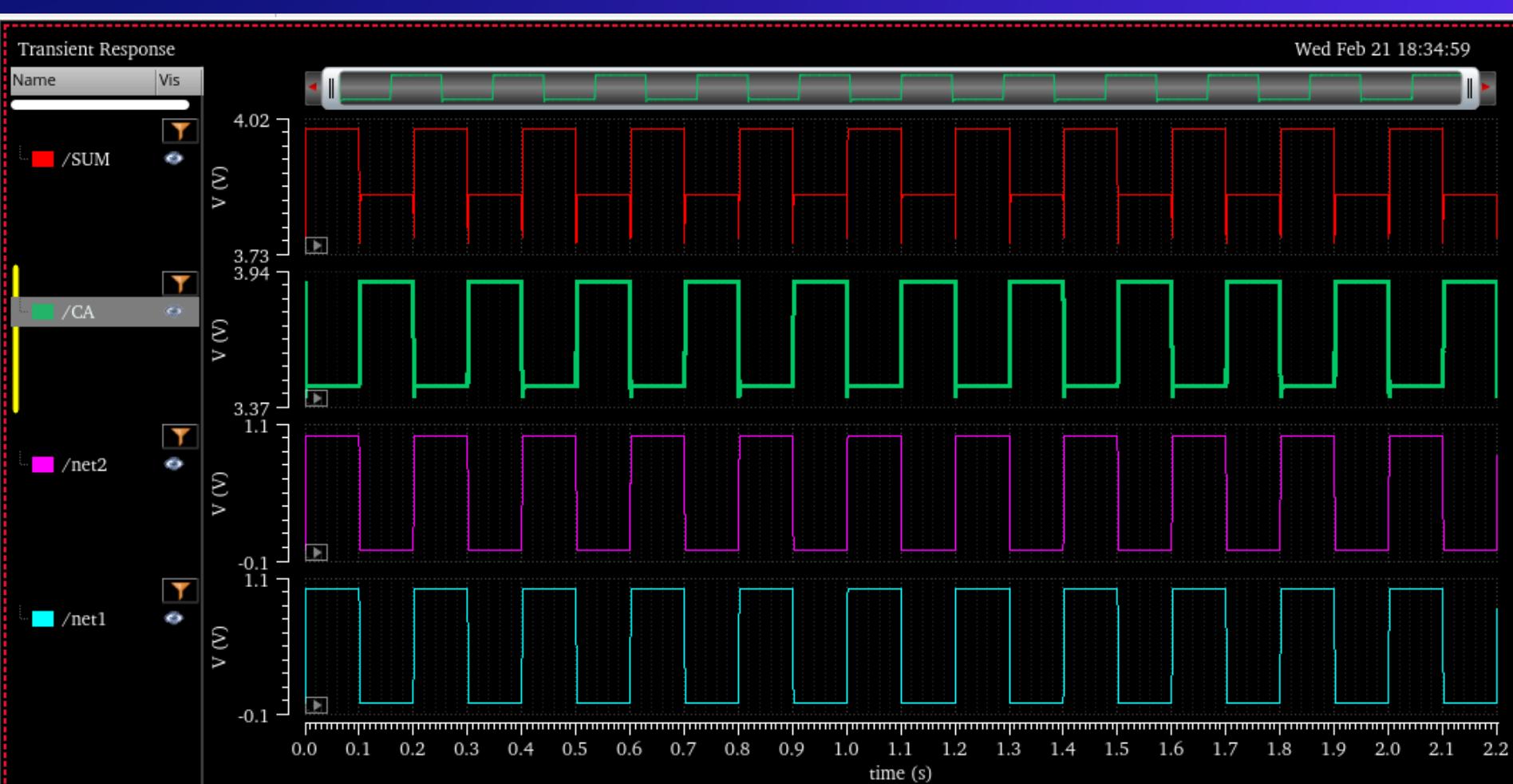


Conventional ALU



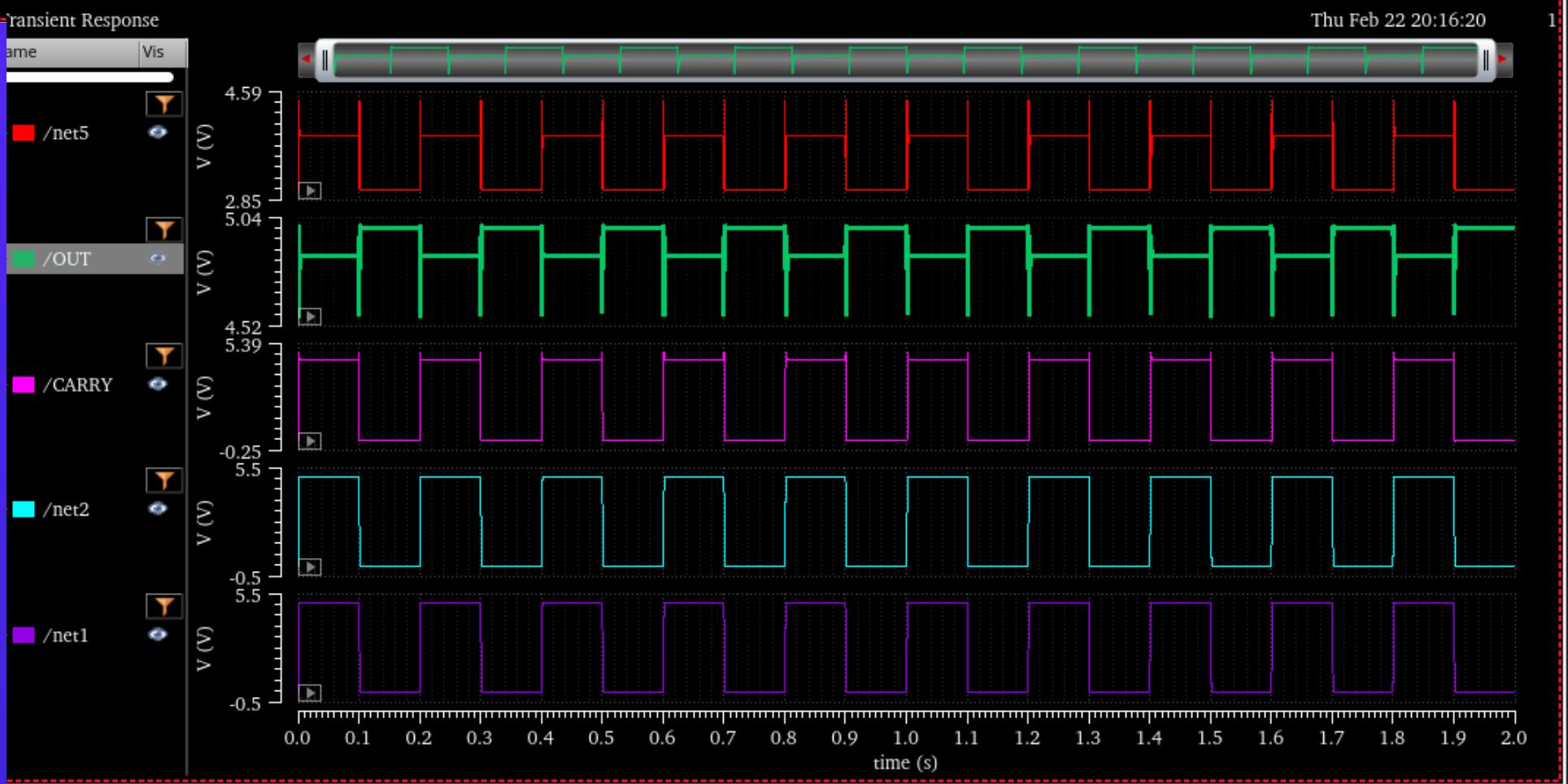
PTL design ALU

GRAPHS



Conventional Adder

PTL Logic Adder





SUMMARY

The project outlines the endeavor to develop sustainable low-power AI accelerators, focusing on CMOS and Pass Transistor Logic (PTL) ALU designs using Cadence tools. The work of the project's architecture, including requirements analysis, architecture design, simulation, and optimization has been done keenly . Notably, our design methodologies prioritize energy efficiency while maintaining optimal performance. Results demonstrate the superiority of the PTL ALU in power efficiency, underscoring its potential for eco-friendly AI hardware. This stands as a testament to our commitment to advancing sustainable AI technologies through innovative architectural approaches.

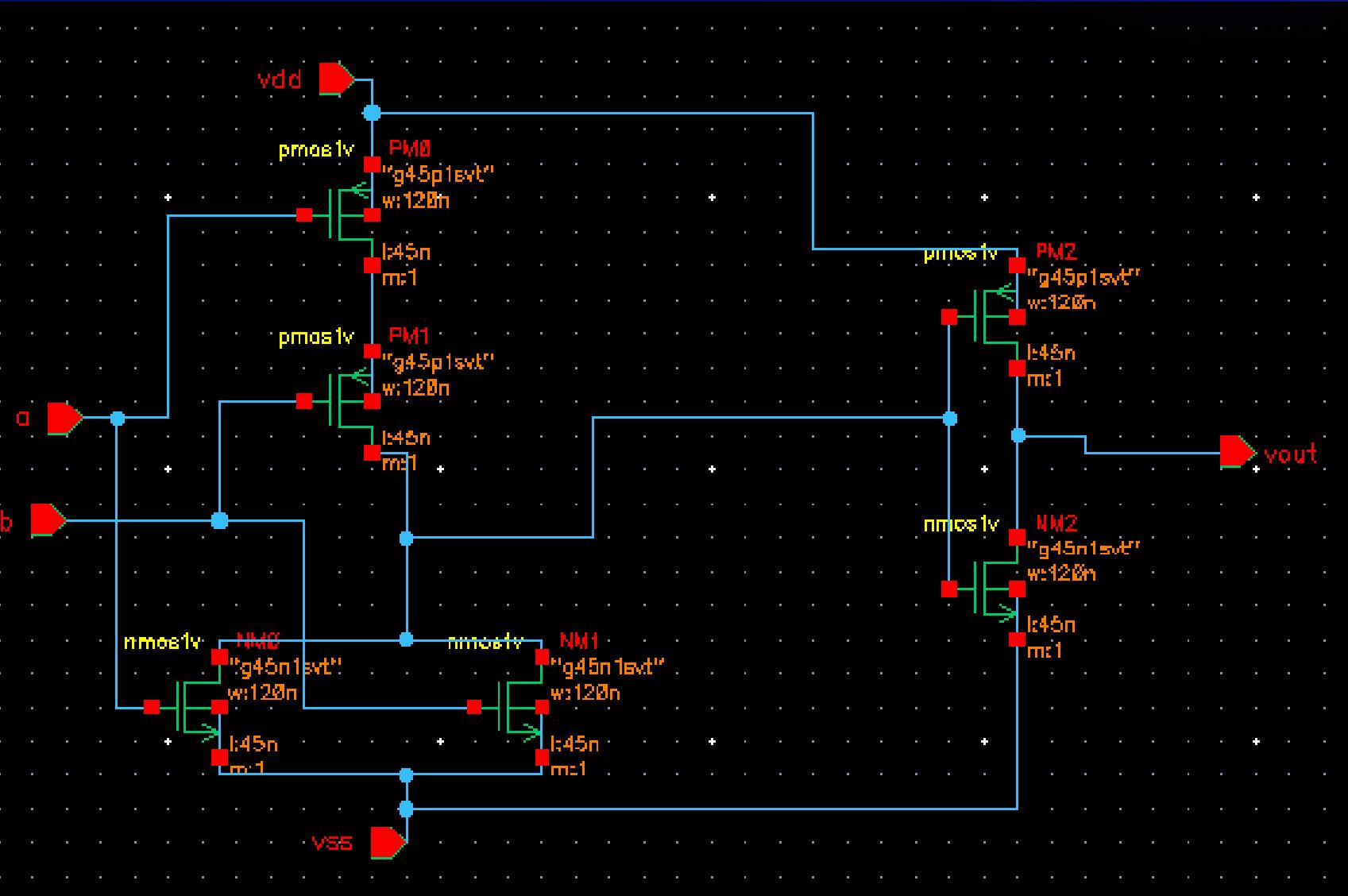


RESULT

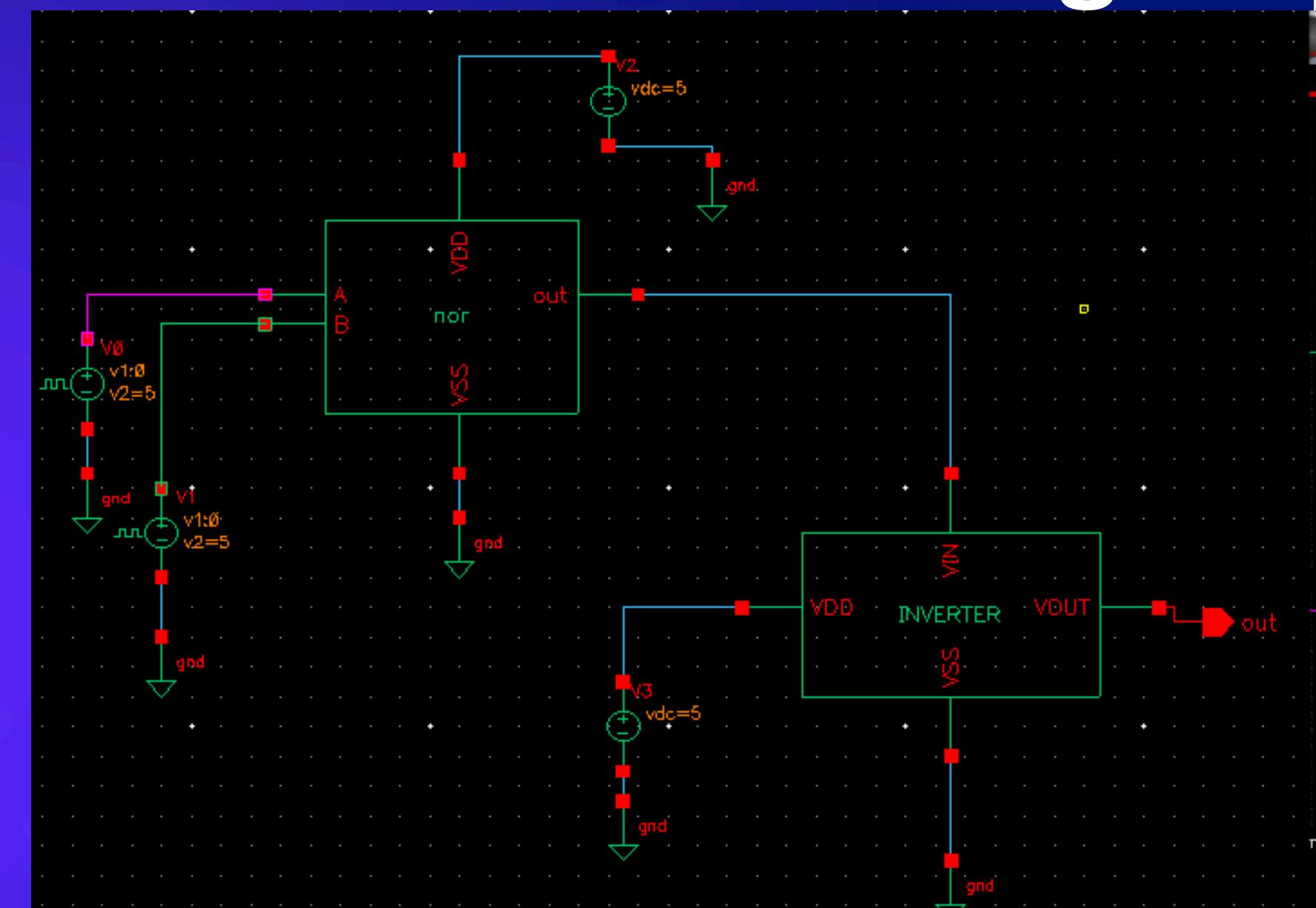
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The results of our project on sustainable low-power AI accelerator design and optimization using Cadence are highly promising. Through meticulous design and analysis, we successfully developed two distinct ALU designs: one based on complementary CMOS transistors and the other utilizing pass transistor logic.

GATE LOGICS

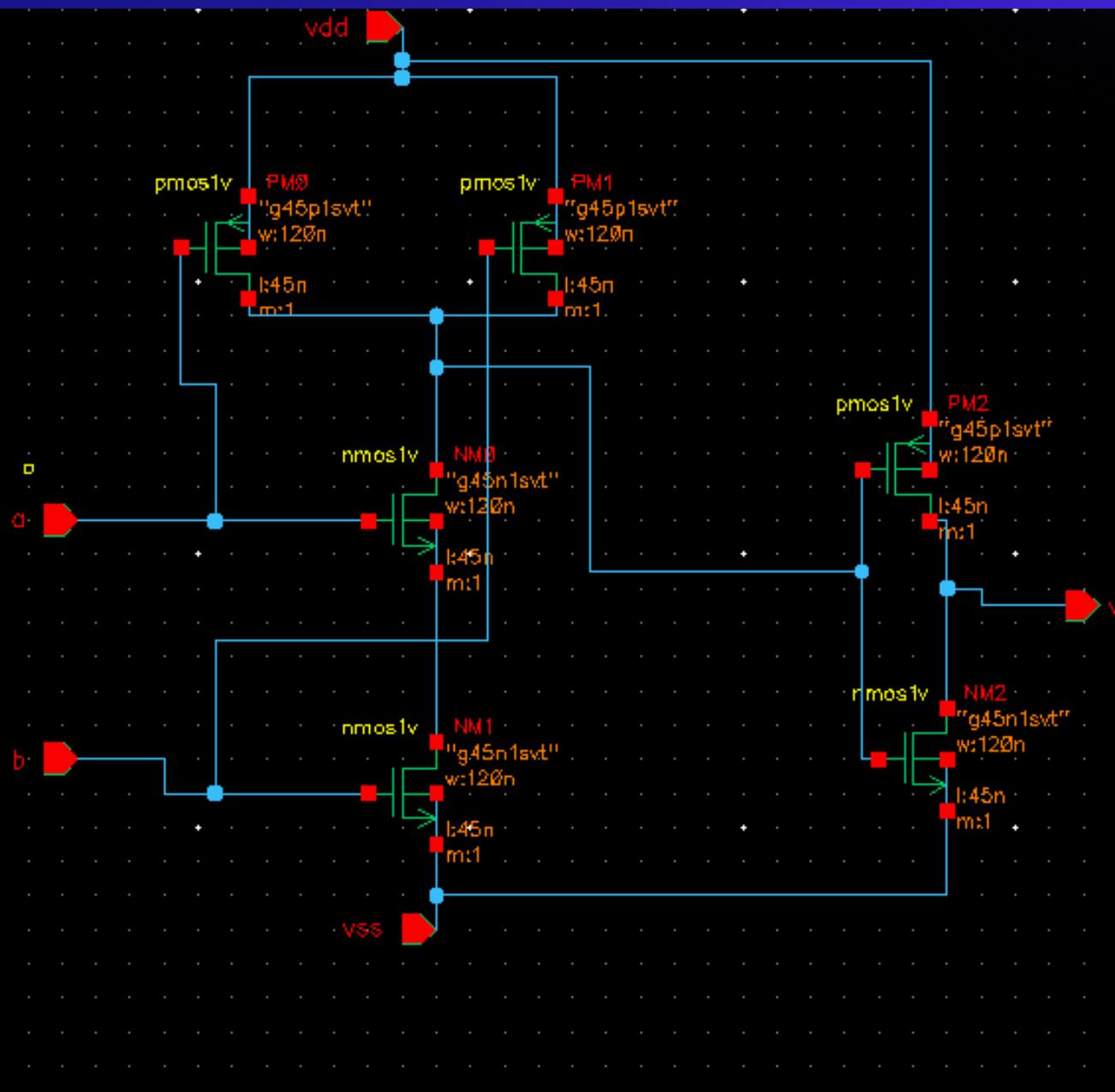


Conventional OR gate



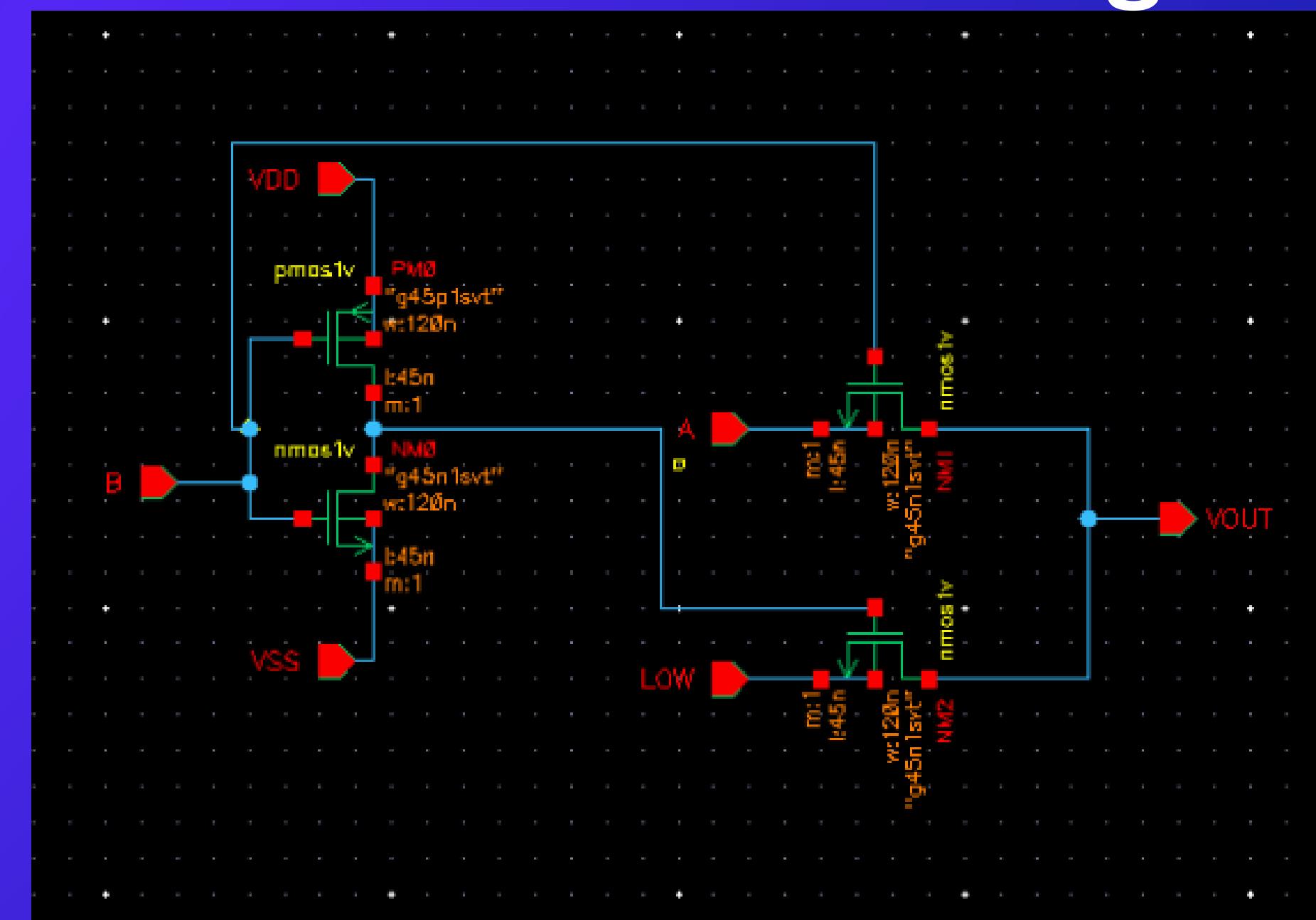
PTL OR gate

GATE LOGICS



Conventional AND gate

PTL AND gate



THANK YOU!

