PSG INSTITUTE OF TECHNOLOGY AND APPLIED RESEARCH
NEELAMBUR ,COIMBATORE

FINAL YEAR PROJECT REVIEW - 3

DESIGN AND IMPLEMENTATION OF EFFICIENT PROCESSING ELEMENT ARRAY FOR CNN ACCELERATOR

Review Date: 10-05-2025

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PROBLEM STATEMENT

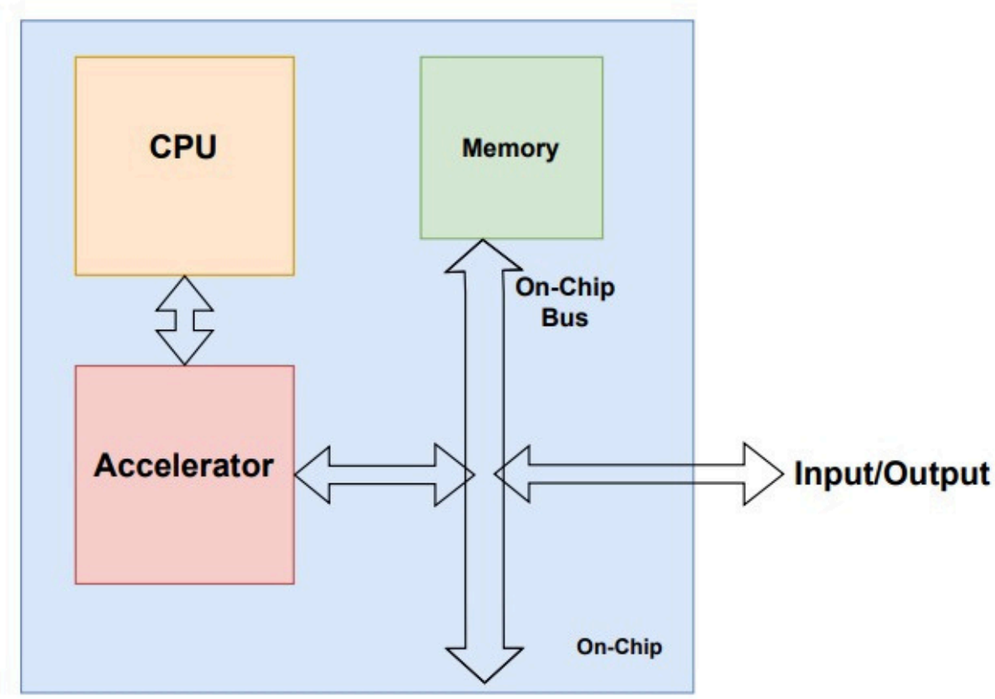
The project aims to address the computational complexity and power consuming challenges of deploying CNN accelerator on resource-constrained devices by optimizing their performance using a Processing Element (PE) Array architecture.

OBJECTIVES

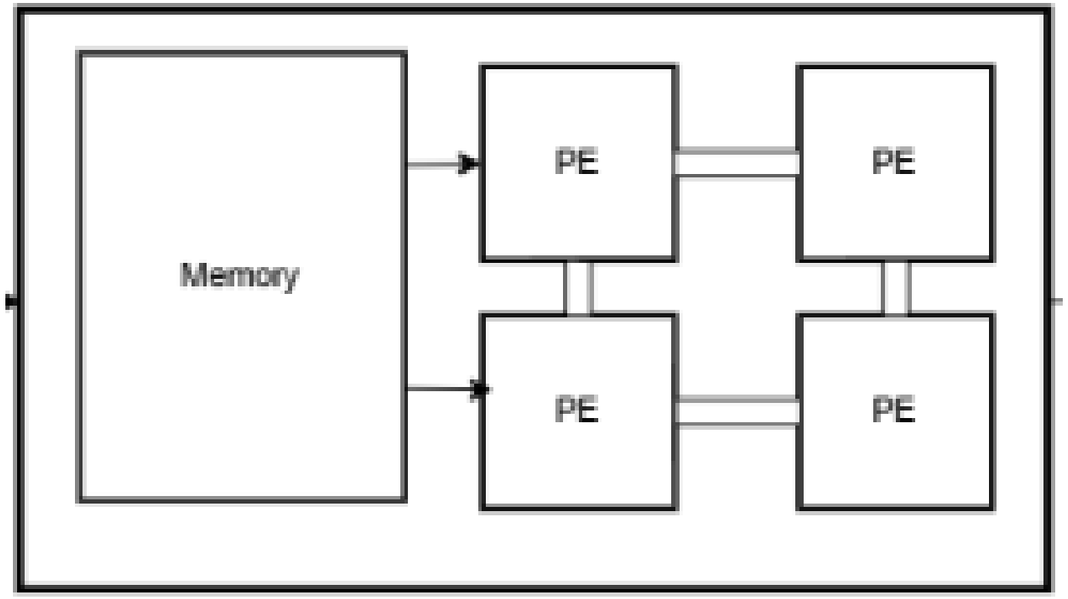
- To optimize data movement and computation.
- To minimize power consumption of processing element.
- To reduce the area of the PE array.

PROPOSED WORK

CNN Accelerator Chip

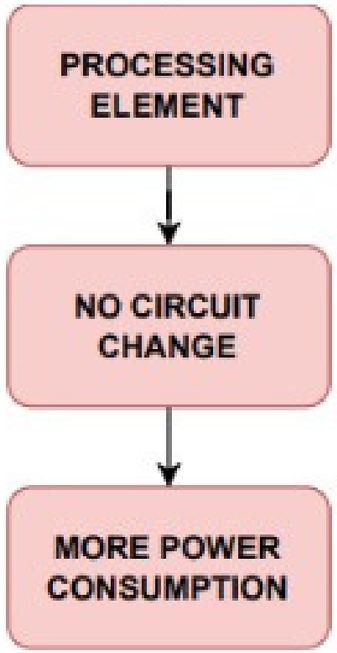


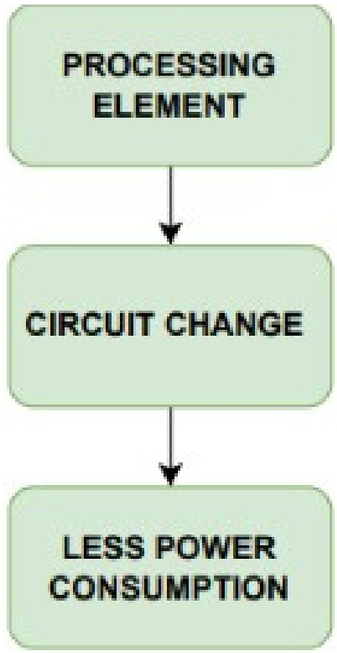
CNN Processing element array



PROPOSED WORK

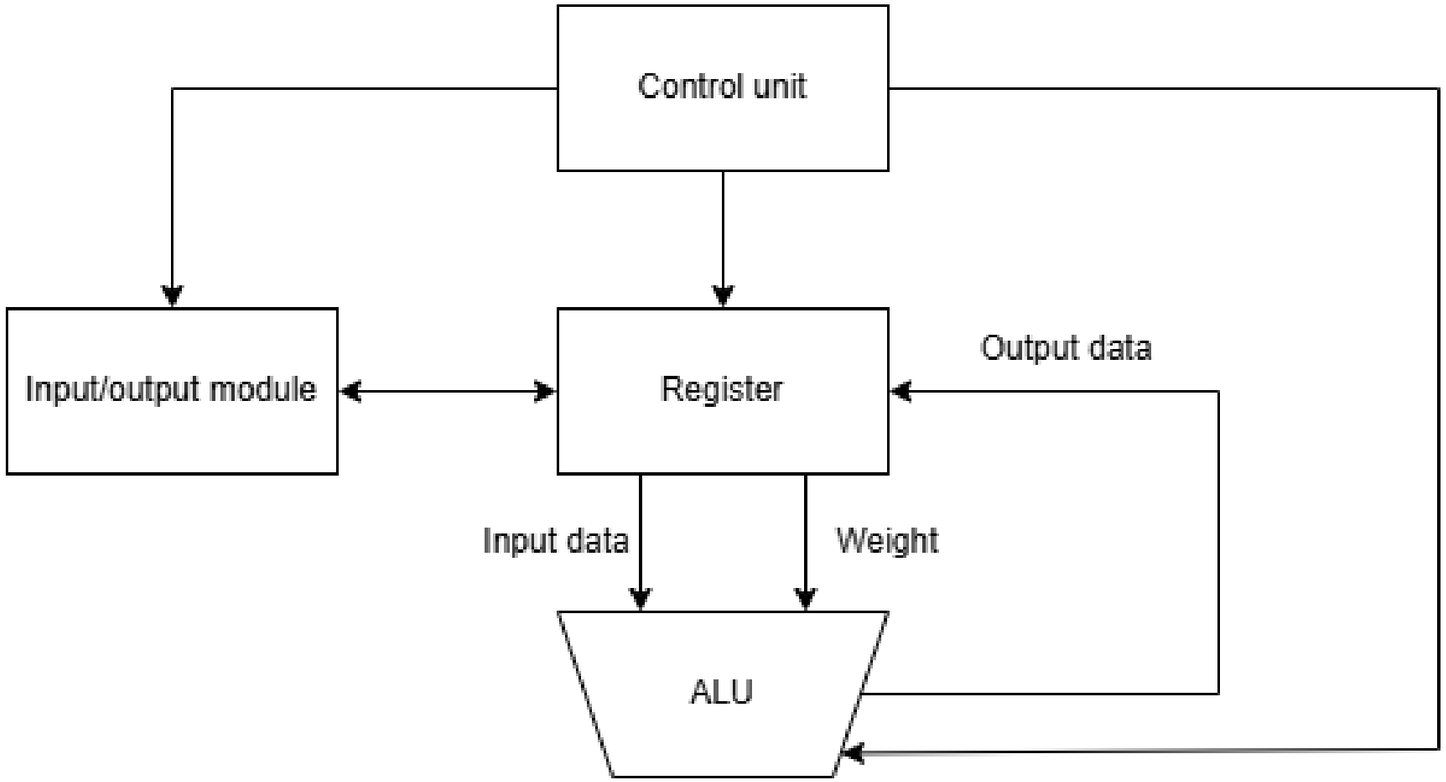
Idea Flow





PROPOSED WORK

Block diagram of a single processing element



ALU Operations :

's' input determines the operation performed by the ALU

- s = 3'b000 → Addition (In Hybrid Adder)
- s = 3'b001 → Multiplication (Dadda Multiplier)
- s = 3'b010 → Bitwise AND
- s = 3'b011 → Bitwise OR
- s = 3'b100 → Bitwise NOT of A
- s = 3'b101 → Bitwise NOT of B
- Default case → No operation → Output remains unchanged (C <= C).

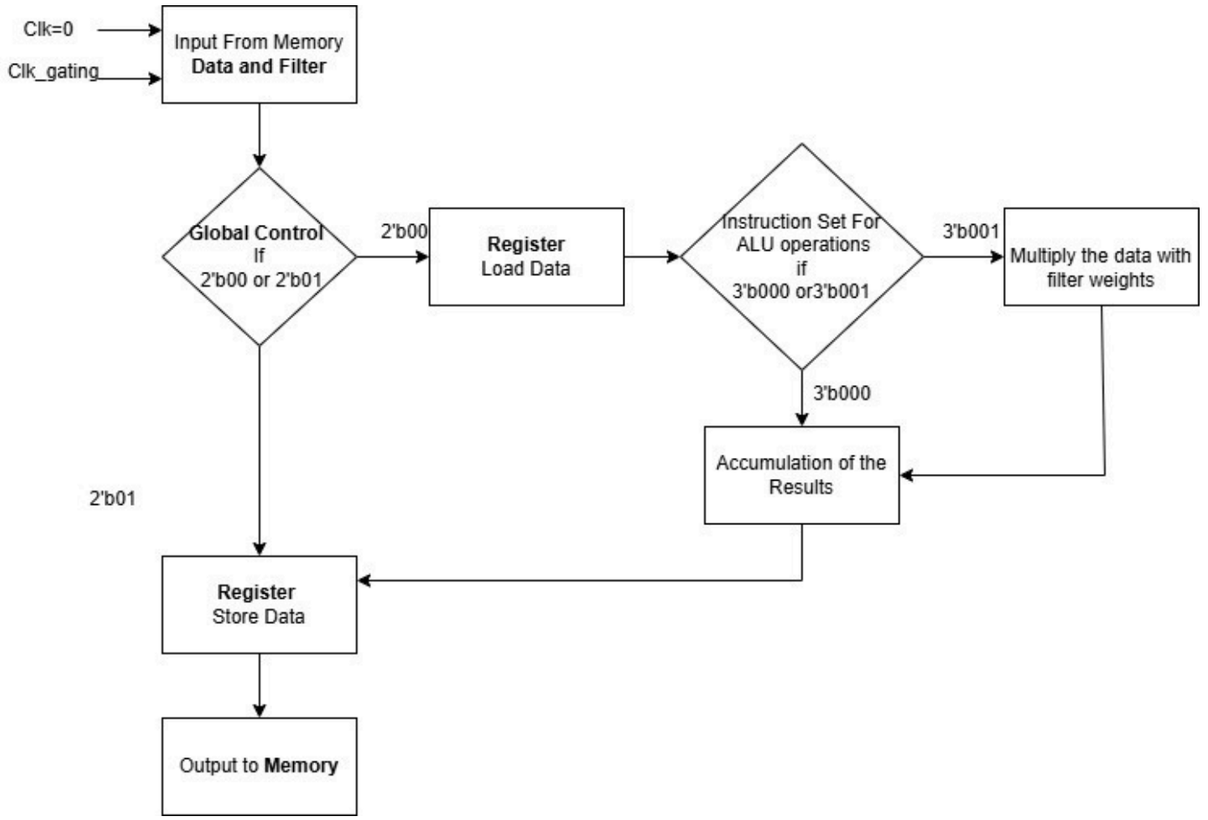
Register Operations :

'cui' signal controls how data flows in and out of Register

- cui = 2'b00 → Load input data
- cui = 2'b01 → Store input data
- cui= 2'b10 → Load output data
- cui= 2'b11 → Store output data

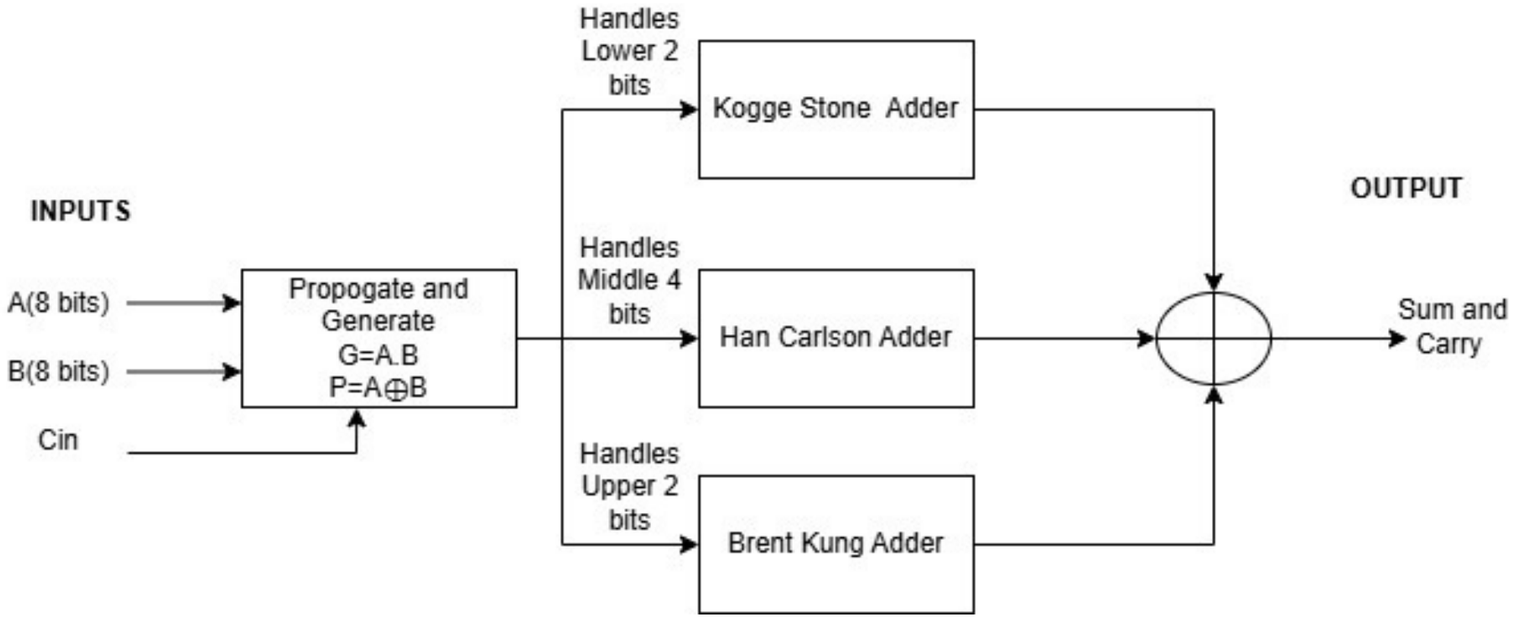
PROPOSED WORK

Convolution Operation Flow in PE Array



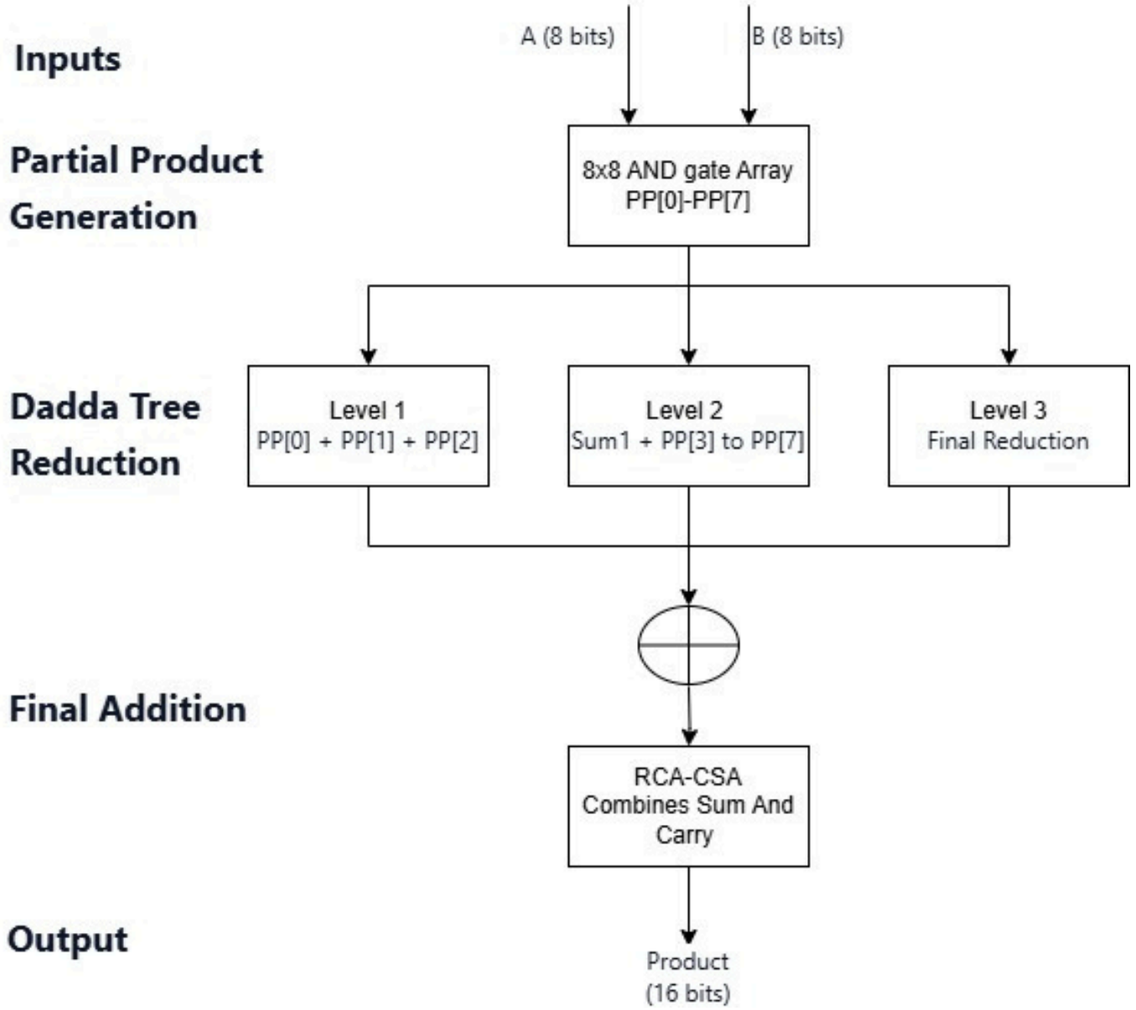
POWER MINIMIZATION METHODS

Block diagram of Hybrid Adder



POWER MINIMIZATION METHODS

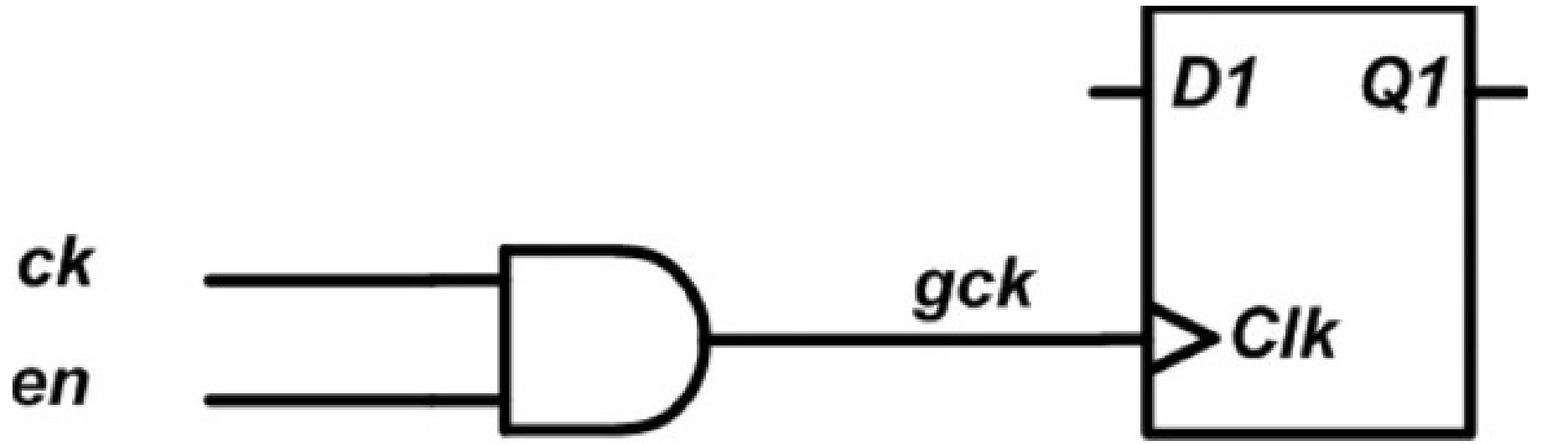
Block diagram of multiplier



- A Dadda multiplier is a hardware circuit that multiplies binary numbers using adders.
- The Dadda multiplier forms a partial product matrix using AND gates.
- Dadda multipliers are known for their efficiency, requiring fewer additions and logical operations compared to other multipliers, leading to lower power dissipation.

POWER MINIMIZATION METHODS

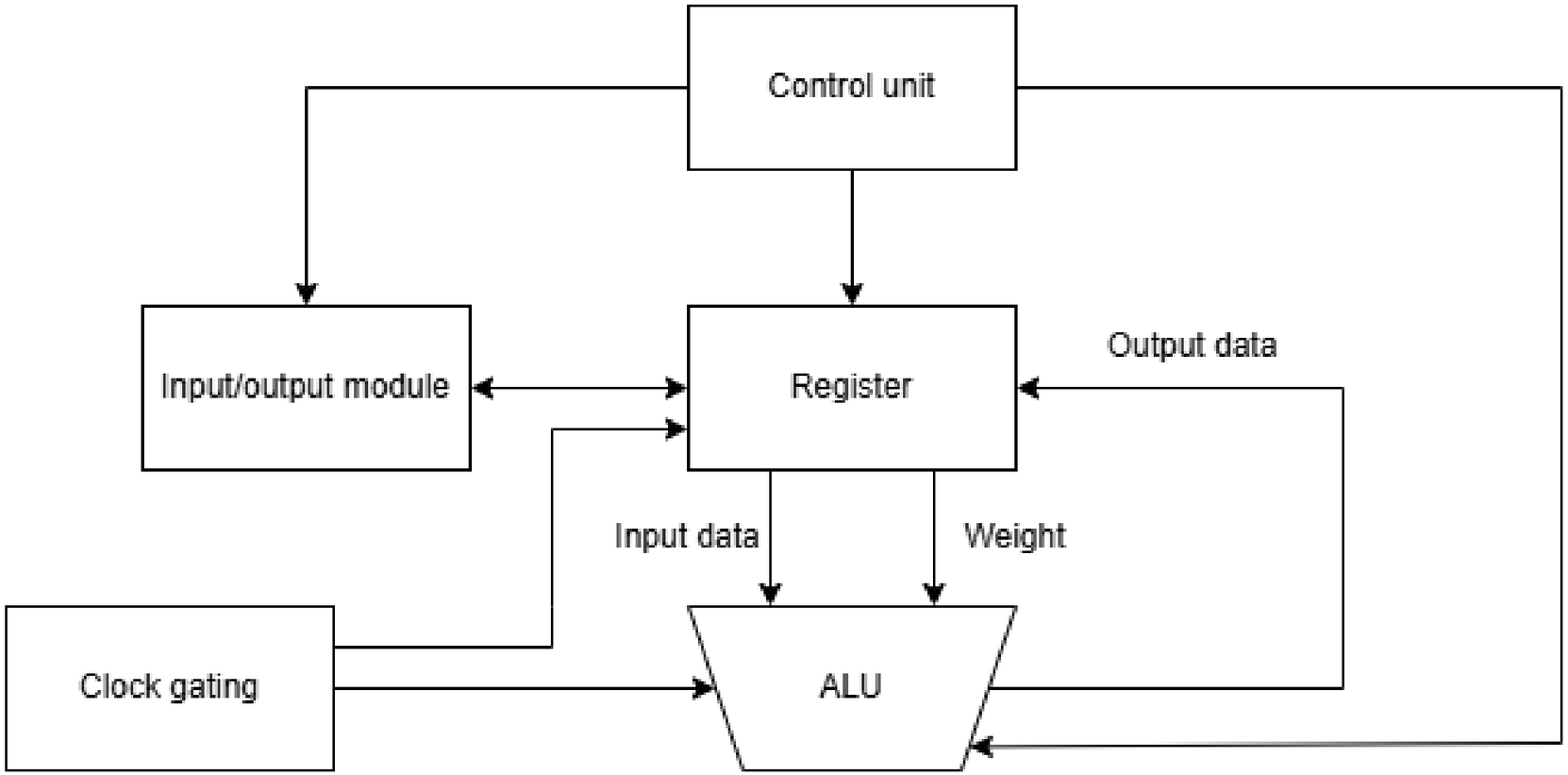
Clock gating- Minimizes the power



Clock gating is a technique that reduces power consumption by temporarily disabling the clock signal for parts of a circuit that aren't in use. It's a popular power management technique used in many synchronous circuits.

POWER MINIMIZATION METHODS

Clock gating- Single Processing Element



TOOLS USED

Xilinx Vivado:

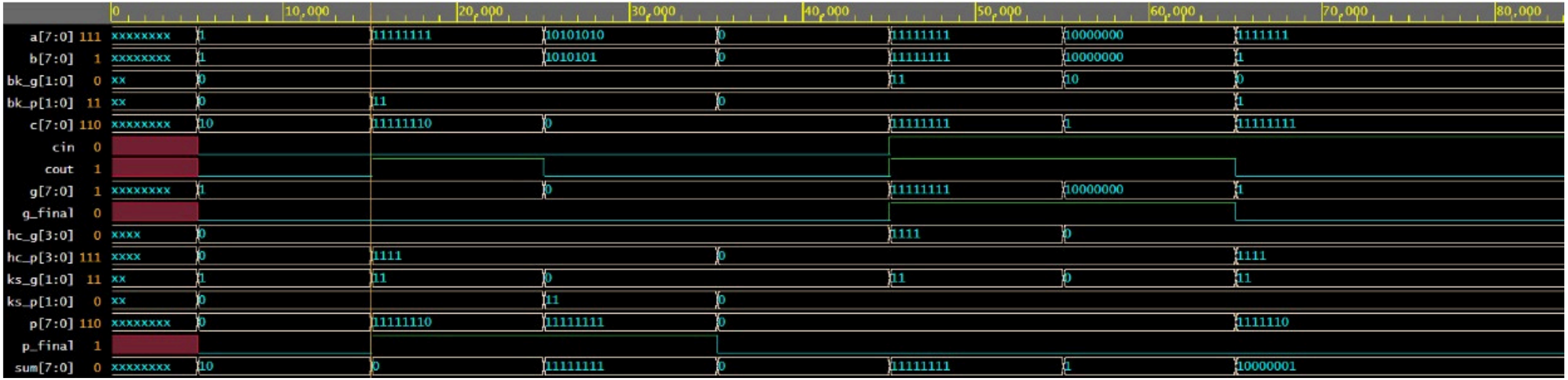
- Simulation
- Synthesis
- FPGA implementation

Cadence:

- Simulation
- Synthesis
- Power, area and timing report

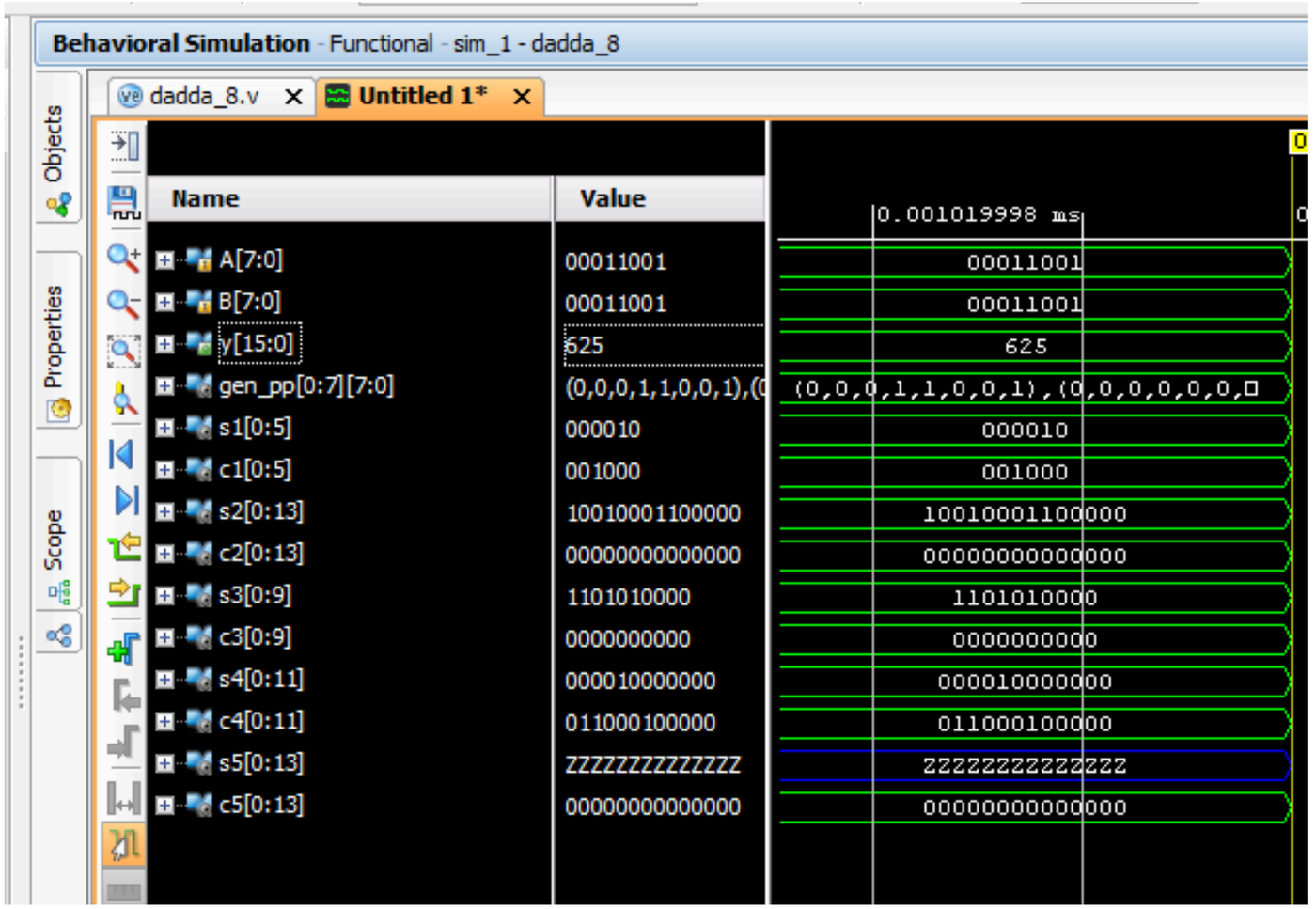
COMPLETED WORK WITH RESULTS

Simulation Output of Hybrid adder



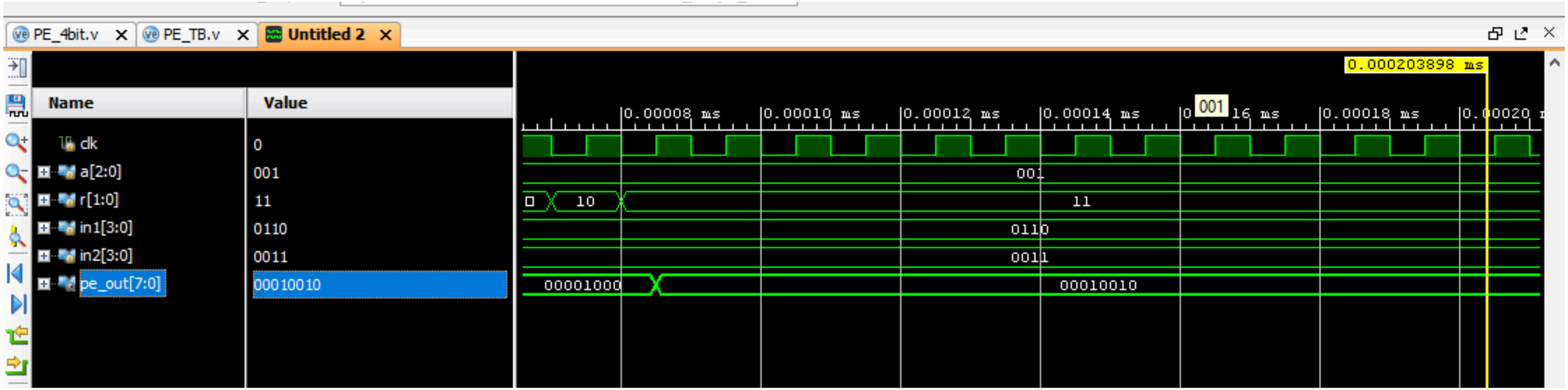
COMPLETED WORK WITH RESULTS

Simulation Output of Dadda Multiplier



COMPLETED WORK WITH RESULTS

Simulation Output of Processing element

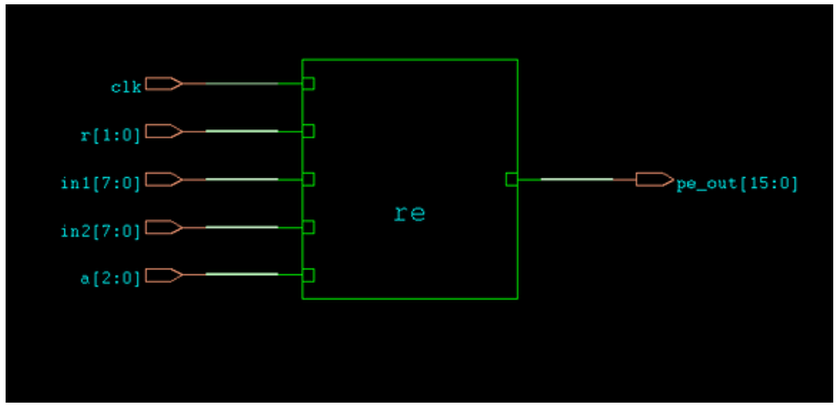


In the above simulation we have performed Addition of two 4-bit inputs and Multiplication of two 4-bit inputs.The operations are:

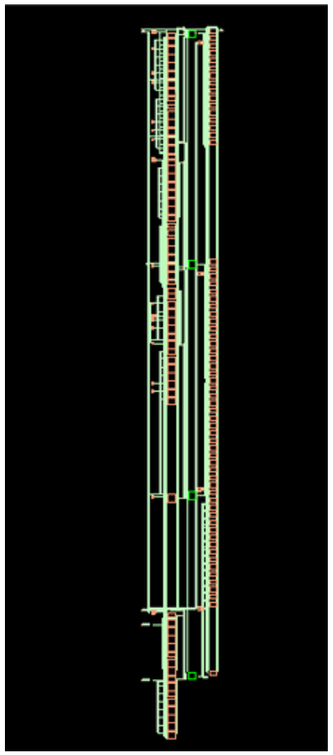
- Addition: in1=5 and in2=3 ----> pe_out=5+3=8
- Multiplication: in1=6 and in2=3 ----> pe_out=6*3=18

COMPLETED WORK WITH RESULTS

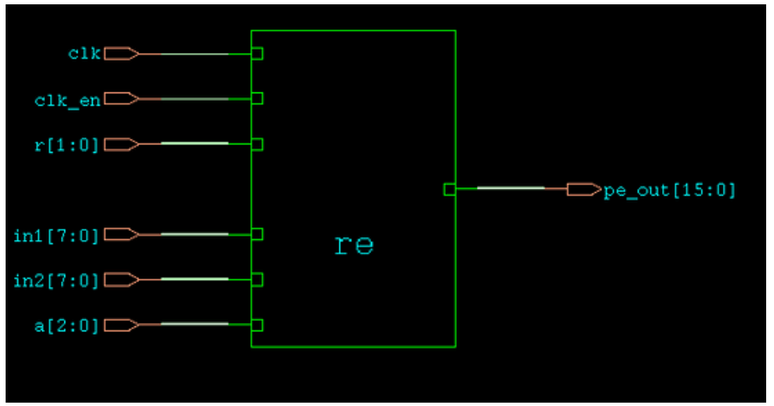
RTL Schematics



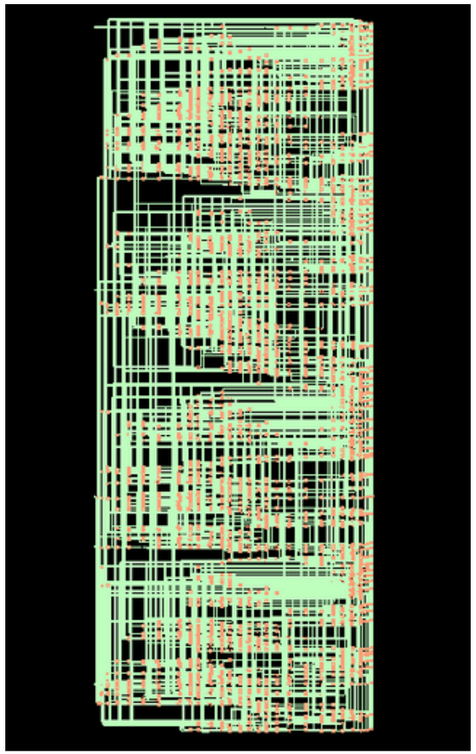
Normal Processing Element



Normal PE Array



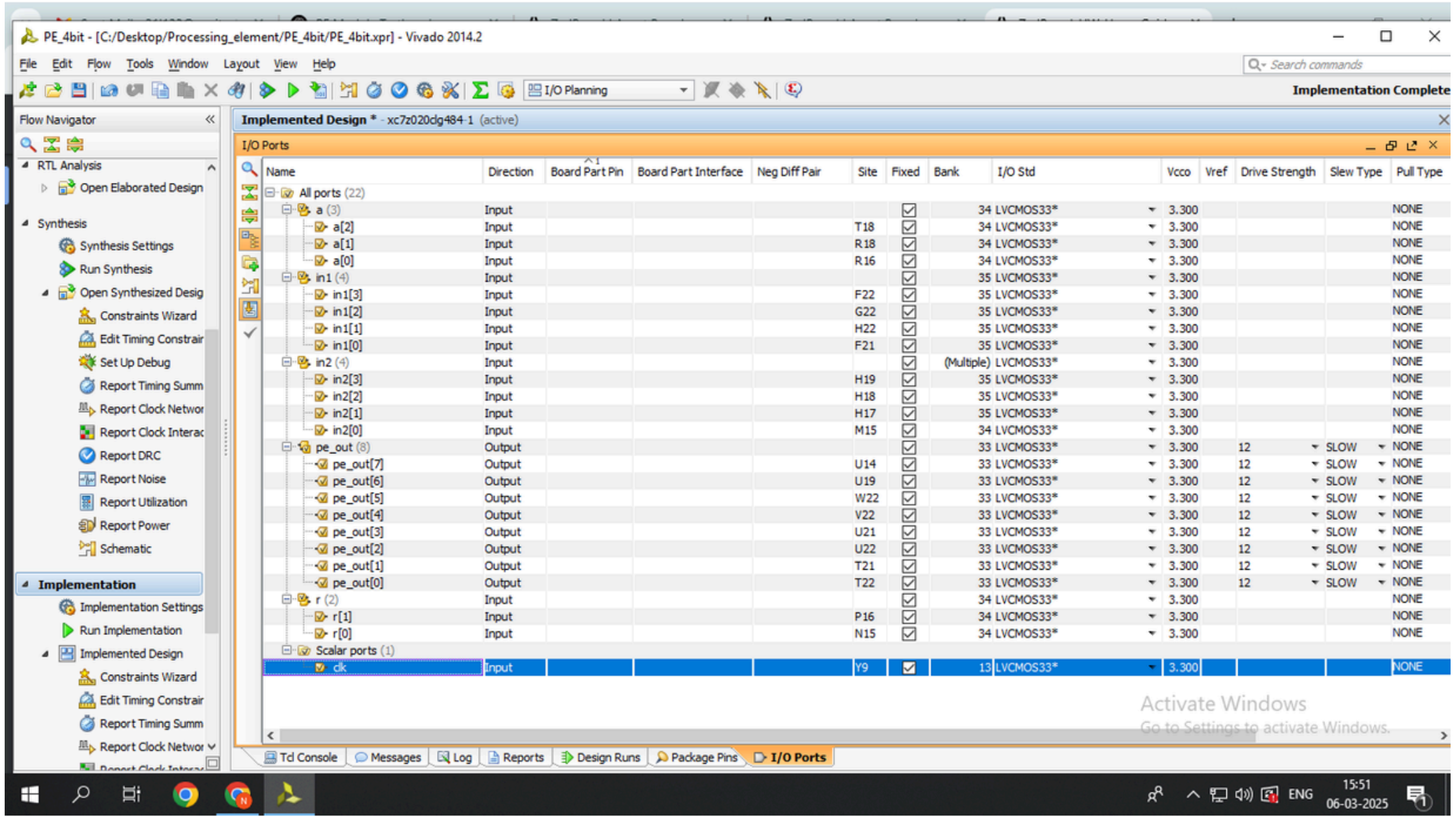
Low Power Processing Element



Low Power PE Array

COMPLETED WORK WITH RESULTS

FPGA Pin assignment diagram



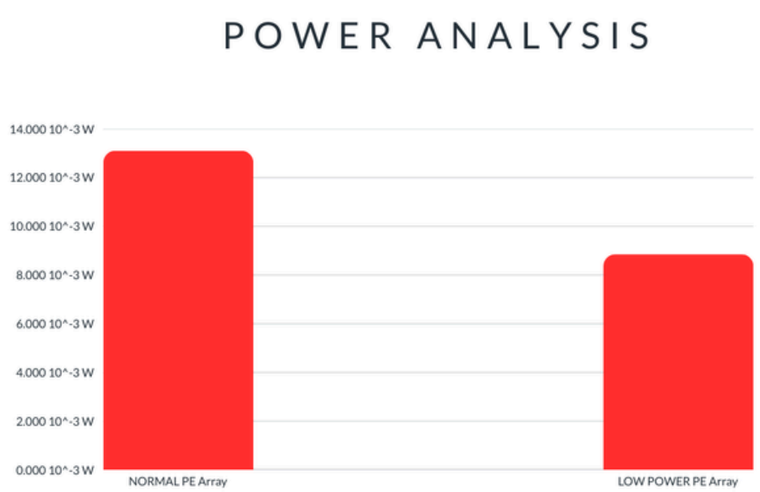
COMPLETED WORK WITH RESULTS

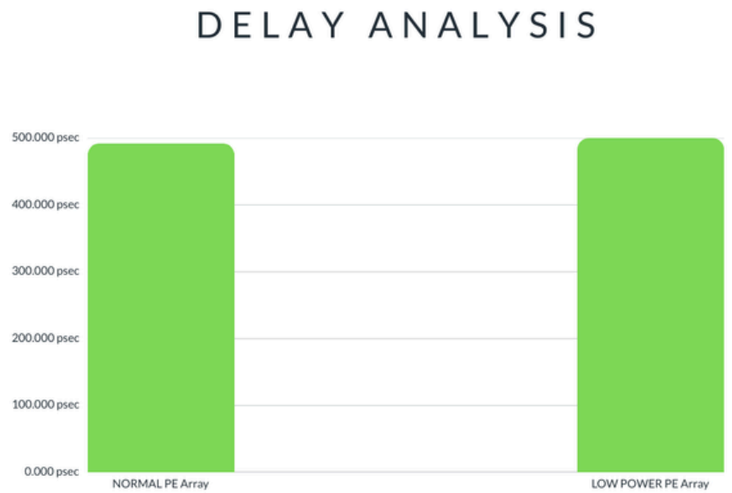
Comparison Table

	Actual Processing Element Array	**Optimized Processing Element Array**
Area	17328.469µm	16933.367 µm
Power	13.1807 milliwatts	8.84629 milliwatts
Delay	492 ps	500 ps

COMPLETED WORK WITH RESULTS

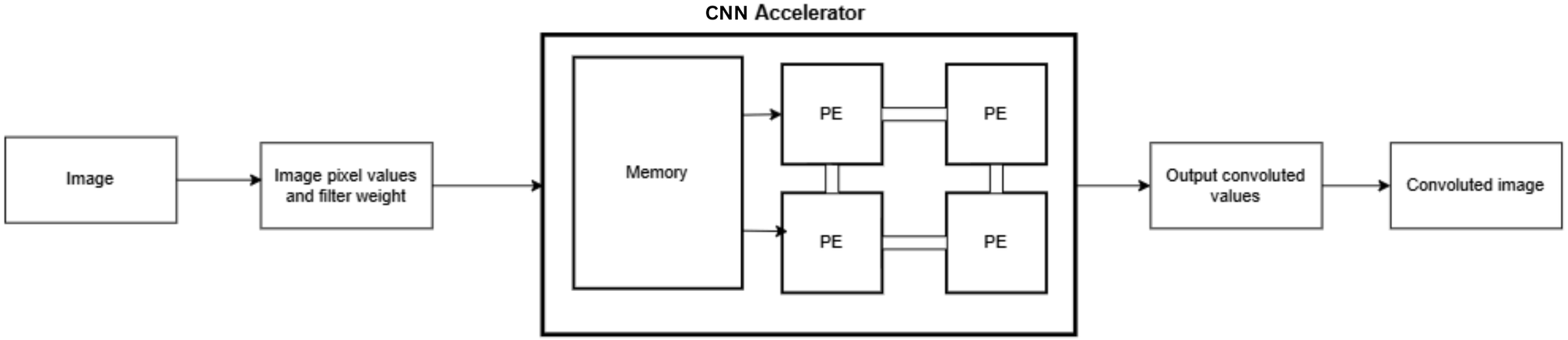
Graphical representation

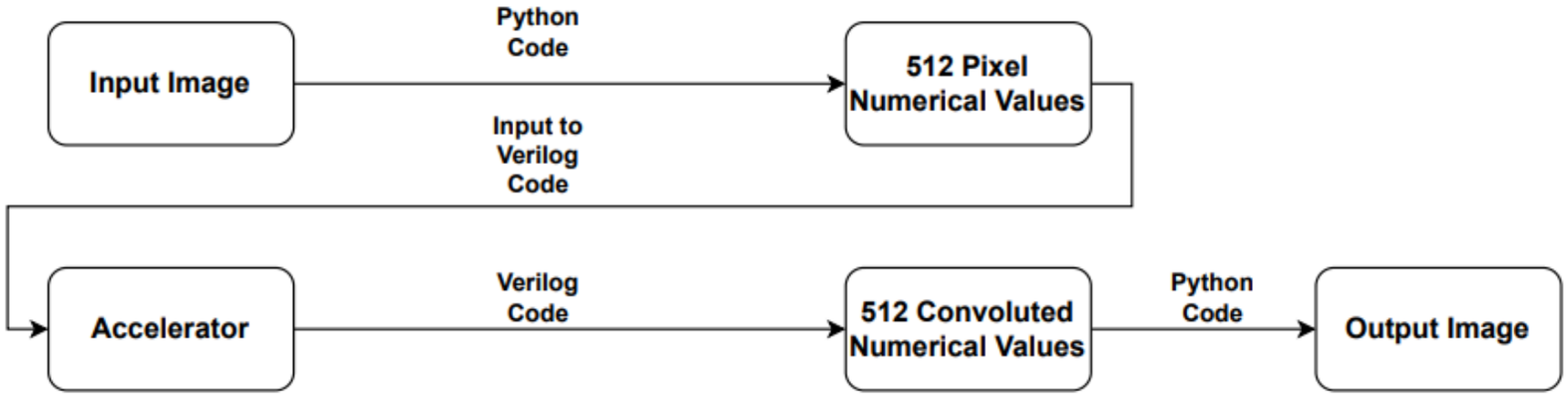




In summary, the optimized processing element array shows improvements in both area and power consumption. However, there is a slight increase in delay compared to the actual array, which might be acceptable depending on the specific performance requirements and trade-offs considered during the optimization process.

Real-World Use Cases of the Proposed CNN Accelerator





Real-World Use Cases of the Proposed CNN Accelerator

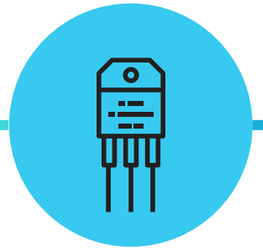
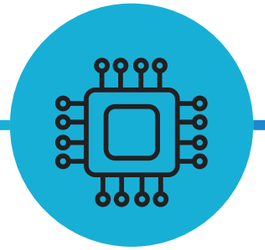
Simulation Output of PE Array

```
Smoothing Filter Output:
      3060
      3485
      3995
      4080
      3995
      3655
      3230
      3145
      3400
      3740
```

COMPLETED WORK WITH RESULTS

Application of Our Work-

TIMELINE

2024	JAN-FEB 2025	FEB 2025	APRIL-MAY2025	MAY-2025
				
Topic and Idea Pitching	1st Review : **Normal Architecture Design**	2nd Review : **Low Power Architecture Design**	3rd Review : **Report and Documentation**	**Completion of Project and Research Paper**

Real-World Use Cases of the Proposed CNN Accelerator

1. Edge AI Devices

Smart cameras, drones, robotics – Low-power, real-time object detection.

2. Medical Imaging

Portable diagnostic tools – Fast, energy-efficient analysis of X-rays/MRI scans.

3. Autonomous Vehicles

Lane/pedestrian detection – High-speed processing with minimal power.

4. IoT & Smart Farming

Crop disease monitoring – TinyML integration for low-cost sensors.

5. Surveillance Systems

24/7 anomaly detection – Power-efficient CCTV processing.

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THANK YOU