Sarveshware

VLSI and Microelectronics graduate engineer with hands-on experience in RTL design, low-power ASIC development, and verification, passionate about advancing semiconductor IP and EDA innovation.

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EDUCATION

PSG Institute of Technology and Applied Research

B.E. Electronics and Communication Engineering CGPA - 8.7 June 2021 - April 2025

Relevant Coursework: Digital Electronics, Low Power IC Design, VLSI Testing & Design Verification (DFT), Circuit Theory, Computer Architecture, CMOS Analog IC Design, Mixed-Signal IC Design (ADC, DAC)

SKILLS

- **Programming:** Python scripting, C, Object Oriented Programming
- **Hardware Description Language:** Verilog, System Verilog
- **Tools & Platforms:** Cadence Virtuoso, Xilinx Vivado, PSPICE, Matlab, Icarus, Cadence Genus,Synopsys VCS
- **Hardware Boards:** Raspberry Pi, 8051, ARM (RISC Processor), PYNQ-Z2, Zed Board
- **Leadership Experience:** Class Representative in College first year, House Captain in school

PROJECTS

Design and Implementation of Efficient Processing Element Array for CNN Accelerator Feb 2025 - April 2025

- An **FPGA-based CNN Accelerator** designed using a modular **Processing Element (PE) Array** to address the computational complexity and high power consumption of deep learning models on edge devices.
- Each PE integrates a **Dadda multiplier** and a **Hybrid adder**, capable of arithmetic and logic operations including convolution.
- Implemented using **Xilinx Vivado** and **Cadence tools**, the optimized array achieved **33% power reduction,**with minimal area tradeoff and acceptable delay increase.
- Validated through simulation and RTL schematics, the design demonstrates real-world applications in **Image Processing**.
- *Awarded "Best Final Year Project"* in the Department of Electronics and Communication Engineering on **31st May 2025** for this project.

UART Design using Xilinx Vivado May 2024 - Jun 2024

- Implemented a UART module with **95%** reliability for **FPGA**-based one-to-one communication.
- Integrated a memory-based Finite State Machine **(FSM)** with a Parallel-In Serial-Out **(PISO)** transmitter and a Serial-In Parallel-Out **(SIPO)** receiver using **RTL design** methodology as **Verilog code**.
- Developed **RTL-level testbenches** and conducted basic **functional simulation using Vivado** for module-level verification

Sustainable Low-Power ALU and MUX Design Feb 2024 - Mar 2024

- Achieved a **20%** reduction in power consumption within the Processing Element blocks without compromising performance and **SoC functionality coverage**. Worked up to the **place-and-route** stage in **Physical Design**.
- Transitioned the design style of Processing Element blocks from **CMOS to MGDI**, significantly enhancing power efficiency. This project was recognized as the **Best Cadence Project** among **10 teams** at **SRISHTI'24**.
- Designed using the **EDA tool Cadence Virtuoso** for circuit simulation and pre-silicon architectural design.

CERTIFICATIONS

Certificates Link

- Achieved a Silver badge in the NPTEL course "**System Design Through Verilog**" with a score of **75%**.
- Secured **100%** in the "**Verilog for FPGA Engineers**" course on Udemy.
- Excelled in the "**CCNA Networking Essentials**" course on the CISCO Netacad platform, scoring **93%**.
- Attained a flawless **100%** in the "**Static Timing Analysis**" course on Udemy.

PAPER PUBLICATIONS

- Authored and submitted "**Power-Efficient 4-Bit Basic Multiplier Optimization Using Approximate Designs and Modified Gate Diffusion Technique**" to VDAT 2024**.**
- Presented "**Sustainable Low-Power 2-Bit ALU and Multiplexer-Based AI Accelerator Design and Optimization Using Cadence Virtuoso**" at **IC(SEC) 2024**, an IEEE-sponsored conference, with **20%** plagiarism.

ACHIEVEMENTS

- 1st place in Embedded System Design Project Expo, PSG College, May 2024.
- Best Cadence Project at SRISHTI'24, Saintgits College of Engineering, Feb 2024.
- 2nd place in IRDC (International Rover Design Competition), May 2023.