Design guidelines for the shutdown function in the SLLIMM-nano series

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Introduction

The SLLIMM™-nano 1st and 2nd series consist of two product families of compact, intelligent power modules offering several advanced functions and protection features such as an op-amp for advanced current sensing, NTC thermistor for temperature monitoring, interlocking function to prevent shoot-through, undervoltage lockout, comparator for fault protection against overcurrent or short-circuit and smart shutdown function.

The smart shutdown function is based on innovative patented circuitry internally connected to the comparator, which provides intelligent fault management and greatly reduces delays in protection intervention.

Both SLLIMM-nano families are equipped with three half bridge IC gate drivers. There is just one comparator input pin (CIN) which is directly connected to the U IC gate driver and one shutdown pin ($\overline{SD}$ / OD) which internally connects all three IC gate drivers. In order to take advantage of the smart shutdown function and to perform very fast, effective overcurrent protection on all legs, an external RC network on the $\overline{SD}$ / OD pin must be added and properly designed.

This application note will describe the how the smart shutdown (SSD) function and the shutdown (SD) work, while providing guidelines for proper external hardware design to implement active overcurrent protection.

Contents

1 Internal circuit

The SLLIMM-nano 1st and 2nd series devices relevant to this application note are the following:

- STGIPN3H60[1]
- STGIPN3H60-E[1]
- STGIPN3H60-Hx([1]
- STGIPN3H60T-H[2]
- STIPNxM50-H[1]
- STIPNxM50T-Hy[2]
- STGIPQxH60T-Hy[2]
- STGIPQxC60T-Hy[2]
- STIPQxM60T-Hy[2]

[1] without NTC thermistor, [2] with NTC thermistor

They may or may not be equipped with an NTC thermistor. Therefore, the internal circuitry of the above-listed SLLIMM-nano devices can differ by specific part number as a function of the presence of the NTC. The SLIMM-nano 1st and 2nd series with NTC thermistor are capable of sensing the module temperature.

In the devices housing the NTC, the SD function and the thermistor share the same pin T / $\overline{\text{SD}}$ / OD. They can coexist, but specific design guidelines must be taken into account for the external SD circuit design in order to avoid any undesired shutdown events. Therefore, different guidelines must be followed when using the SLLIMM-nano with or without the NTC, as will be explained hereafter in *Section 3: "Design guidelines"*.

Thanks to the open emitter configuration of the SLLIMM-nano, it is possible to monitor the instantaneous currents by using one or three shunt resistors. The shunt voltage can be sensed through the internal comparator (CIN) pin, providing protection against overcurrent and short-circuit events in a very short time, thanks to the smart shutdown and shutdown functions. The smart shutdown function is a dedicated feature connected to the comparator of the U gate driver only and is able to turn off the switches of the U leg in a few hundred nanoseconds (dashed and dotted, blue path in *Figure 1*, *Figure 2* and *Figure 3*), whereas the other two legs, V and W, are internally connected to the U gate driver through the $\overline{\text{SD}}$ / OD pad (dashed, green path). This internal path is responsible for the overcurrent protection of the V and W legs thanks to the SD function and the external RC circuit, the design of which will be described in detail in *Section 2: "Smart shutdown and shutdown function"*. The $\overline{\text{SD}}$ / OD pin (or T / $\overline{\text{SD}}$ / OD pin if using the NTC-embedded SLLIMM-nano) can be used either as an input or output pin.

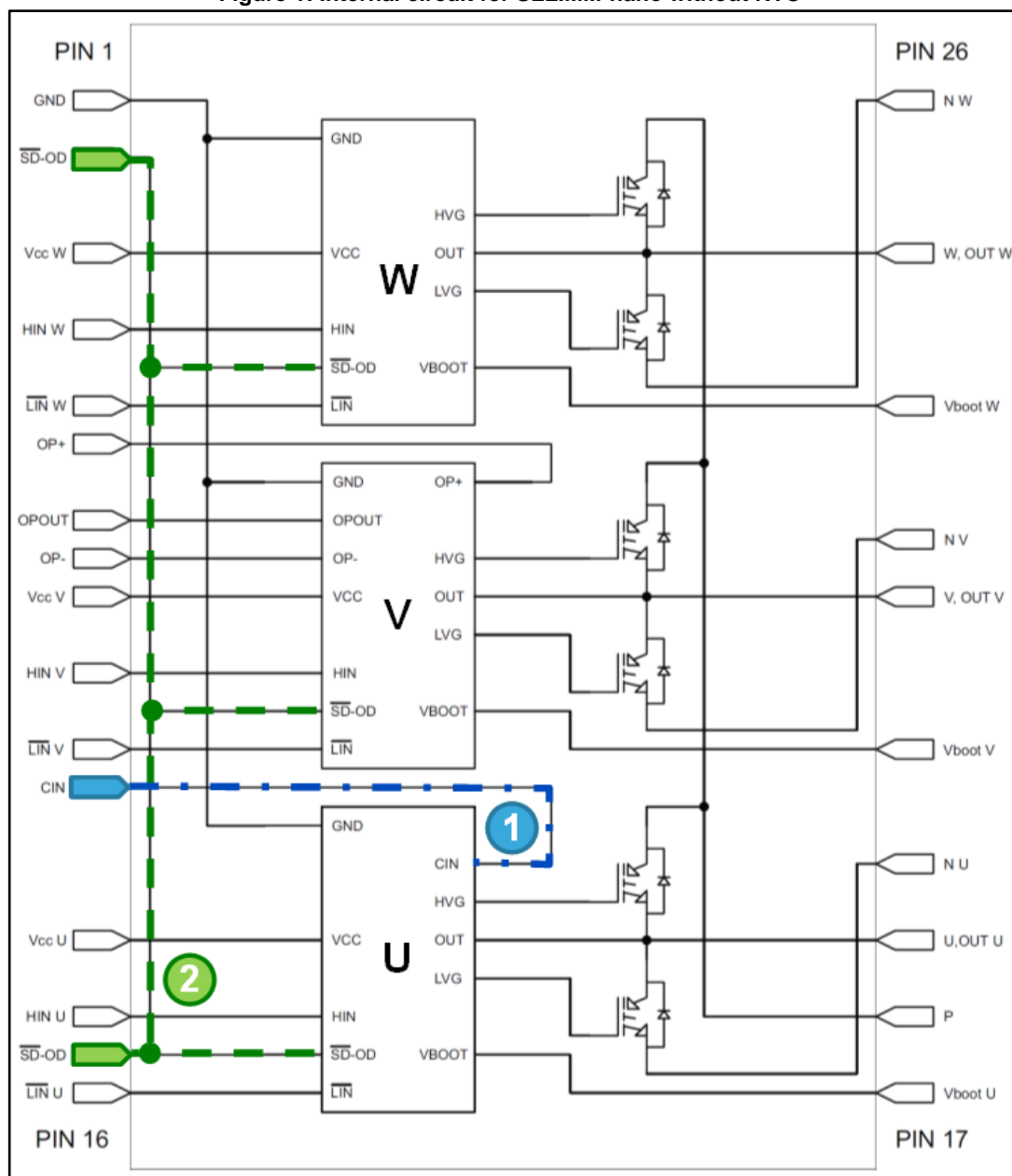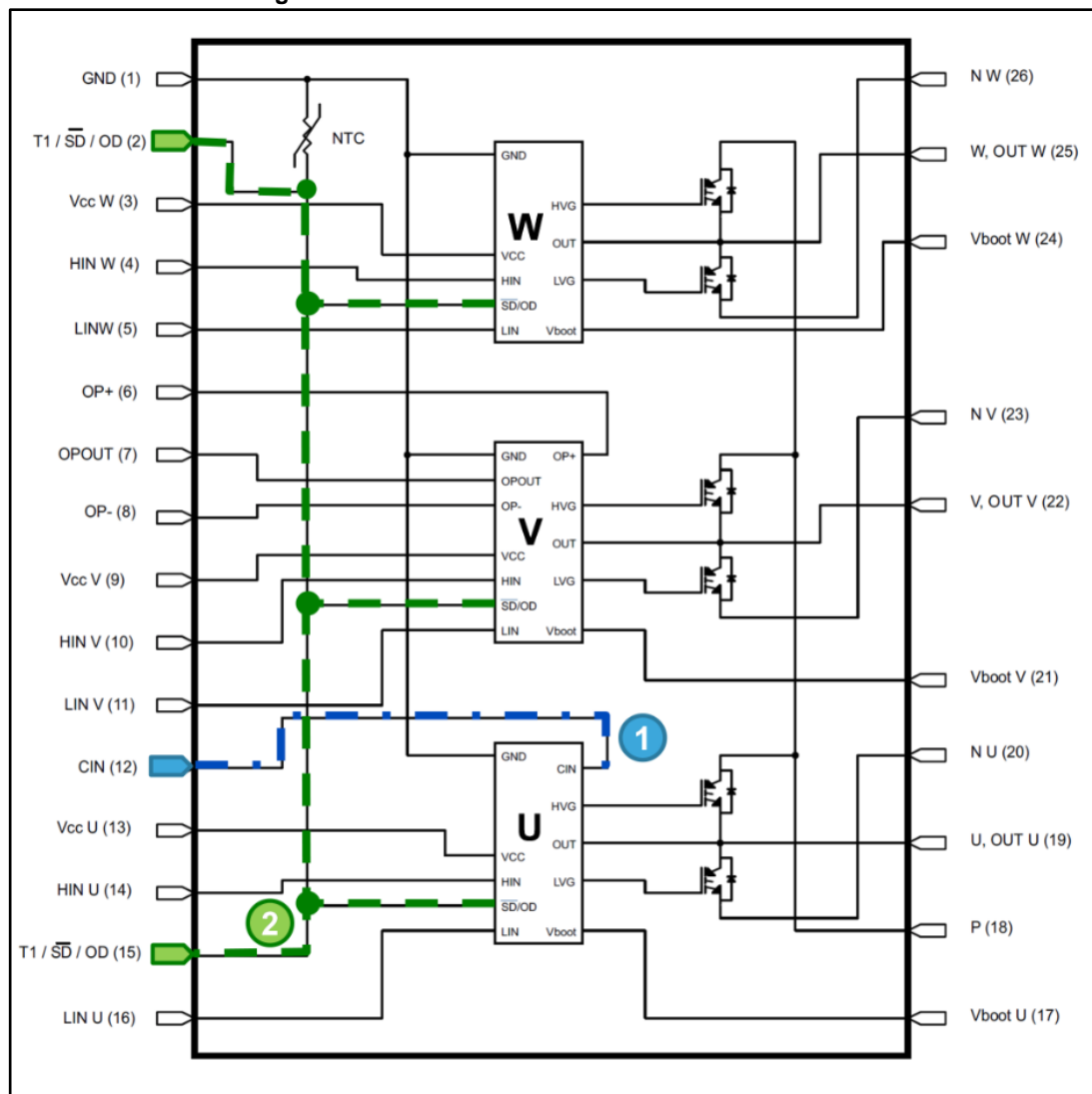**Figure 1: Internal circuit for SLLIMM-nano without NTC**

Figure 2: Internal circuit for SLLIMM-nano with NTC

2 Smart shutdown and shutdown function

The details of the IC gate drivers for the SLLIMM-nano are shown below in *Figure 3* along with the external RC circuit to be added to obtain the proper behavior for overcurrent protection.

Figure 3: SD and SSD gate driver detail
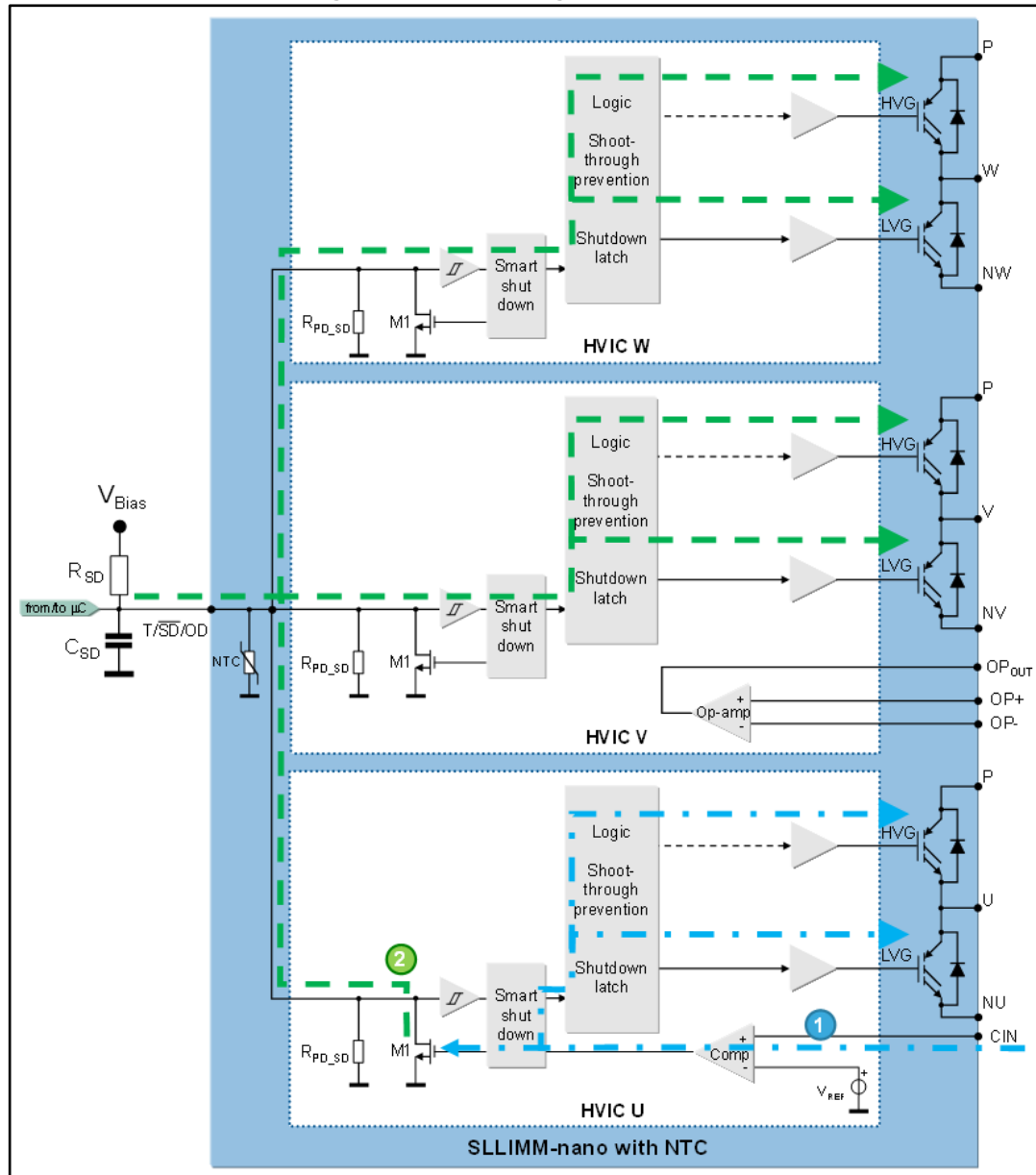
The comparator is integrated on the U IC gate driver and has an internal reference voltage, V_{REF}, on its inverting input, whereas the non-inverting input is available on the CIN pin. The comparator provides the ability to monitor the current, ensuring protection against overcurrent and short-circuit events. The output signal of the comparator enables the smart shutdown (SSD) function (dashed and dotted, blue path) which is responsible for very fast

overcurrent protection of the module. Thanks to a preferential internal path, the SSD is able to set the outputs of the U gate driver (HVG and LVG) to low level in only 200 ns (typical propagation delay time) while at the same time switching on the open drain MOSFET M1 available on the $\overline{SD}$ / OD pin (or T / $\overline{SD}$ / OD pin). The SD pin is connected to the external RC network (R_{SD} and C_{SD}) in order to obtain a mono stable circuit. This external RC network also determines the protection time on the V and W legs when a fault condition occurs, as shown by the dashed, green path.

In *Figure 4* the timing chart of an overcurrent event is represented. At t2, the fault event is detected, the outputs of U gate drive (LVG, HVG) are immediately set to low level, protecting the U leg, and the M1 MOSFET is switched on. The external capacitor C_{SD} then starts the discharging phase with a time constant τ_A since the SD voltage is pulled down through the M1 R_{ON_OD} resistor.

Figure 4: Timing chart of the smart shutdown function


------- Overcurrent in V/W phase
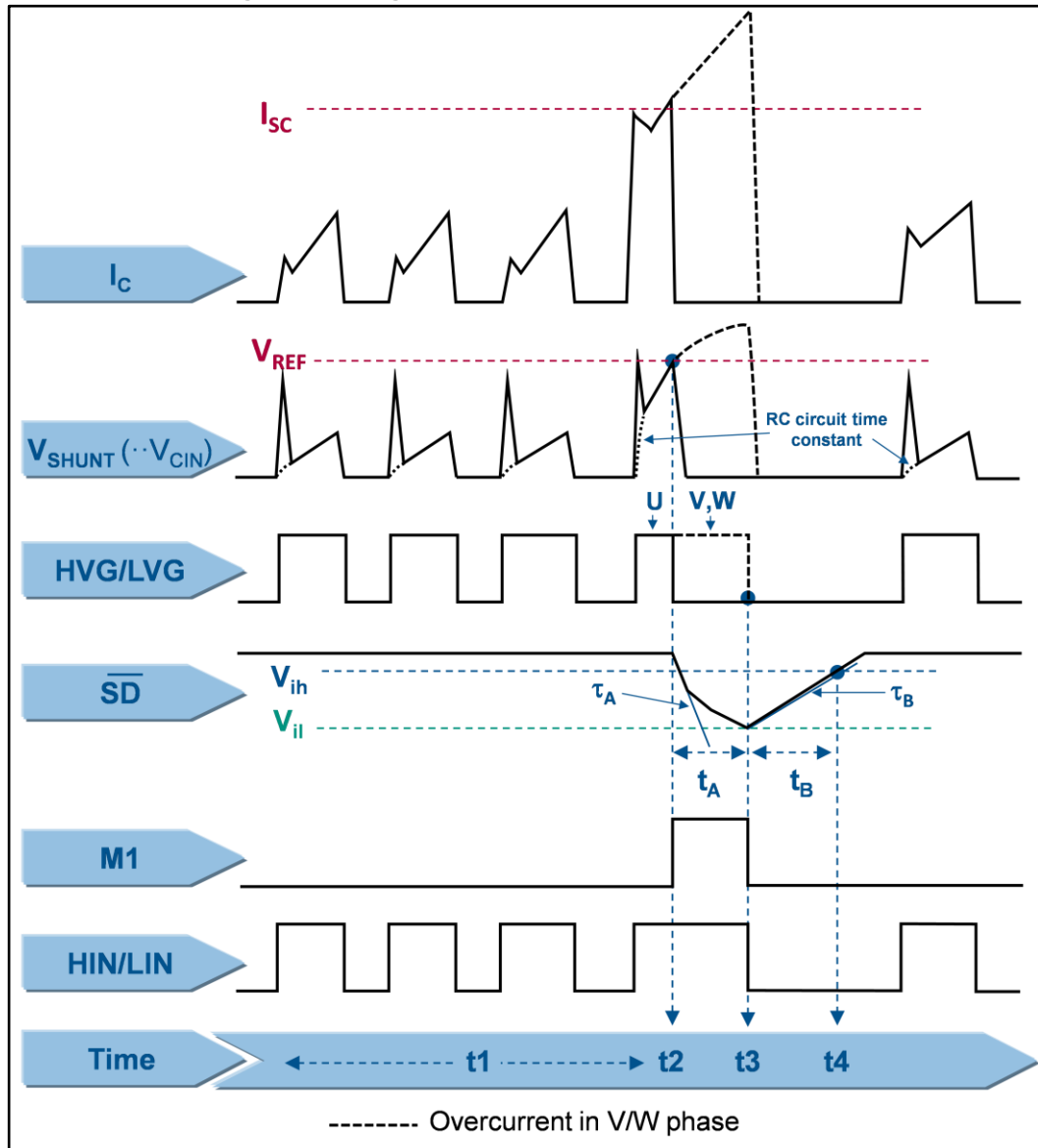
As soon as the SD voltage reaches the internal lower threshold V_{il} (t3), the V and W driver outputs are also set to low level and the device is completely turned-off.

Starting from that moment, the M1 MOSFET is switched off, leading the external RC circuit back to a charging phase with τ_B time constant. When the SD voltage reaches the high level logic threshold voltage V_{ih} (t4) the system is eventually re-enabled.

The two time constants, τ_A and τ_B, are different for SLLIMM-nano with or without the NTC thermistor, since the equivalent circuit can change accordingly, as shown in *Figure 5*.

Figure 5: Shutdown circuits with and without the NTC
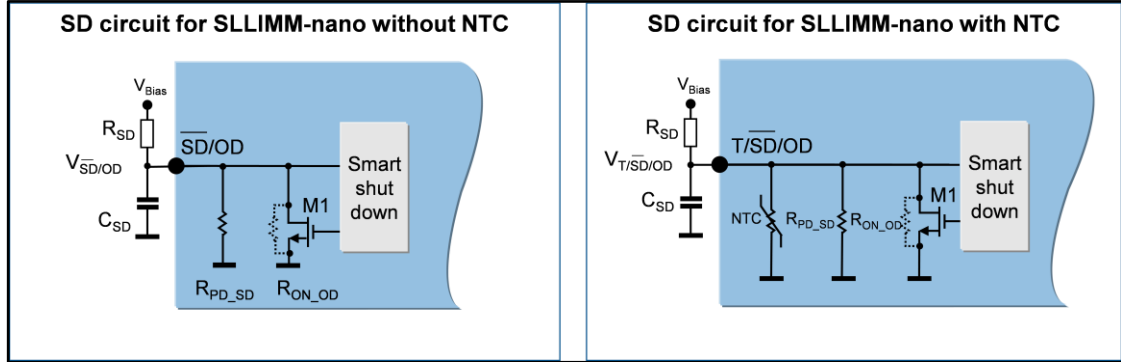
In the devices without NTC thermistor, the time constant τ_A and τ_B are given by:

Equation 1

$$\tau_A = (R_{ON\_OD} \mathbin{/\!/} R_{SD} \mathbin{/\!/} R_{PD\_SD}) \cdot C_{SD} \cong R_{ON\_OD} \cdot C_{SD}$$

Equation 2

$$\tau_B = (R_{SD} \mathbin{/\!/} R_{PD\_SD}) \cdot C_{SD}$$

In the devices with NTC thermistor, the time constant τ_A and τ_B are given by:

Equation 3

$$\tau_A = (R_{ON\_OD} \mathbin{/\!/} R_{SD} \mathbin{/\!/} R_{PD\_SD} \mathbin{/\!/} R_{NTC}) \cdot C_{SD} \cong R_{ON\_OD} \cdot C_{SD}$$

Equation 4

$$\tau_B = (R_{SD} \mathbin{/\!/} R_{PD\_SD} \mathbin{/\!/} R_{NTC}) \cdot C_{SD}$$

As previously discussed, the overcurrent intervention delay time t_A (defined as the time interval t3 – t2) is strictly linked to the time constant τ_A, which is a function of the R_{SD} and C_{SD} values. Therefore, the external RC network must be carefully designed for effective protection of the device, as explained in *Section 3: "Design guidelines"*.

3 Design guidelines

The design guidelines to be followed to ensure effective overcurrent protection of the SLLIMM-nano are described in this section. The external RC network (R_{SD} and C_{SD}) needed for the SD function must be designed according to specific guidelines dedicated to SLLIMM-nano with NTC or without NTC. Any other external network that may be connected to the SD pin, other than a simple R_{SD}-C_{SD} mono stable circuit (e.g. additional filter, optocoupler or latching circuit), needs to be taken into account with their passive or active components in order to estimate the actual time constants.

3.1 SLLIMM-nano without NTC

If using the SLLIMM-nano without NTC, the pull-up R_{SD} resistor and C_{SD} capacitor can be correctly sized by following a few steps.

The R_{SD} value must be designed in order to guarantee an open drain voltage drop lower than the low logic level threshold V_{il} (i.e. $V_{OD} \leq 500$ mV @ $I_{od} = 3$ mA), and it is a function of the pull-up supply voltage (V_{Bias}), as expressed by the following:
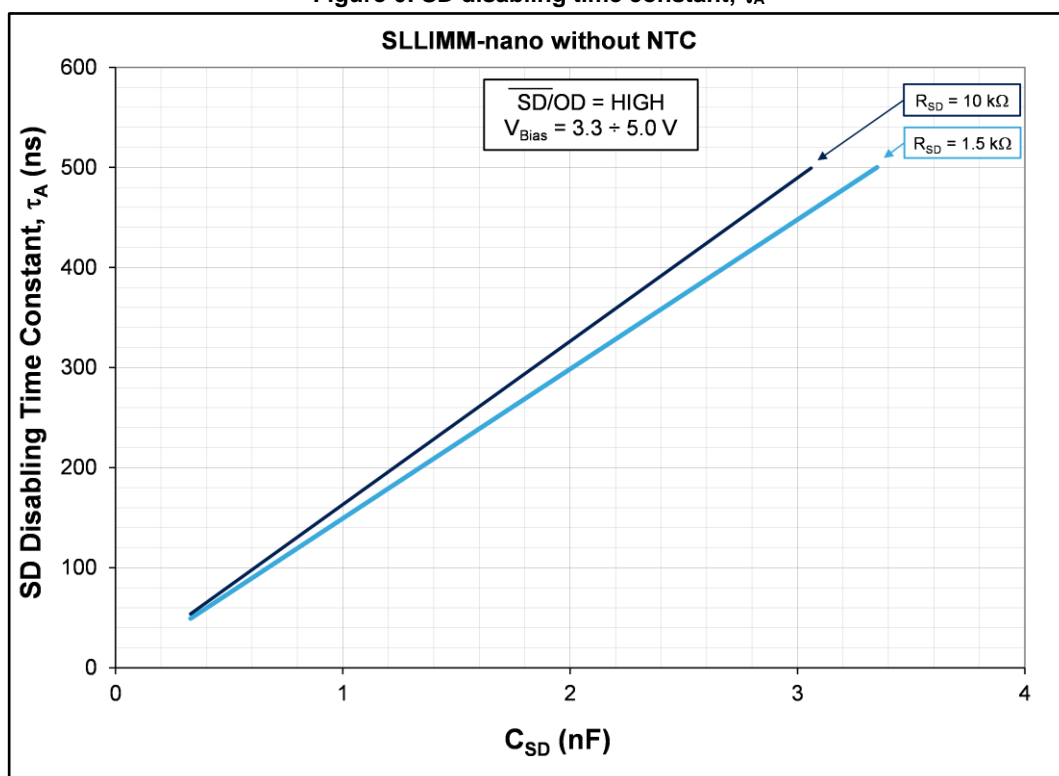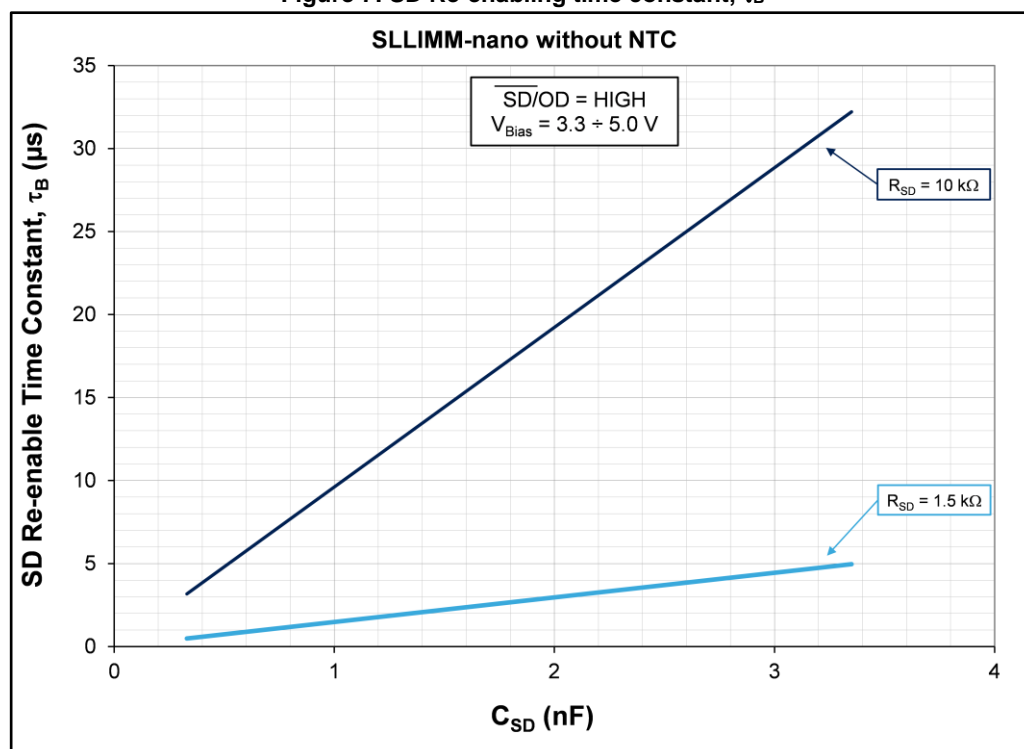
Equation 5

$$R_{SD} \geq \frac{V_{Bias} - V_{OD}}{I_{od}}$$

The C_{SD} value, along with the R_{SD}, sets the SD disabling (τ_A) and re-enabling (τ_B) time constants and t_A (linked to τ_A) is responsible for protection of the V and W legs.

It is recommended to set the disabling time constant τ_A no higher than 500 ns in order to guarantee a fast shutdown time also for the V and W legs.

Figure 6 and *Figure 7* show the trends of τ_A and τ_B respectively as a function of the C_{SD} capacitor.

Figure 6: SD disabling time constant, τ_A

Figure 7: SD Re-enabling time constant, τ_B

The curves shown have been derived starting from Equation *1* and *2*.

An RC filter (R_{SF}, C_{SF}) is recommended at the CIN pin to avoid sensing noise on the shunt resistor. Since it adds a time delay to the SSD/SD total intervention time, starting from the fault instant, its time constant is recommended to be no greater than 1 µs. Therefore the total disable time t_{Total} necessary to switch off the SLLIMM-nano starting from the fault event is:

Equation 6

$$U \text{ leg only: } t_{Total,U} = t_{SF} + t_{isd} + t_{off}$$

Equation 7

$$V \text{ and } W \text{ legs: } t_{Total,V\,W} = t_{SF} + t_{d\_comp} + t_A + t_{sd} + t_{off}$$

where:

- t_{SF} is the time delay due to the shunt RC filter
- t_{isd} is the propagation delay time of the gate driver, from comparator to high/low side driver turn-off (refer to the device datasheet)
- t_{d_comp} is the propagation delay time of the gate driver, from comparator to SD (refer to the device datasheet)
- t_A is the SD disabling delay time during the RC discharging phase (t3 – t2 in *Figure 4*), which depends on τ_A.
- t_{sd} is the propagation delay time of the gate driver, from SD to high/low side driver turn-off (refer to the device datasheet)
- t_{off} is the IGBT turn-off time

3.2 SLLIMM-nano with NTC thermistor

If using an NTC-embedded SLLIMM-nano, as previously stated it is internally connected between the SD path and ground, therefore its resistance must be taken into account. The equivalent parallel resistance of the NTC thermistor and pull-down resistor R_{PD_SD} is shown below as a function of temperature (*Figure 8*). Temperature monitoring and the SD function can coexist on the same pin if a proper external pull-up resistor R_{SD} is designed. To avoid unwanted shutdown, the SD voltage should be kept higher than the high-level logic threshold V_{ih} during normal operation of the module for all of the allowed operating temperatures. This is done by setting the R_{SD} to 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU bias voltages, respectively (see *Figure 9*).
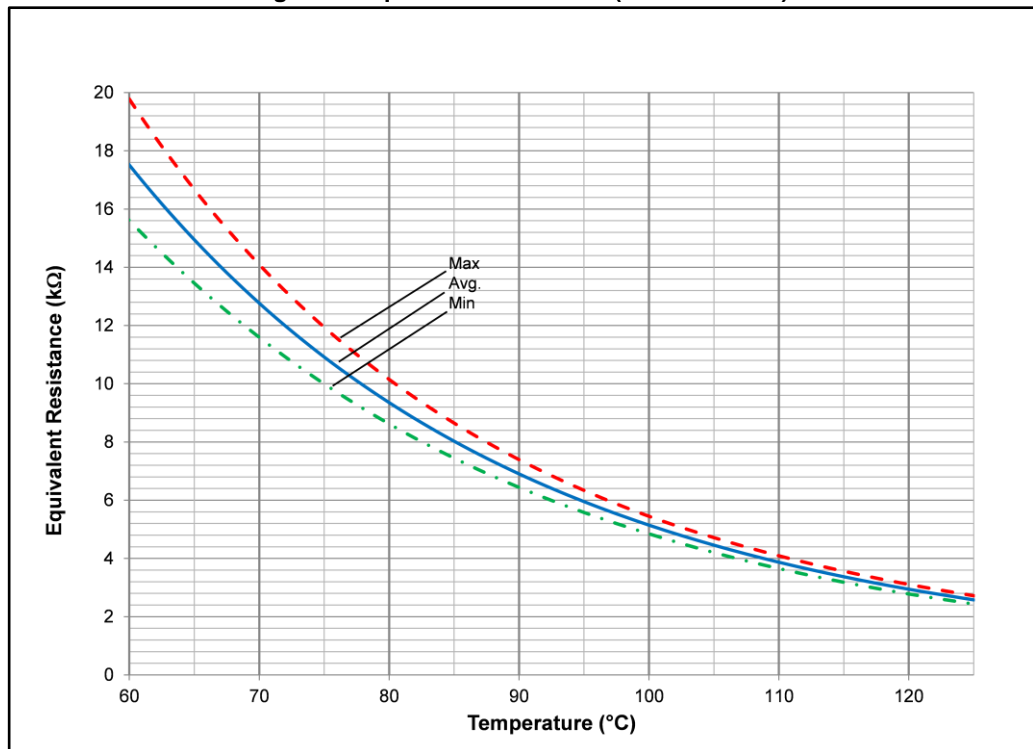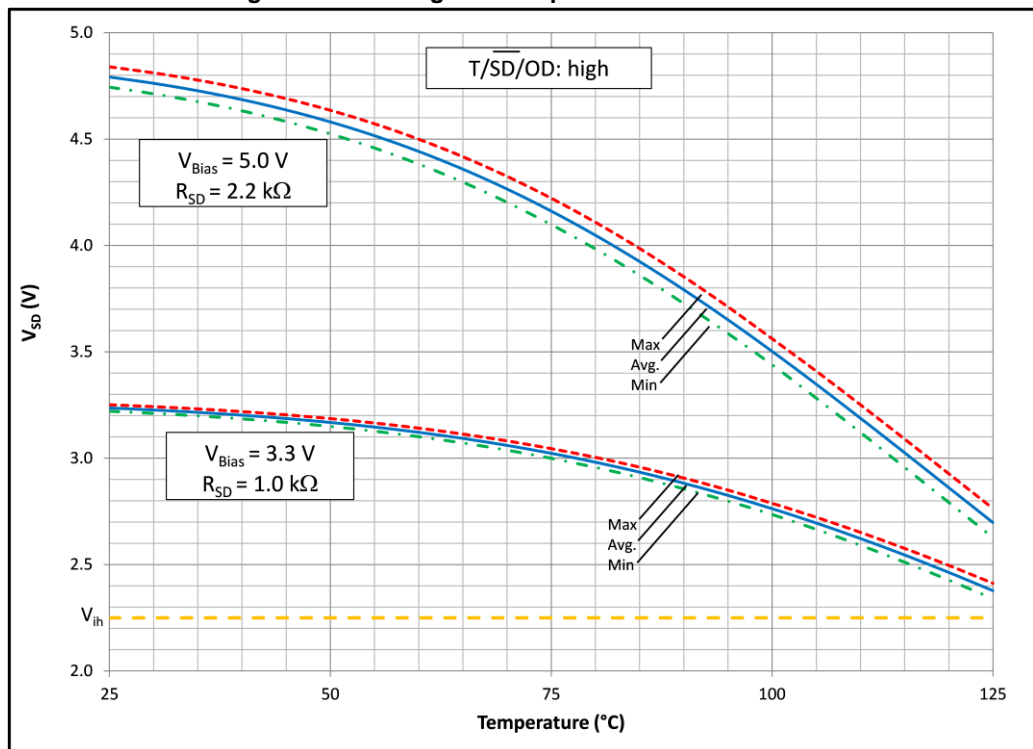
Figure 8: Equivalent resistance (NTC//RPD_SD)

Figure 9: SD voltage in NTC-provided SLLIMM-nano

The C_{SD} value, along with the R_{SD}, will set the SD disabling (τ_A) and re-enabling (τ_B) as represented in *Figure 10* and *Figure 11* respectively, considering the recommended

disabling time constant τ_A not higher than 500 ns for a fast shutdown time also for the V and W legs.

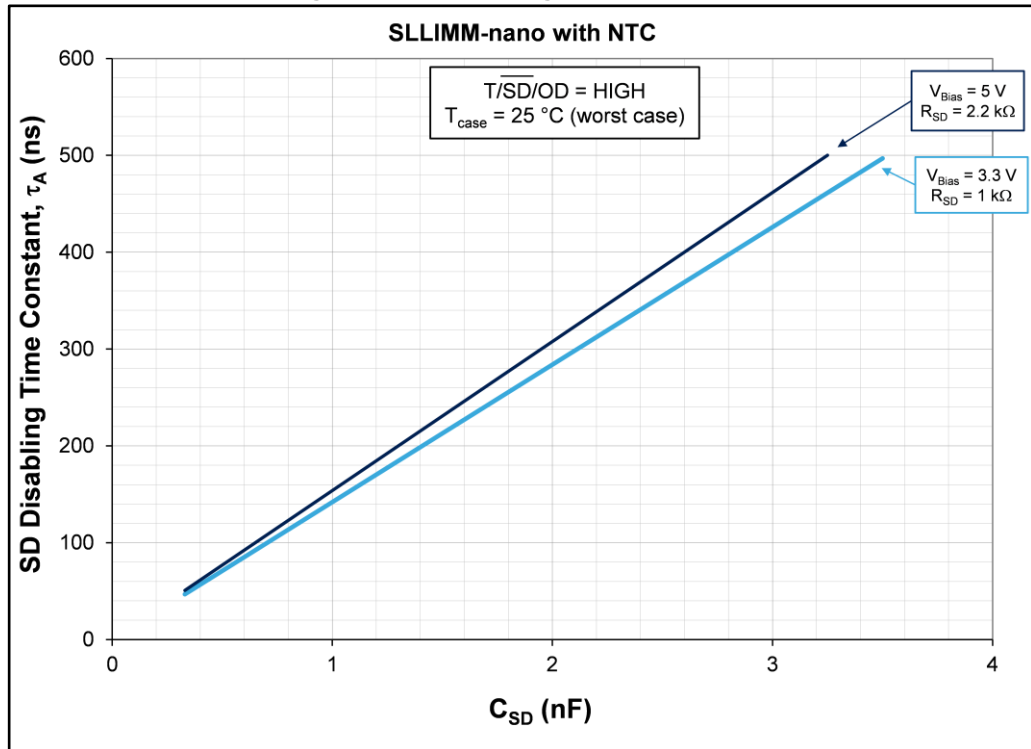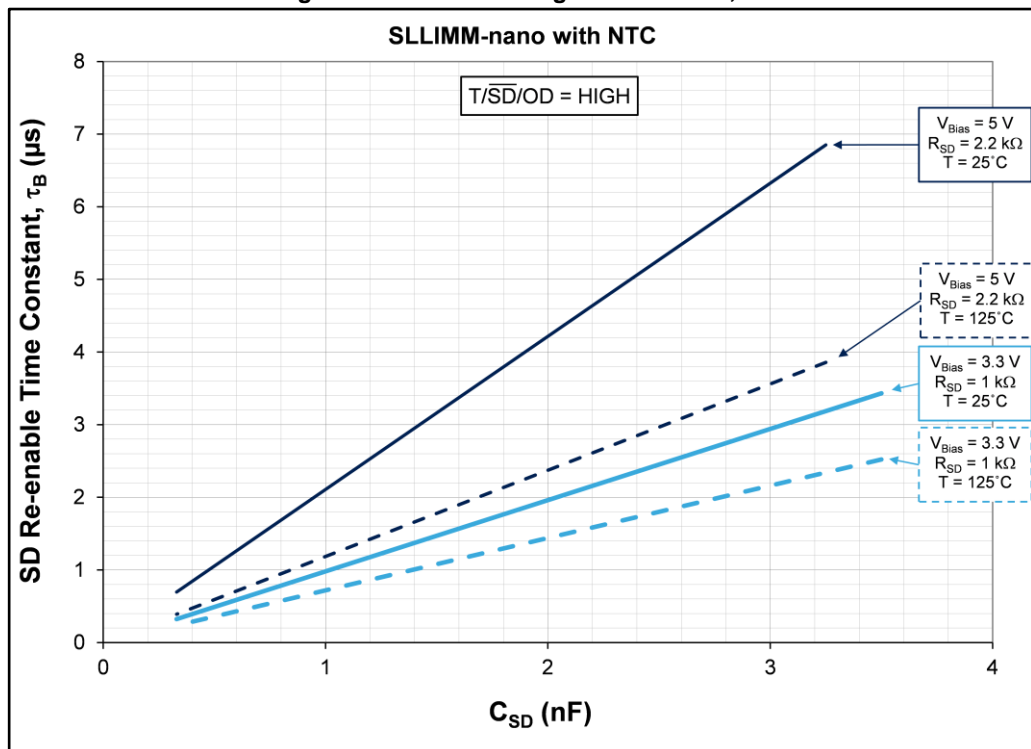**Figure 10: SD disabling time constant, τ_A**

Figure 11: SD re-enabling time constant, τ_B

The curves shown have been derived starting from Equation 3 and 4 and the total disable time t_{Total} necessary to switch off the SLLIMM-nano starting from the fault event, is still given by Equation 6 and 7. Only t_A (SD disabling delay time during the RC discharging phase) is impacted by the NTC thermistor.

4 Experimental results

In this section, two practical test cases are analyzed. The first one refers to a correct configuration of the external SD circuit which ensures proper overcurrent protection behavior. The second case is instead based on a non-recommended configuration, which could lead to module damaged in case of a fault event.

4.1 Example of suggested configuration
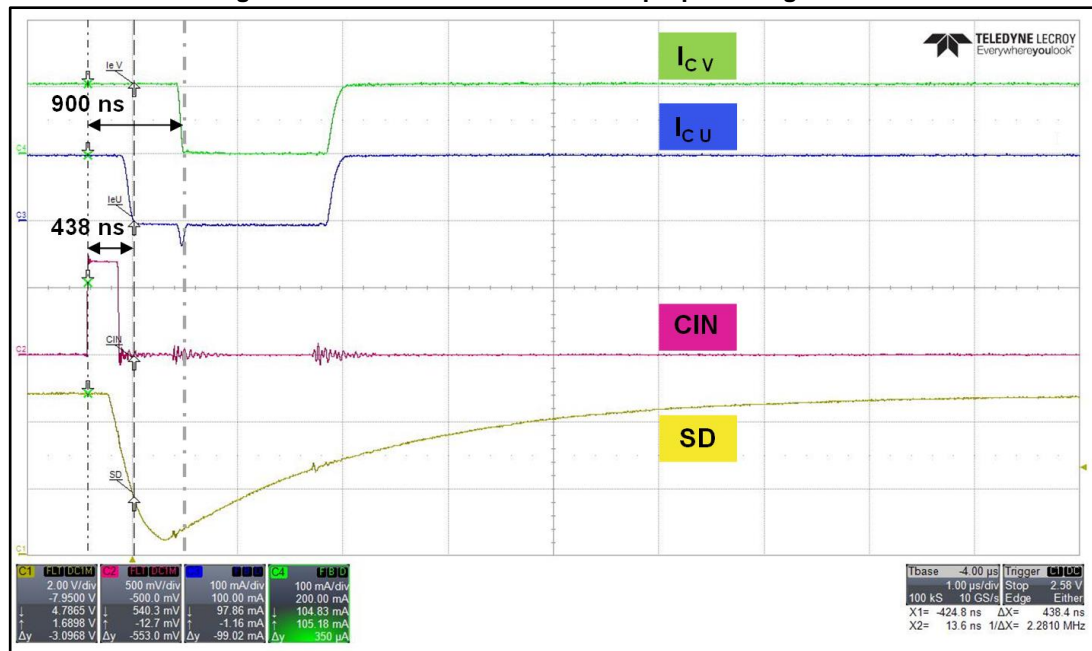
The test configuration is as follows:

- STIPN1M50T-H (SLLIMM-nano 1st series with NTC)
- V_{Bias} = 5 V
- R_{SD} = 2.2 kΩ
- C_{SD} = 1 nF

Since the considered module is NTC-provided, according to the guidelines one of the two MCU voltage/pull-up resistor configurations (3.3 V – 1 kΩ or 5 V – 2.2 kΩ) must be used. Then, a 1 nF capacitor has been selected to obtain a proper disabling time constant, according to recommendations. Therefore the expected time constants are:

τ_A ≈ 150 ns τ_B ≈ 2100 ns @ T_{case} = 25 °C

These have been calculated using the formulas from *Figure 5*. The test consists in a SD/SSD intervention event through externally controlling the CIN pin in order to simulate an overcurrent event (shunt resistor voltage greater than V_{REF}). The test capture is shown in *Figure 12*. Low side IGBT emitter currents of the U and V legs along with SD and CIN voltage have been sensed. The same behavior of the V leg is applicable also on the W leg. As can be observed, the U leg is completely switched off (current $I_{C, U}$ going to zero) 438 ns after the CIN voltage exceeds the V_{REF} threshold, thanks to the SSD feature directly implemented on the U leg gate driver. This time delay comprises the SSD internal delay time (t_{isd}) and IGBT turn off time (t_{off}). The SD voltage starts to decrease after the comparator senses the overvoltage in t_{d_comp} (about 150 ns). Once the SD voltage reaches the low level logic threshold (V_{il}) the other two legs can also be switched off (V and W driver outputs low) and as a consequence, this eventually leads the module itself to be completely turned off. It is clearly shown that the overall process takes only 900 ns after the fault detection, thanks to a proper τ_A sizing which ensures fast and effective protection of the power module.

Figure 12: SD and SSD behavior with proper configuration

4.2 Example of an unsuitable configuration

The test configuration has been modified as follows:

- STIPN1M50T-H (SLLIMM-nano 1st series with NTC)
- V_{Bias} = 5 V
- R_{SD} = 2.2 kΩ
- C_{SD} = 100 nF

Since the C_{SD} has been changed to 100 nF, the new time constants are now expected to be:

τ_A ≈ 15 µs τ_B ≈ 210 µs @ T_{case} = 25 °C

This means that both t_A and t_B are now much higher than before, which leads to an improper total disable time for the V and W legs (nothing changes for the U leg). As shown in *Figure 13*, the V leg (as well as the W leg) is switched off in almost 40 µs, which is not recommended since it does not protect the module from short-circuit events.

Figure 13: SD and SSD behavior with an unsuitable configuration
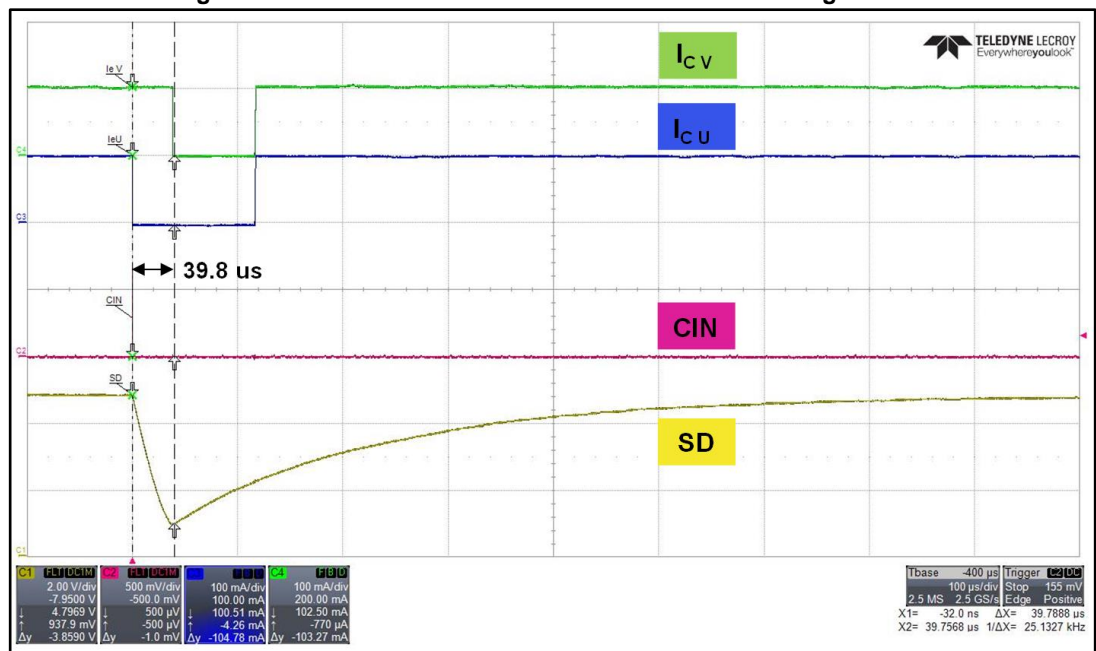
5 Conclusions

Thanks to the shutdown and smart shutdown features, the SLLIMM-nano 1st and 2nd series can be effectively protected from overcurrent and short-circuit events. The protection intervention delay time for the V and W phases are related to the external mono-stable circuit, thus its design must comply with the suggested guidelines discussed in this application note.

6 References

AN4043 - SLLIMM™-nano small low-loss intelligent molded module

AN4840 - SLLIMM™-nano 2nd series small low-loss intelligent molded module

7 Revision history

Table 1: Document revision history

Date	Version	Changes
01-Feb-2017	1	Initial release.

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