California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 5 Report

By

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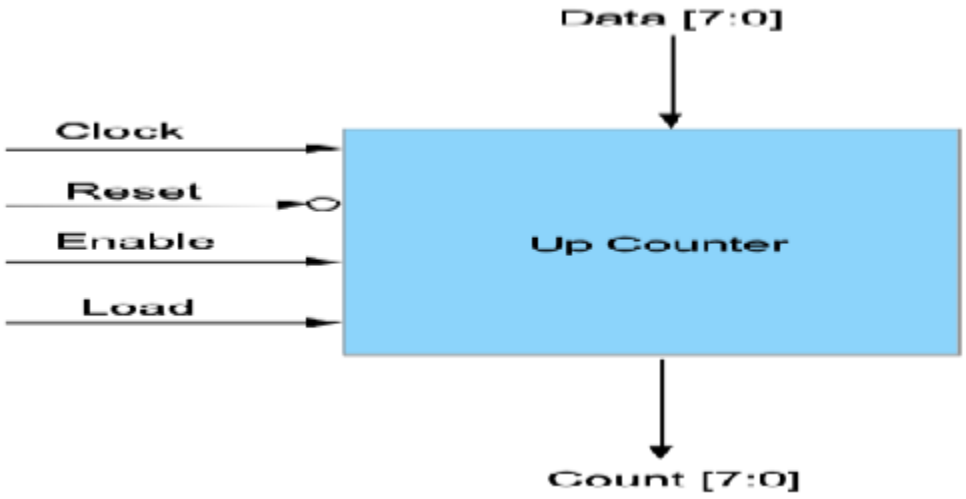
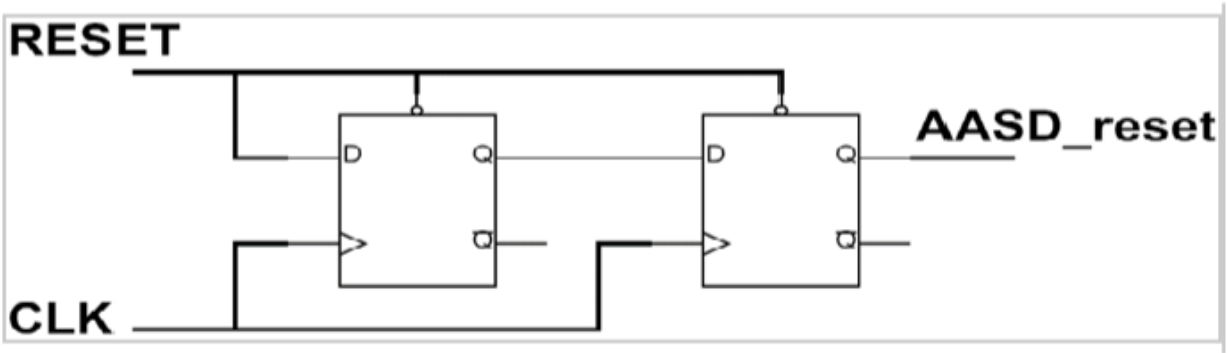
1: Introduction

The objective of this lab is to build Verilog model for a reloadable 8-bit up counter. And Implement an asynchronous assert, synchronous de-assert reset for the counter.



Here we have to use following diagram to build asynchronous assert, synchronous de-assert reset for the counter.



2: Procedure

a. Part 1: Creating Counter Module

In this lab I have created a Counter module for 8-bit up counter. Inside the module I have assigned “CLK, RST, ENA, LOAD, and DATA,” as input variables and “CNT” as output variables. Then I wrote the counting logic inside module. After completing the code I ended the module using and saved the file with name “Counter.v”.

b. Part 2: Creating AASD Module

In this lab I have created a module AASD for asynchronous assert, synchronous de-assert reset. Inside the module I have assigned “RESET, CLOCK” as input variables and “RST” as output variables. Then I wrote the AASD logic . After completing the code I ended the module using and saved the file with name “AASD.v”.

c. Part 2: Creating Top Module

In this lab I have created a module Top in wich I have instantiated Counter and AASD modules. After completing the code I ended the module using and saved the file with name “Top.v”.

d. Part 3: Creating Top_tb Module

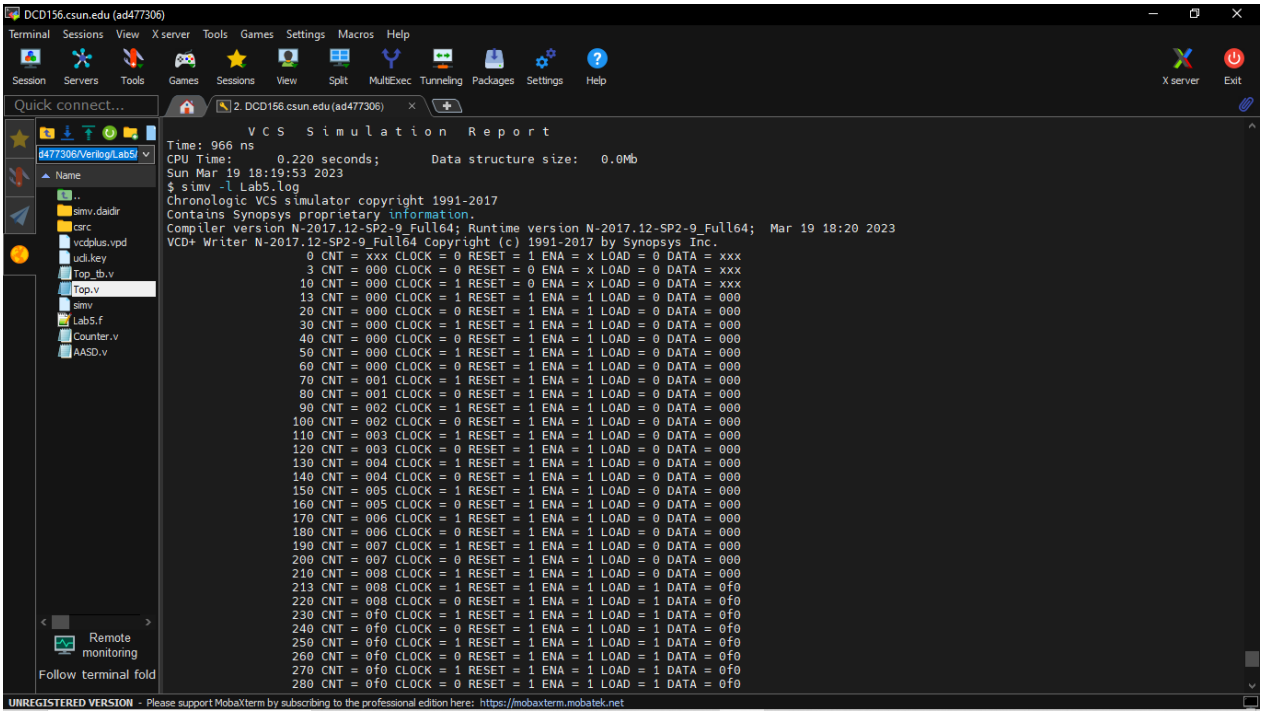
I have written the test bench for the Top module.We require test bench just to make sure that the module we have created is working properly. Here, in this testbench I have used some delays and after using trial and error method I got the final expected output.

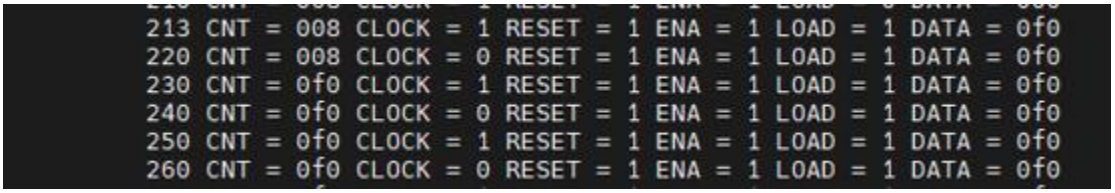
e. Part 4: Creating “.f ” file for execution.

I have created Lab5.f file and wrote “vcs -debug -full64 Counter.v AASD.v Top.v Top_tb.v” command in that file.
Now using “chmod +x Lab5.f” followed by “./Lab5.f” command I executed the file.

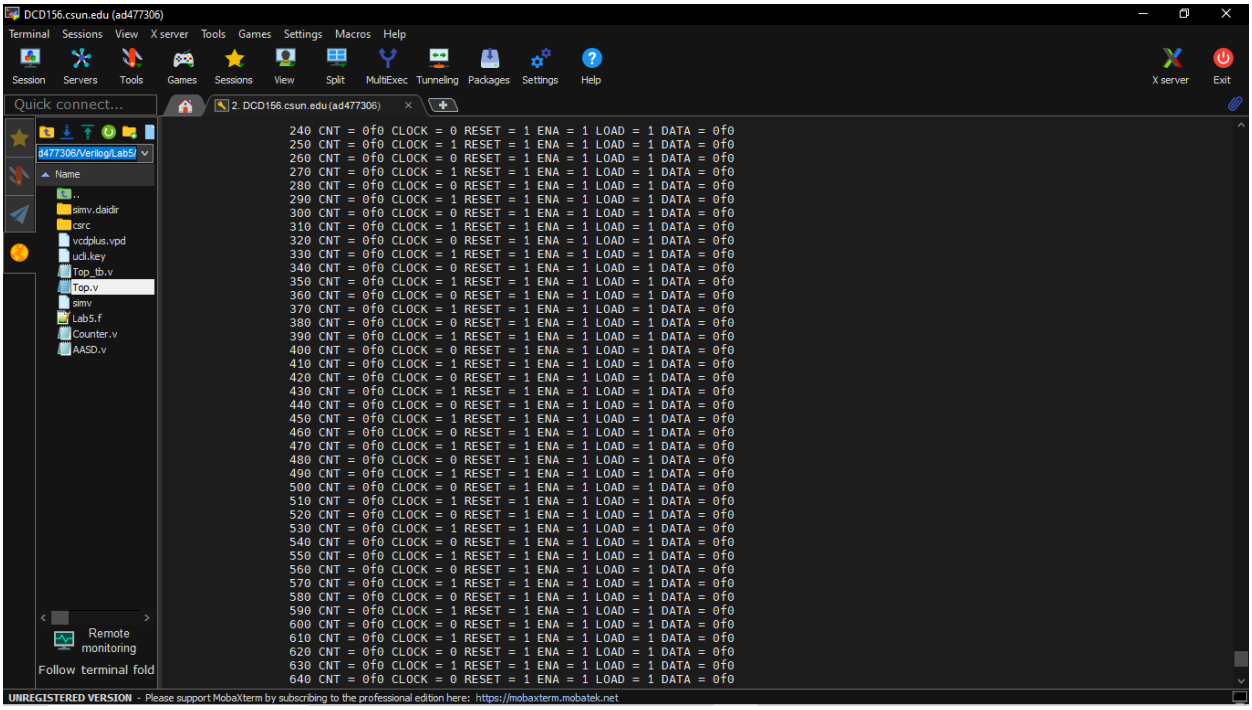
f. Part 5: Simulation

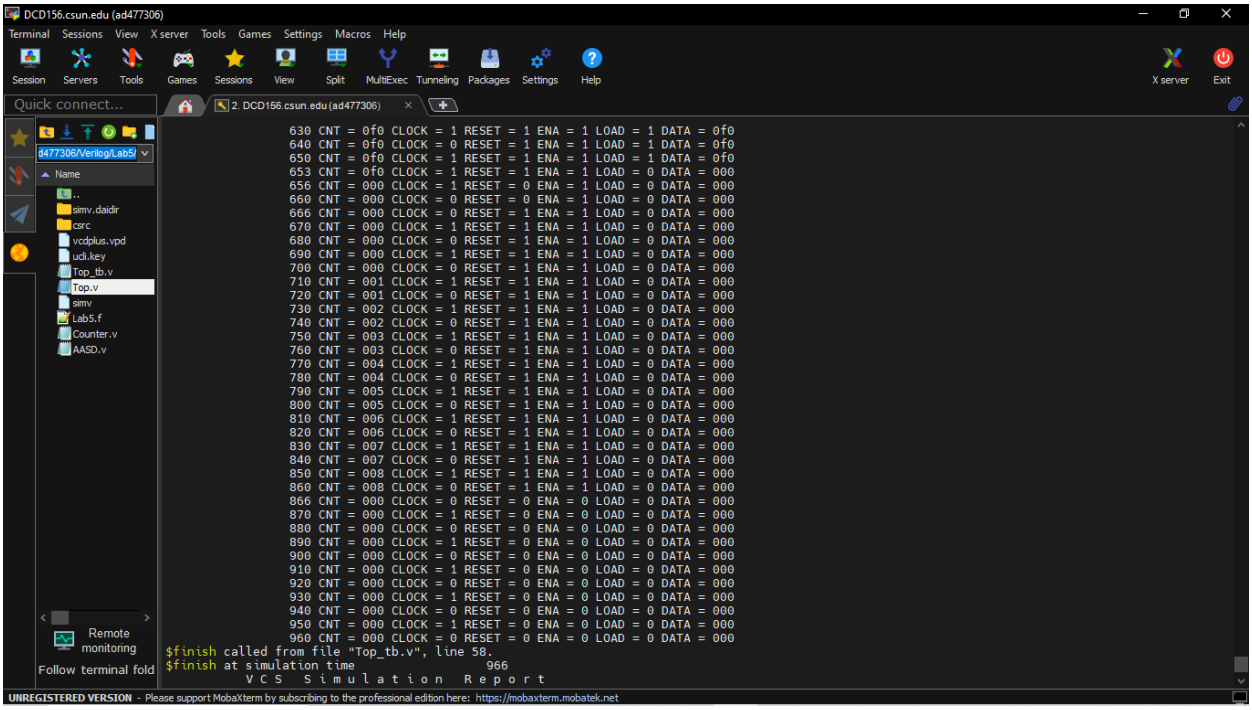
After an execution of all modules, I have run the command “simv” for simulation.





Here I have loaded 240(F0).






```
700 CNT = 000 CLOCK = 0 RESET = 1 ENA = 1 LOAD = 0 DATA = 000
710 CNT = 001 CLOCK = 1 RESET = 1 ENA = 1 LOAD = 0 DATA = 000
720 CNT = 001 CLOCK = 0 RESET = 1 ENA = 1 LOAD = 0 DATA = 000
730 CNT = 002 CLOCK = 1 RESET = 1 ENA = 1 LOAD = 0 DATA = 000
740 CNT = 002 CLOCK = 0 RESET = 1 ENA = 1 LOAD = 0 DATA = 000
```

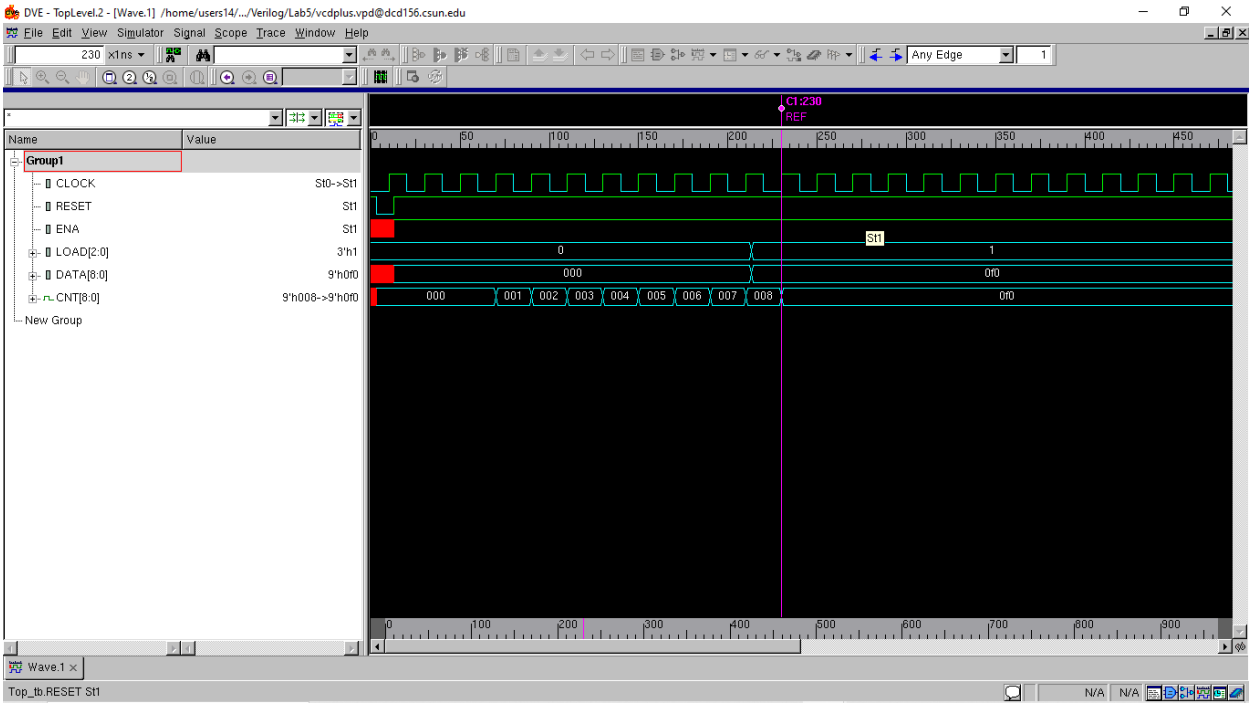
Again started counting from 1

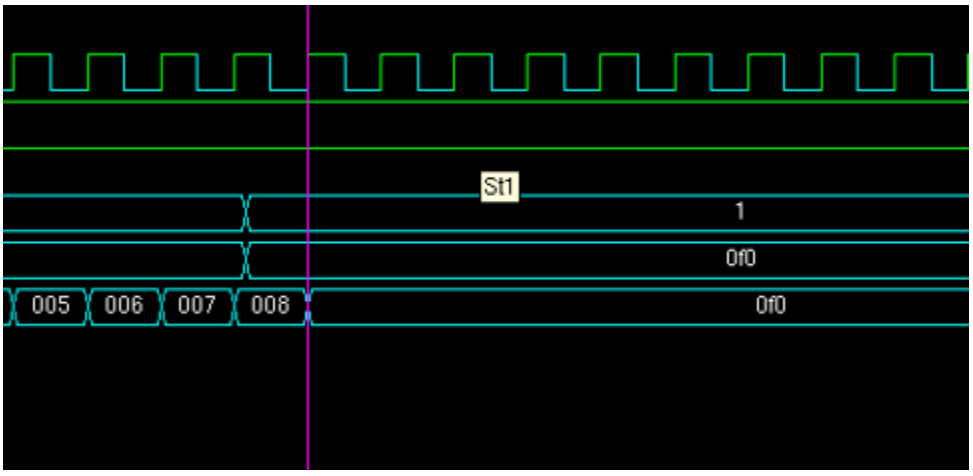
e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab5.log” command.

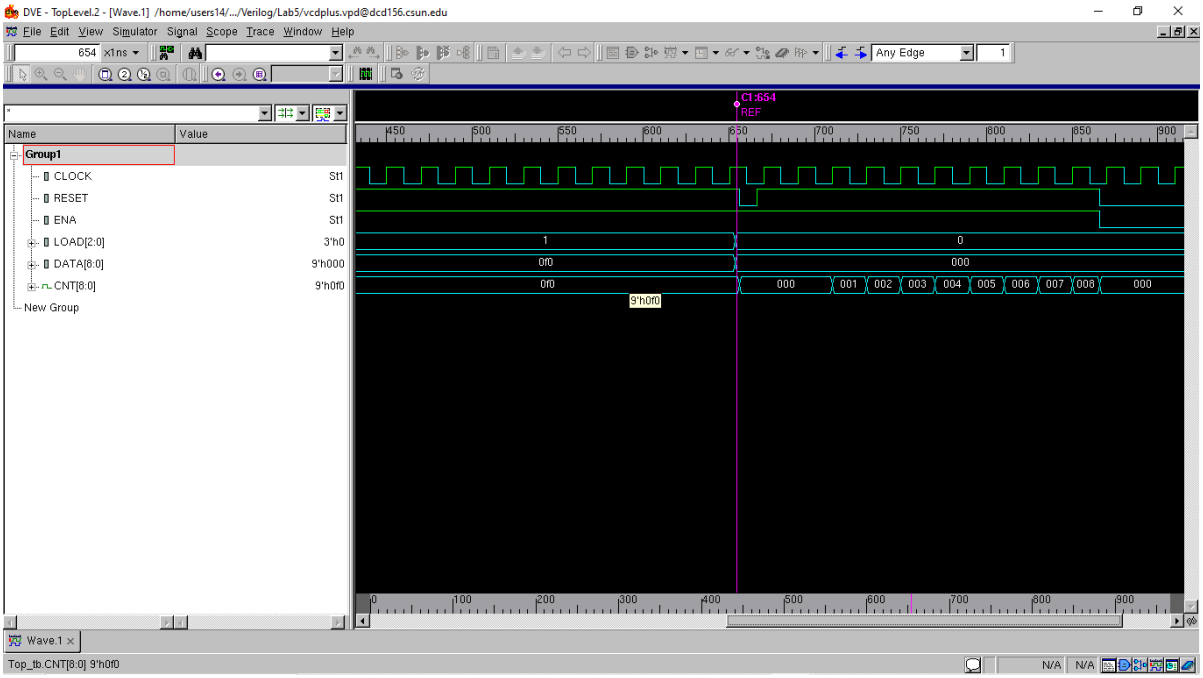
f. Part 6: Seeing the waveform.

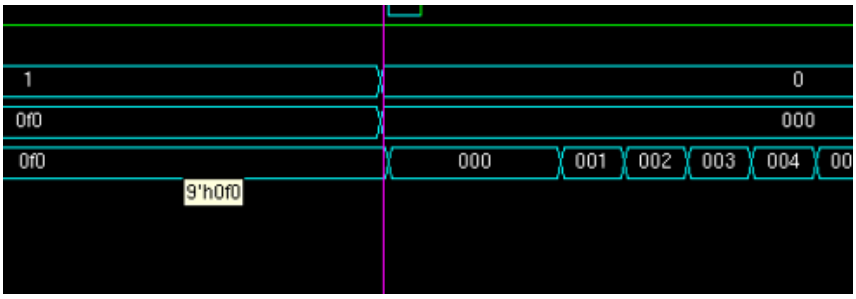
After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.



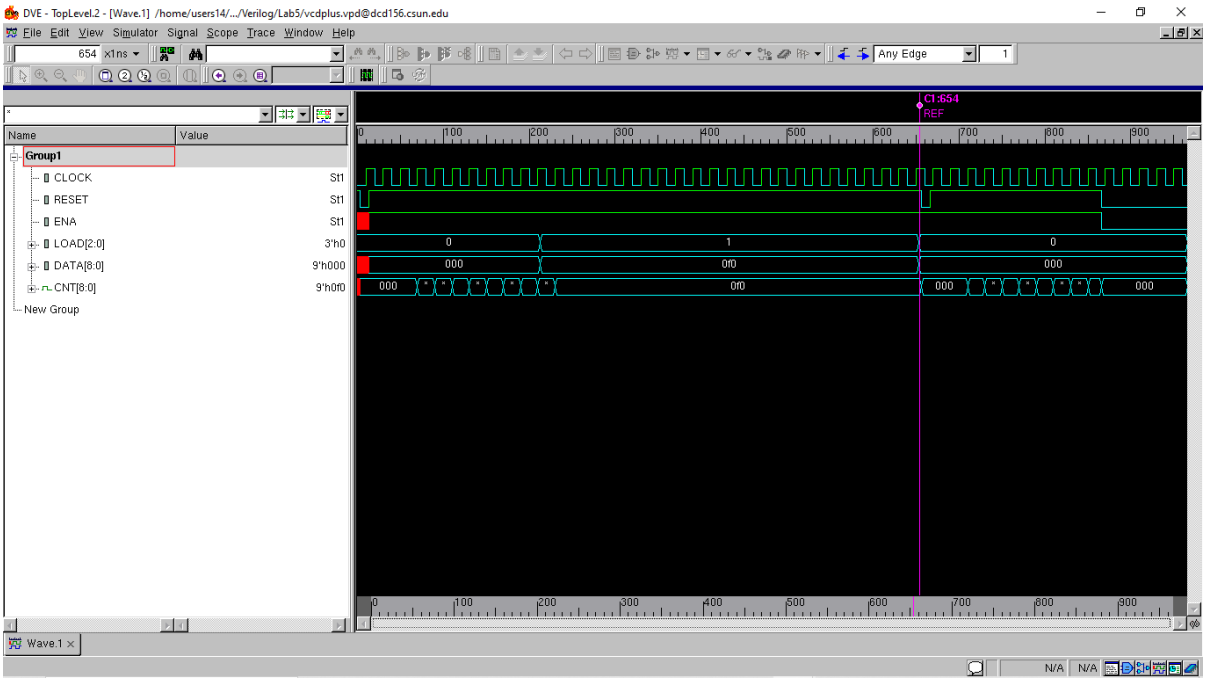


Loaded 240 .





Rolls over and starts counting form 1



Lab report question

a.If the reset was synchronous, how would the circuit behave differently?

Ans-

The reset signal would be synchronized with the clock signal, so the counter would be reset on the next clock edge after the reset signal goes low. The synchronous reset would be more predictable and easier to control, as it would not be affected by any setup or hold time violations that could occur in an asynchronous reset.

b.How would you change the code to have a defined max counter 240 and then counter rolls over (i.e. returns to zero) and then starts counting back up.

Ans –

Here I just loaded the 240 decimal value in Data and reset was already high so it stated counting from 240(F0).

After 440 ns I Loaded Data 0 and set RESET to 0 then is started counting from 1 again

Conclusion:

The behaviorally modeled 8-bit counter was verified of its functions which included the ENABLE, LOAD, and RST. The asynchronous assert, synchronous de-assert function was also successfully implemented for the counter's reset line. The counter also demonstrated a bit overflow situation and its resolution to wrapping back to the zero value. Finally, the counter also demonstrated the priority of the asynchronous reset over the other inputs.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 19-March-2023