California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 2 Report

By

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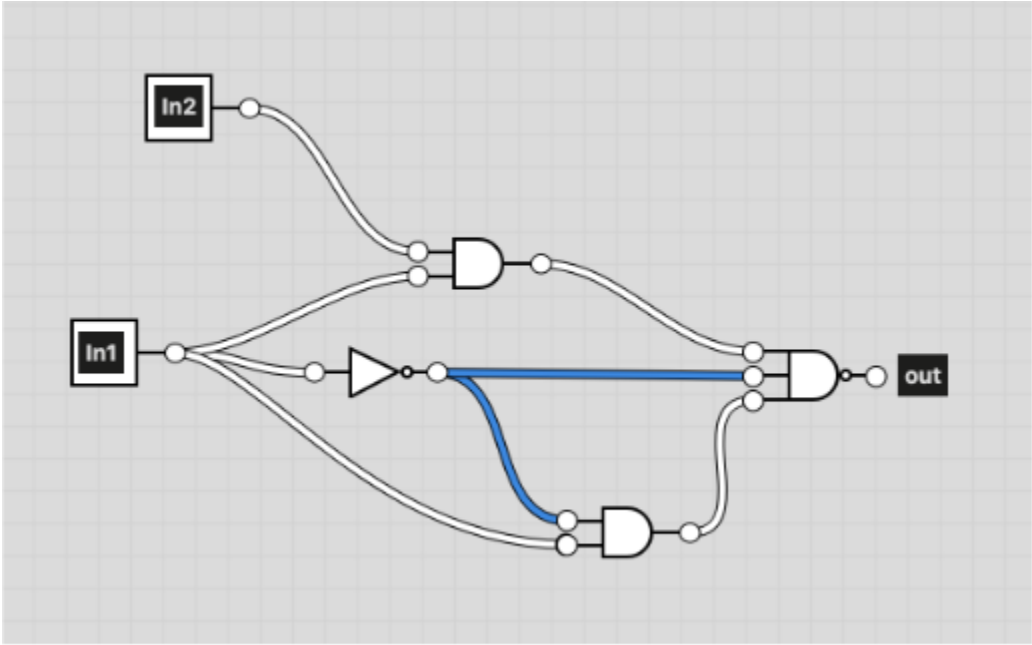
1: Introduction

The objective of this lab is to build a below circuit with two inputs and one output using AND, NOT and NAND gates which uses delays for primitives. And changing the delays later on to see how it affects the waveforms.



Here initially all the delays are 0 ns.

Truth table

The truth table of the given circuit is given below for given test cases . Here we are using two inputs(In1,In2) which produces one output (out).

In1	In2	out
0	0	1
0	1	1
1	0	1
1	1	1

2: Procedure

a. Part 1: Creating Lab2_1 Module

In this lab I have created a module given circuit . Inside the module I have assigned “In1”,”In2” as input variables and “out” as output variables. Then I performed “AND”,”NOT” and “NAND” operations. According to the circuit given in the diagram . After completing the code I ended the module using and saved the file with name “Lab2_1.v”.

b. Part 2: Creating Lab2_1_tb Module

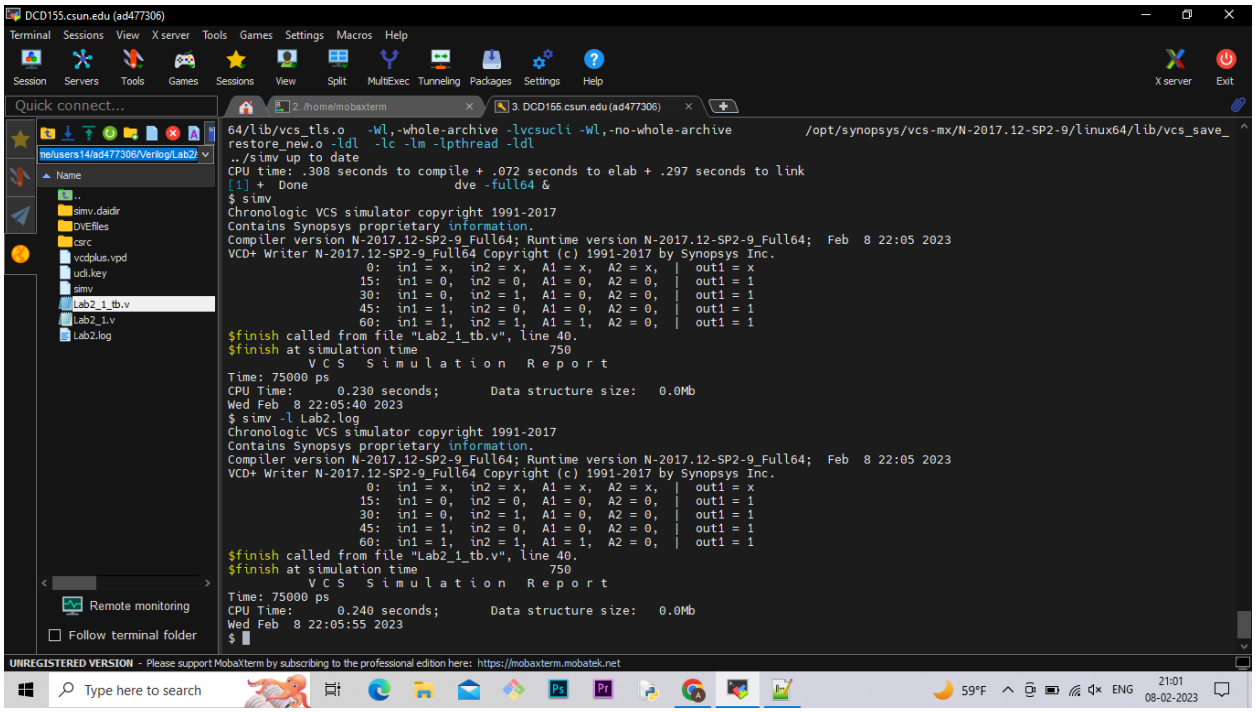
I have written the testbench for the Lab2_1 module code after creating my module. We require testbench just to make sure that the module we have created is working properly. In this lab, I have written the testbench and saved the file as “Lab2_1_tb.v”.

c. Part 3: Checking the Lab2_1 and Test Bench Module

After completing the Lab2_1 module and testbench module , we have to check if the code is running properly or not. To make sure that the code is running perfectly or not I have run the VCS command followed by the Lab2_1.v and Lab2_1_tb.v module. I have used the command “vcs -debug -full64 Lab2_1.v Lab2_1_tb.v” and checked if any error occurs. I found one error in the code, with the help of the “gedit” command. I edited the code and re-run again. This time code executed without any error.

d. Part 4: Simulation

After completing the code and testbench for Lab2_1 I have run the command “simv” for simulation.

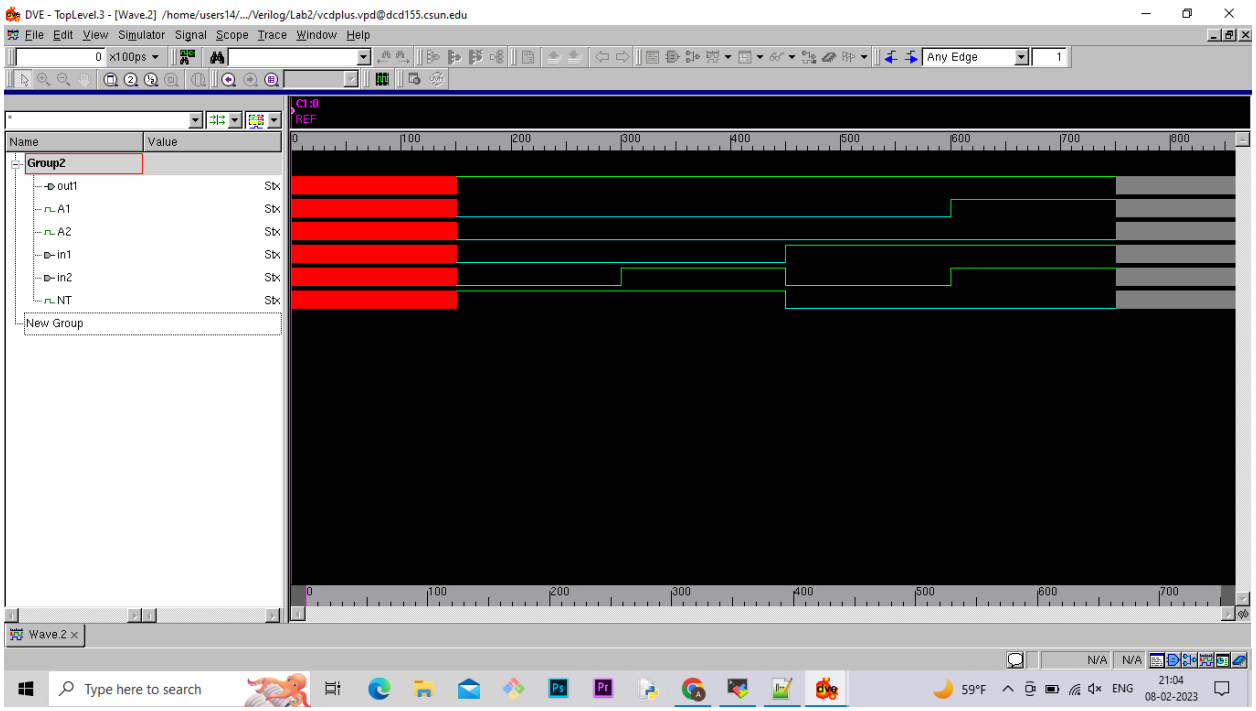


e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab2.log” command.

f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveform.

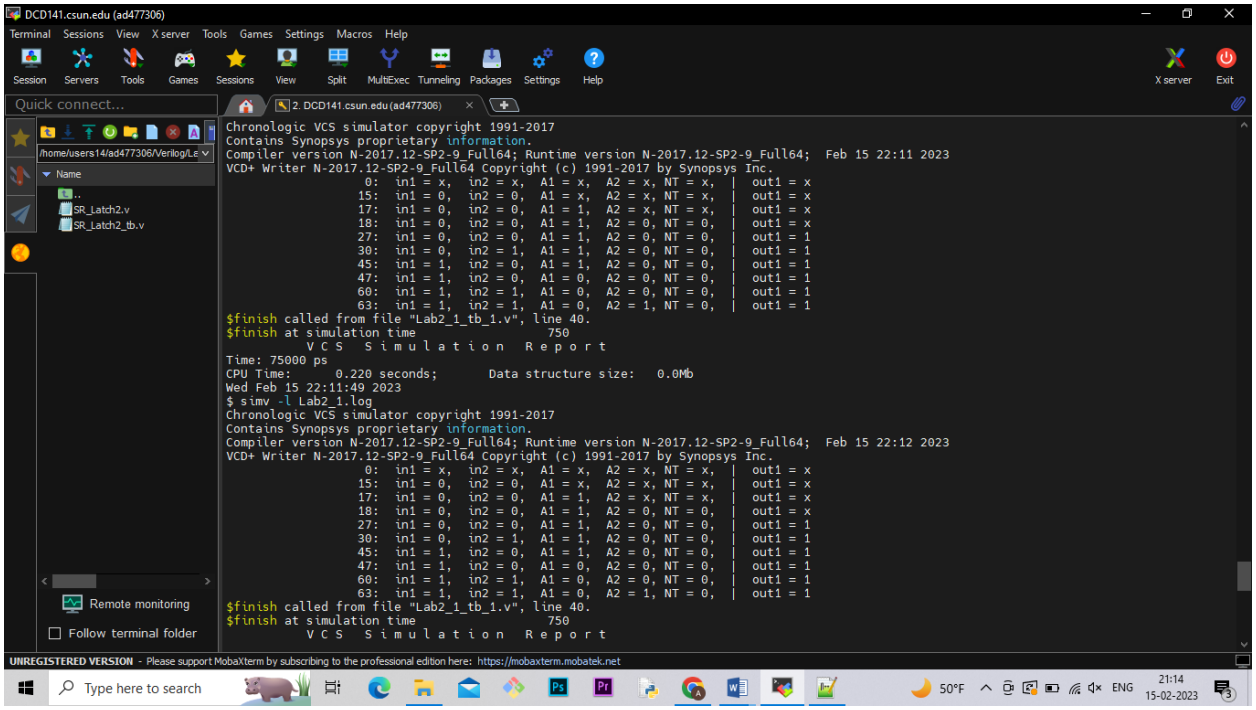


Part 2 With Changes in delays.

Primary_out	5ns
Fan_out_1	0.5ns
Fan_out_2	1ns
Fan_out_3	1.5ns
Time_delay_1	1ns
Time_delay_2	2ns
Time_delay_3	4ns
Time_delay_4 (4 input gate)	5ns

Here I repeated all the steps I did in the first part without delays. And the results i got are as follows:

Simulation :


DCD141.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
X server Exit
Quick connect...
2. DCD141.csun.edu (ad477306)
/home/users14/ad477306/Verilog/Le
Name
SR_Latch2.v
SR_Latch2_tb.v
Remote monitoring
Follow terminal folder
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64; Feb 15 22:11 2023
VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
0: in1 = x, in2 = x, A1 = x, A2 = x, NT = x, | out1 = x
15: in1 = 0, in2 = 0, A1 = x, A2 = x, NT = x, | out1 = x
17: in1 = 0, in2 = 0, A1 = 1, A2 = x, NT = x, | out1 = x
18: in1 = 0, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = x
27: in1 = 0, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = 1
30: in1 = 0, in2 = 1, A1 = 1, A2 = 0, NT = 0, | out1 = 1
45: in1 = 1, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = 1
47: in1 = 1, in2 = 0, A1 = 0, A2 = 0, NT = 0, | out1 = 1
60: in1 = 1, in2 = 1, A1 = 0, A2 = 0, NT = 0, | out1 = 1
63: in1 = 1, in2 = 1, A1 = 0, A2 = 1, NT = 0, | out1 = 1
$finish called from file "Lab2_1_tb_1.v", line 40.
$finish at simulation time 750
VCS Simulation Report
Time: 75000 ps
CPU Time: 0.220 seconds; Data structure size: 0.0Mb
Wed Feb 15 22:11:49 2023
$ simv -l Lab2_1.log
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64; Feb 15 22:12 2023
VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
0: in1 = x, in2 = x, A1 = x, A2 = x, NT = x, | out1 = x
15: in1 = 0, in2 = 0, A1 = x, A2 = x, NT = x, | out1 = x
17: in1 = 0, in2 = 0, A1 = 1, A2 = x, NT = x, | out1 = x
18: in1 = 0, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = x
27: in1 = 0, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = 1
30: in1 = 0, in2 = 1, A1 = 1, A2 = 0, NT = 0, | out1 = 1
45: in1 = 1, in2 = 0, A1 = 1, A2 = 0, NT = 0, | out1 = 1
47: in1 = 1, in2 = 0, A1 = 0, A2 = 0, NT = 0, | out1 = 1
60: in1 = 1, in2 = 1, A1 = 0, A2 = 0, NT = 0, | out1 = 1
63: in1 = 1, in2 = 1, A1 = 0, A2 = 1, NT = 0, | out1 = 1
$finish called from file "Lab2_1_tb_1.v", line 40.
$finish at simulation time 750
VCS Simulation Report
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net
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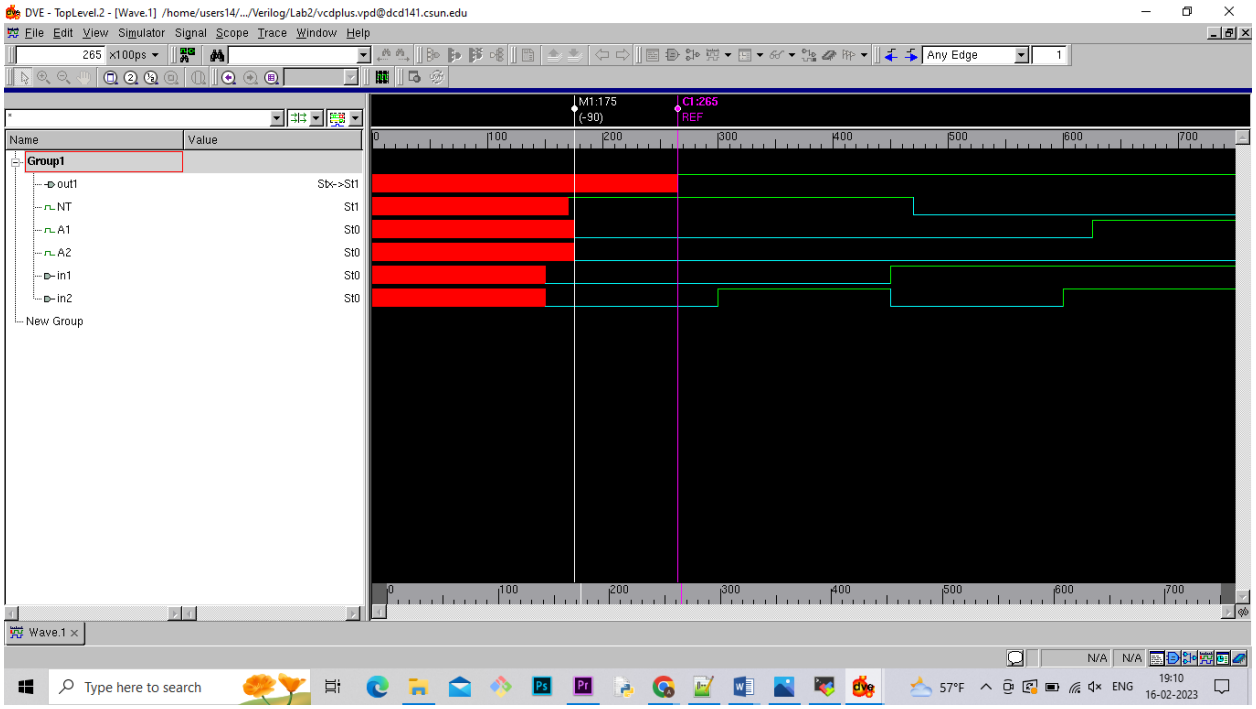
15-02-2023

Waveform :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Any Edge
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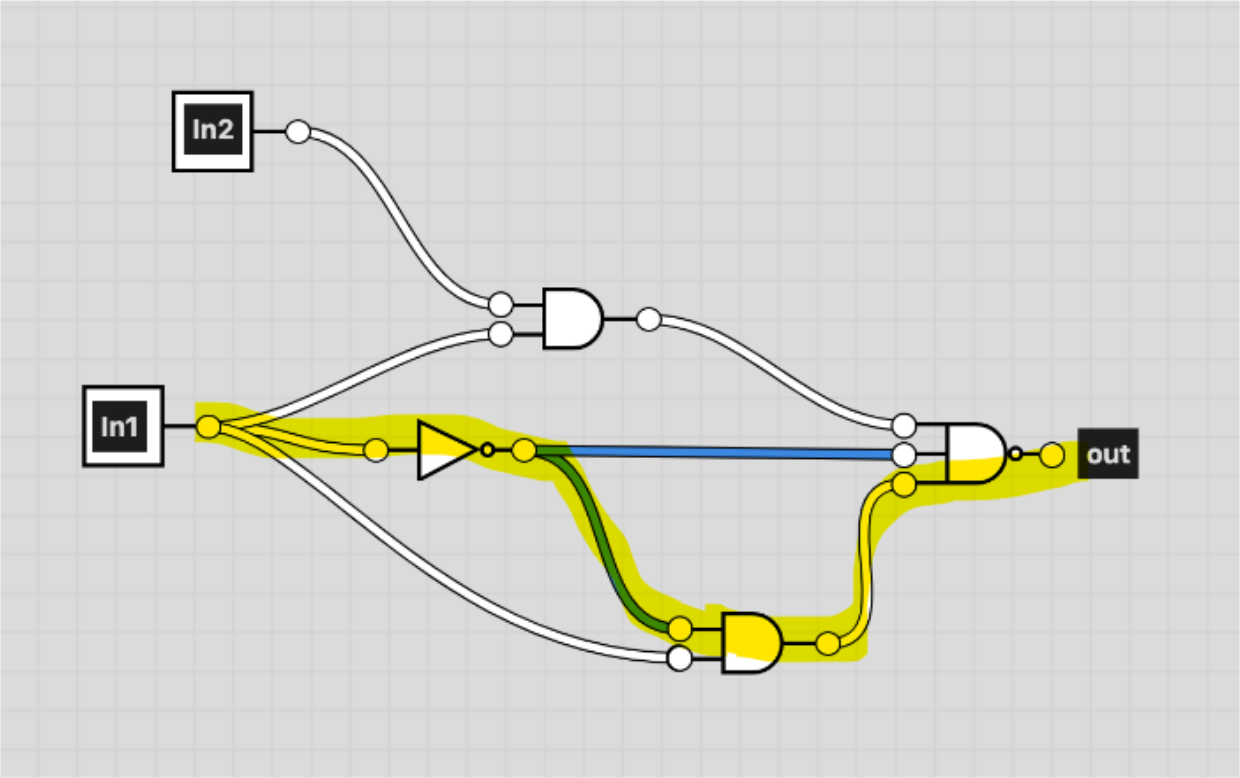
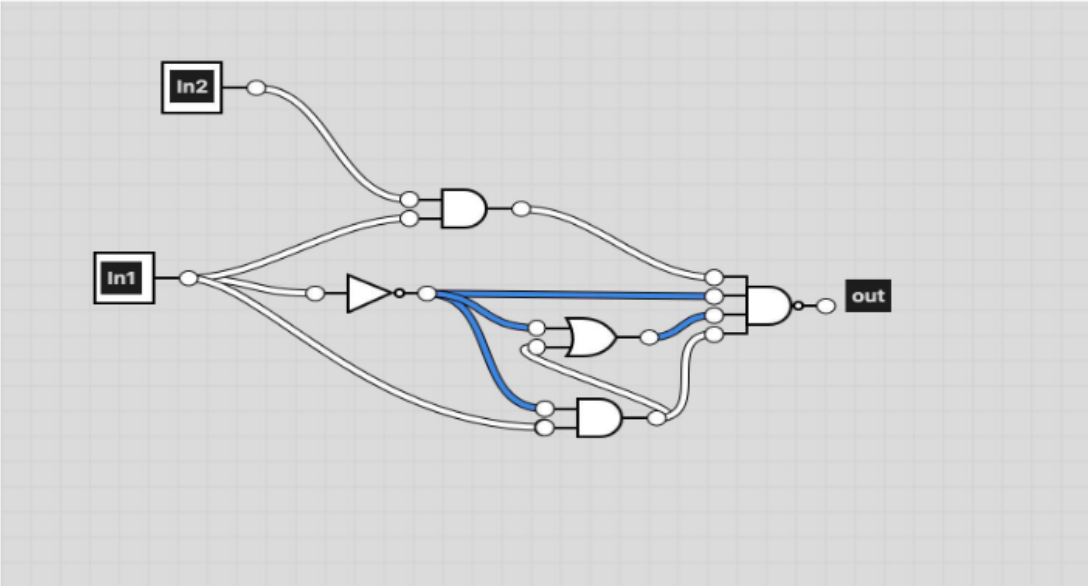
16-02-2023

Lab report question: What's the critical path (longest delay) of this design?



The critical path for this circuit with delays is highlighted .
The longest delay is 13.5 ns

Part 3 : New Circuit



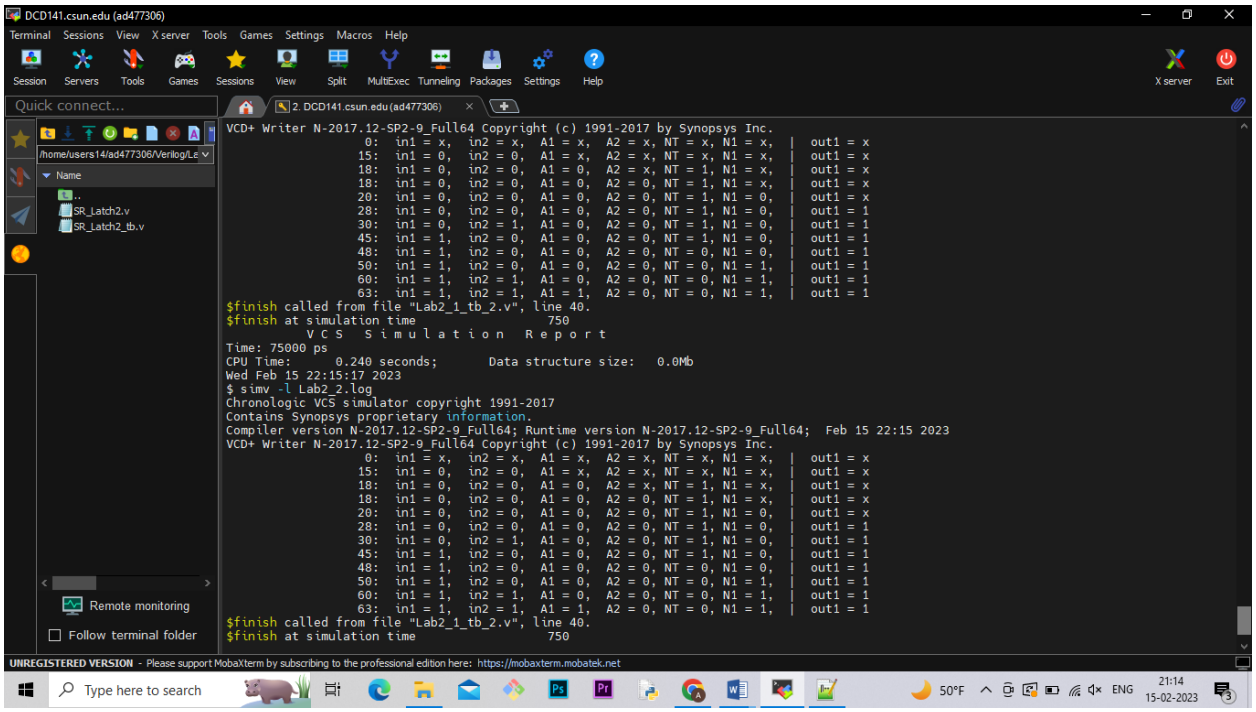
Here in the new circuit there is addition of one NOR gate which takes inputs from the previous AND(A2) and NOT(NT) gate which will be further added to the final NAND gate to get output.

Truth table

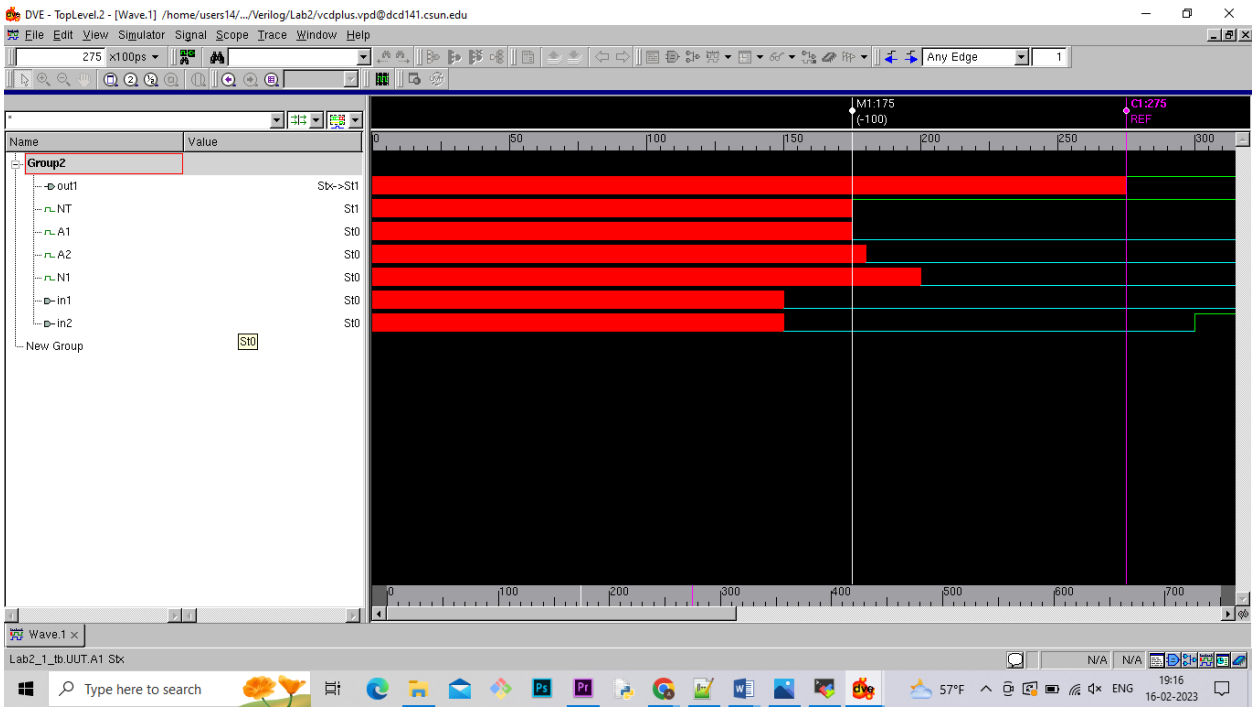
The truth table of the new circuit is given below for given test cases . Here we are using two inputs(In1,In2) which produces one output (out1).

In1	In2	out1
0	0	1
0	1	1
1	0	1
1	0	1
1	0	1
1	0	1
1	1	1
1	1	1

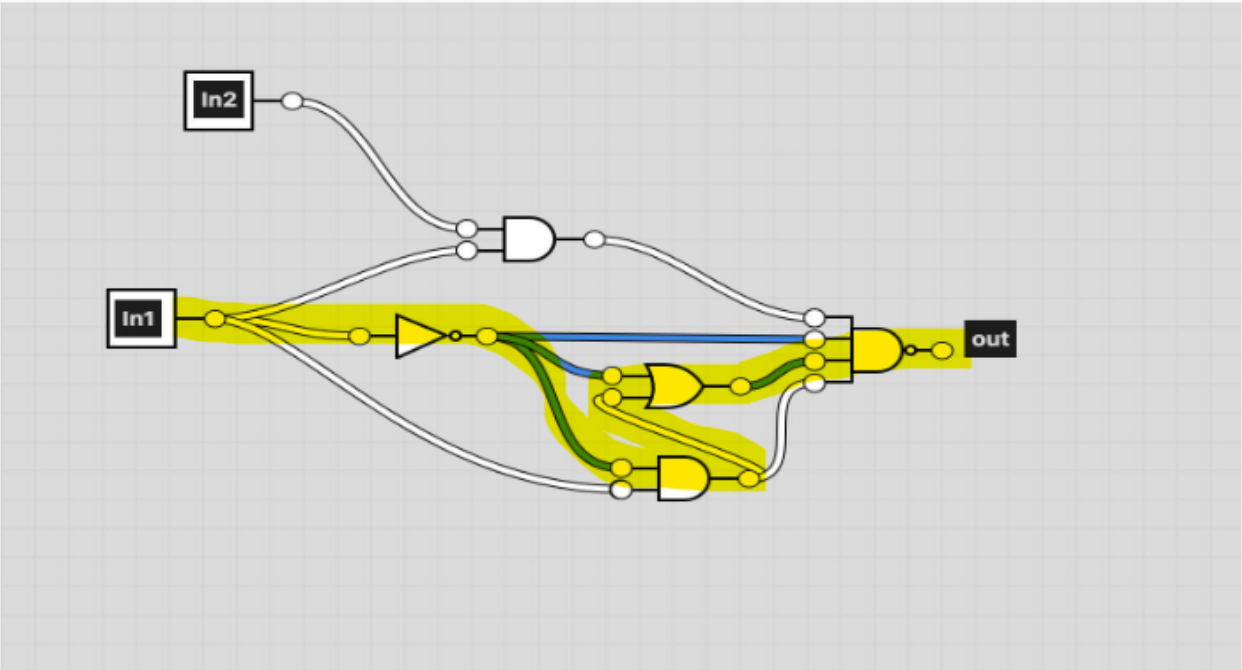
Simulation :



Waveform :



Lab report question: What's the critical path (longest delay) of this new design?



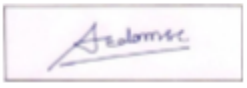
The critical path for this circuit with delays is highlighted .
The longest delay is 18 ns

Conclusion :

In this lab I learned how to design circuit diagrams with given inputs and some gates in verilog . This lab taught me how to calculate the longest delay in any circuit diagram . And how slight change in the delays changes the waveforms.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 14-02-2023