California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 10 Report

By

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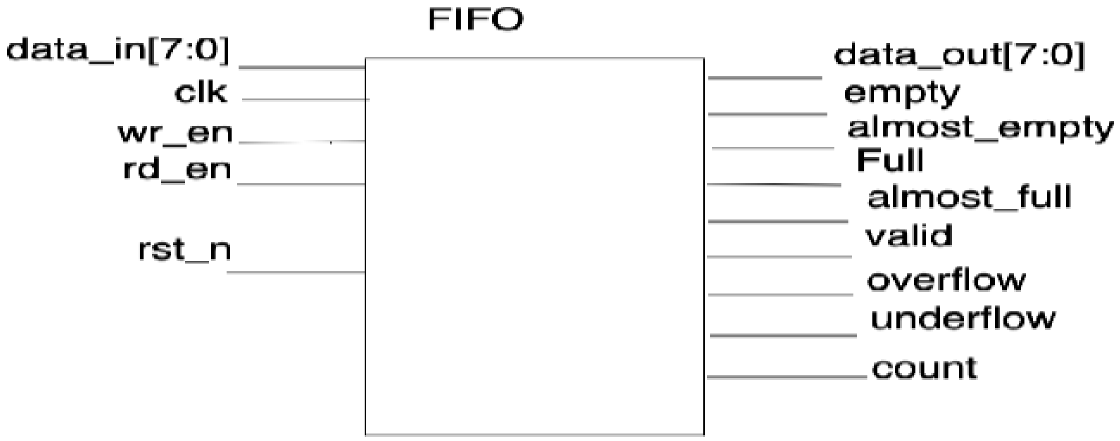
1: Introduction

The objective of this lab a parameterized synchronous FIFO .

Here we have to use following diagram to build FIFO.



2: Procedure

a. Part 1: Creating FIFO Module

In this lab I have created a FIFO module. Inside the module I have assigned “CLK, reset, wr_enable,wr_data and rd_enable ” as input variables and “empty and full” as output variable and CF, OF, SF, ZF,rd_data, count as an output variables. Then I wrote the FIFO. After completing the code I ended the module using and saved the file with name “FIFO.v”.

b. Part 4: Creating FIFO_tb Testbench

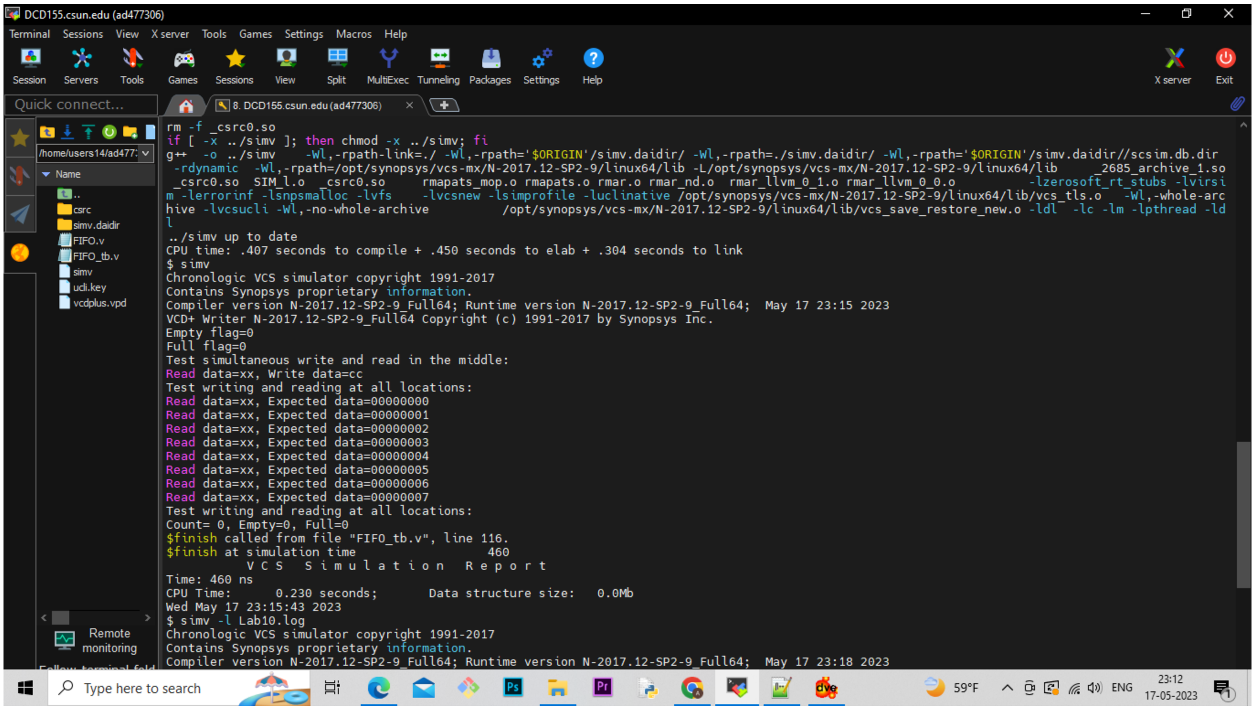
I have written the test bench for the **FIFO** module. We require test bench just to make sure that the module we have created is working properly.

c. Part 3: execution.

Using “vcs -debug -full64 FIFO.v FIFO_tb.v” command I executed testbench file.

d. Part 4: Simulation

After an execution of all modules, I have run the command “simv” for simulation.


DCD155.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help X server Exit
Quick connect...
8. DCD155.csun.edu (ad477306)
/home/users14/ad477
Name
..
csrc
simv.daidir
FIFO.v
FIFO_tb.v
simv
ucli.key
vcdplus.vpd
Remote monitoring
Type here to search
59°F ENG 23:12 17-05-2023

```
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir
 -rdynamic  -Wl,-rpath=/opt/synopsys/vcs-mx/N-2017.12-SP2-9/linux64/lib -L/opt/synopsys/vcs-mx/N-2017.12-SP2-9/linux64/lib     _2685_archive_1.so
 _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsi
m -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /opt/synopsys/vcs-mx/N-2017.12-SP2-9/linux64/lib/vcs_tls.o   -Wl,-whole-arc
hive -lvcsucli -Wl,-no-whole-archive         /opt/synopsys/vcs-mx/N-2017.12-SP2-9/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ld
l
../simv up to date
CPU time: .407 seconds to compile + .450 seconds to elab + .304 seconds to link
$ simv
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64;  May 17 23:15 2023
VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
Empty flag=0
Full flag=0
Test simultaneous write and read in the middle:
Read data=xx, Write data=cc
Test writing and reading at all locations:
Read data=xx, Expected data=00000000
Read data=xx, Expected data=00000001
Read data=xx, Expected data=00000002
Read data=xx, Expected data=00000003
Read data=xx, Expected data=00000004
Read data=xx, Expected data=00000005
Read data=xx, Expected data=00000006
Read data=xx, Expected data=00000007
Test writing and reading at all locations:
Count= 0, Empty=0, Full=0
$finish called from file "FIFO_tb.v", line 116.
$finish at simulation time                  460
           V C S   S i m u l a t i o n   R e p o r t
Time: 460 ns
CPU Time:      0.230 seconds;       Data structure size:   0.0Mb
Wed May 17 23:15:43 2023
$ simv -l Lab10.log
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64;  May 17 23:18 2023
```

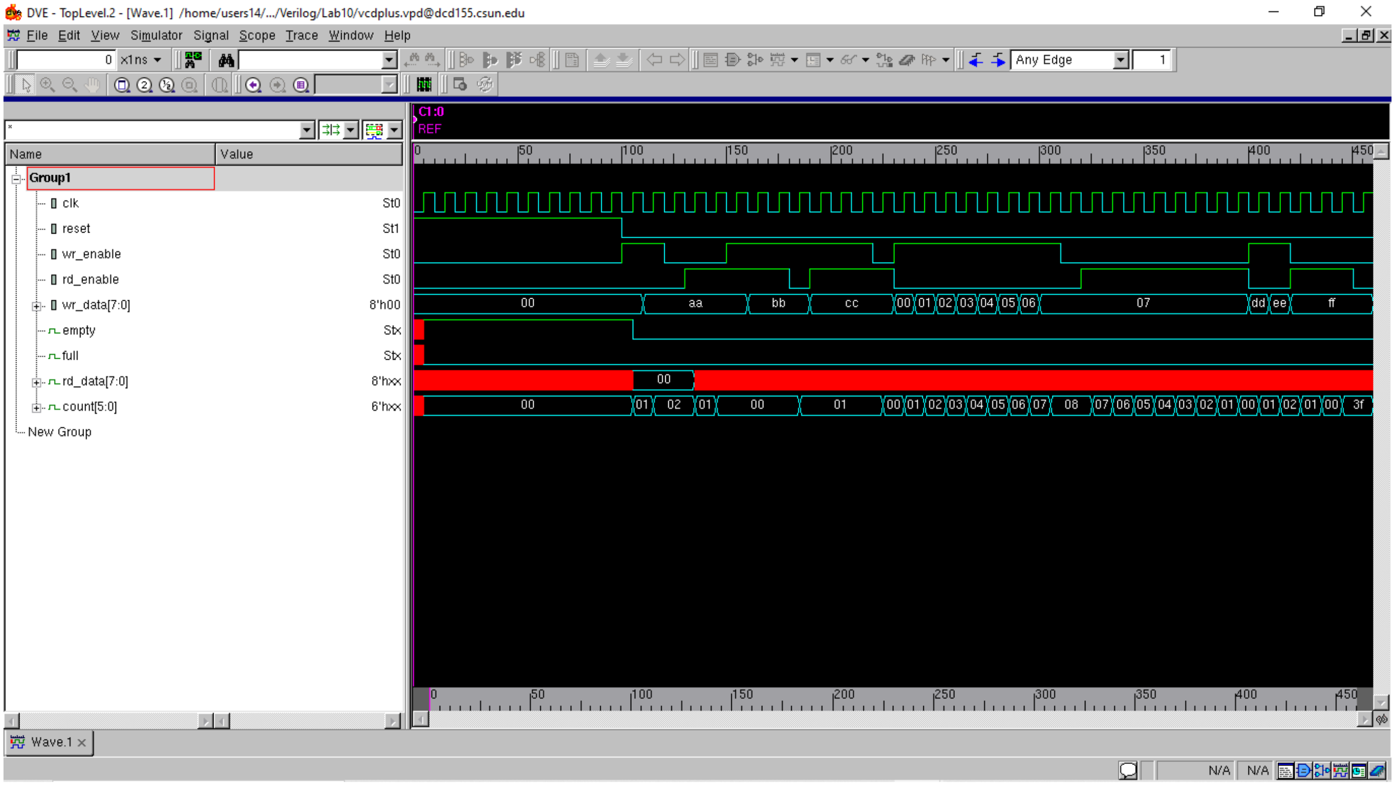
e. Part 5: Creating Log File

After running the simulation I created the log file for first stategy using the “simv -l Lab8_non_exh.log” command

```
Command: /home/users14/ad477306/Verilog/Lab10/./simv -l Lab10.log
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64;  May 17 23:18
2023
VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
Empty flag=0
Full flag=0
Test simultaneous write and read in the middle:
Read data=xx, Write data=cc
Test writing and reading at all locations:
Read data=xx, Expected data=00000000
Read data=xx, Expected data=00000001
Read data=xx, Expected data=00000002
Read data=xx, Expected data=00000003
Read data=xx, Expected data=00000004
Read data=xx, Expected data=00000005
Read data=xx, Expected data=00000006
Read data=xx, Expected data=00000007
Test writing and reading at all locations:
Count= 0, Empty=0, Full=0
$finish called from file "FIFO_tb.v", line 116.
$finish at simulation time                  460
           V C S   S i m u l a t i o n   R e p o r t
Time: 460 ns
CPU Time:      0.230 seconds;       Data structure size:   0.0Mb
Wed May 17 23:18:09 2023
```

f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.


DVE - TopLevel.2 - [Wave.1] /home/users14/.../Verilog/Lab10/vcdplus.vpd@dcd155.csun.edu
File Edit View Simulator Signal Scope Trace Window Help
Any Edge
C1:0
REF
Name
Value
Group1
clk St0
reset St1
wr_enable St0
rd_enable St0
wr_data[7:0] 8'h00
empty StX
full StX
rd_data[7:0] 8'hxx
count[5:0] 6'hxx
New Group
0 50 100 150 200 250 300 350 400 450
00 aa bb cc 00 01 02 03 04 05 06 07 dd ee ff
00
00 01 02 01 00 01 00 01 02 03 04 05 06 07 08 07 06 05 04 03 02 01 00 01 02 01 00 3f
Wave.1
N/A N/A

Conclusion:

The constructed ALU unit in this experiment was verified of its functionalities. Using testbench I have successfully tested the FIFo functionality.

Extra Credit:

To modify the FIFO module to be asynchronous, you can remove the clock (clk) signal and the posedge clk sensitivity in the always blocks. Additionally, you can change the reset behavior to be asynchronous.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed) ADamse

Date : 14-May-2023