California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 6 Report

By

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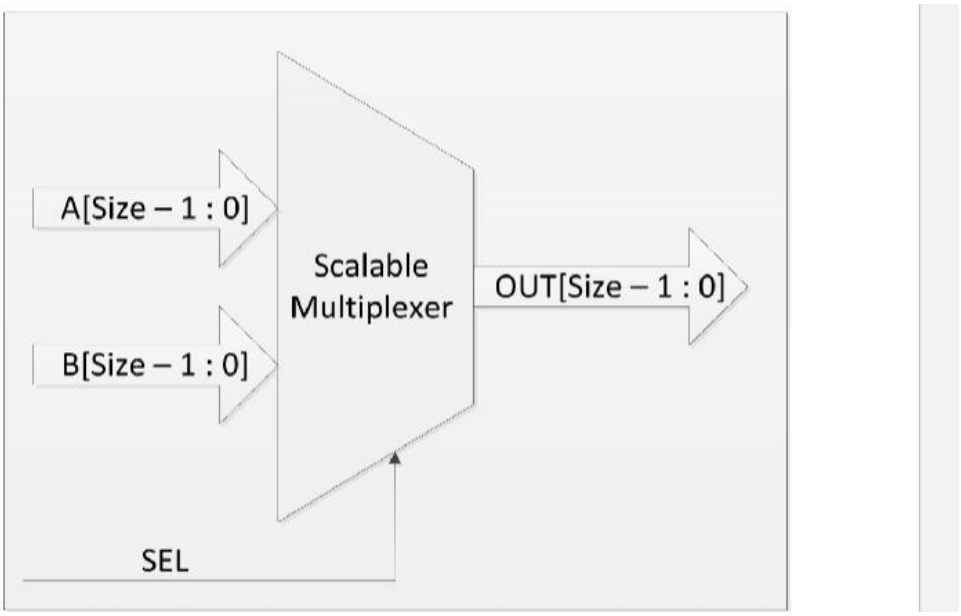
1: Introduction

The objective of this lab is to build Verilog model for a scalable multiplexer using behavioral Verilog and Familiarization with instance-by-instance parameter specification.

Here we have to use following diagram to build scalable multiplexer.



2: Procedure

a. Part 1: Creating mux Module

In this lab I have created a mux module for scalable multiplexer. Inside the module I have assigned “A, B and SEL,” as input variables and “OUT” as output variables. Then I wrote the scalable multiplexter logic inside module. After completing the code I ended the module using and saved the file with name “mux.v”.

b. Part 2: Creating mux_tb Module

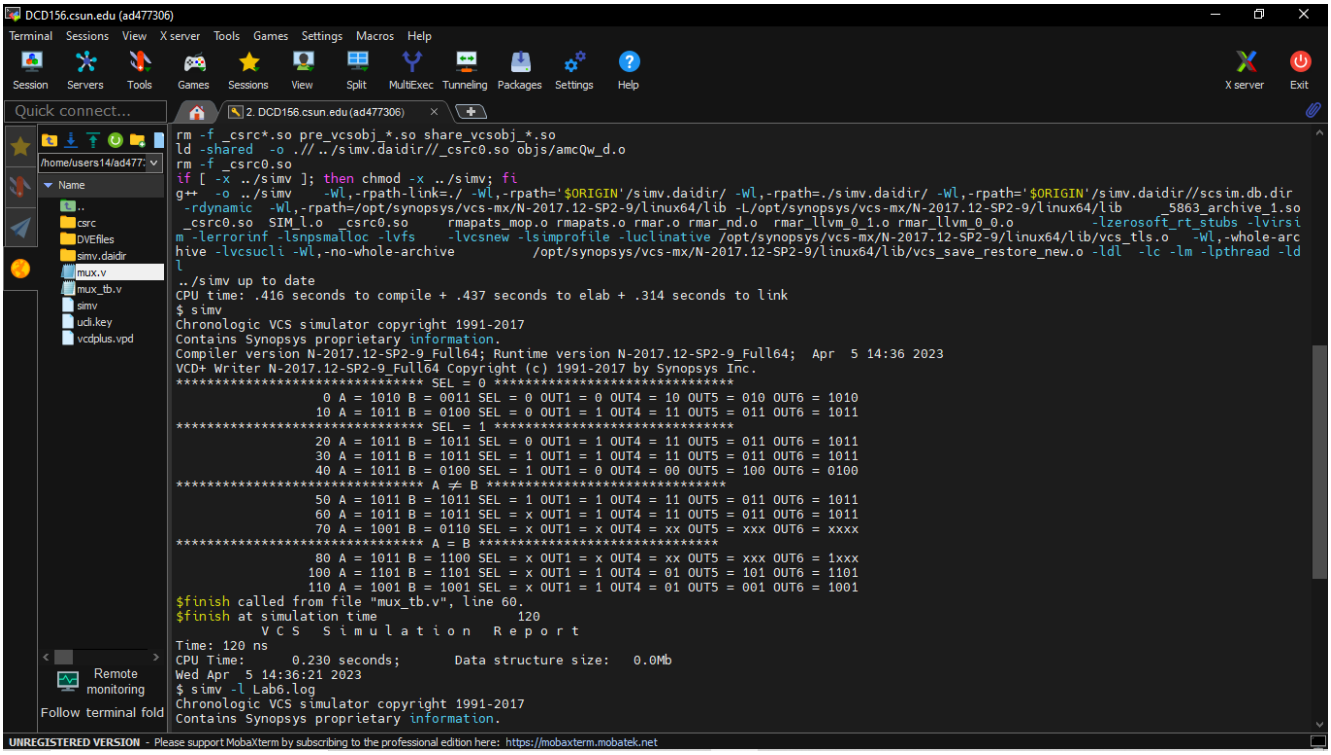
I have written the test bench for the mux module.We require test bench just to make sure that the module we have created is working properly. Here, in this testbench I instantiated the mux module and wrote some test cases to check the output.

c. Part 3: execution.

Using “vcs -debug -full64 mux.v mux_tb.v” command I executed the file.

d. Part 4: Simulation

After an execution of all modules, I have run the command “simv” for simulation.



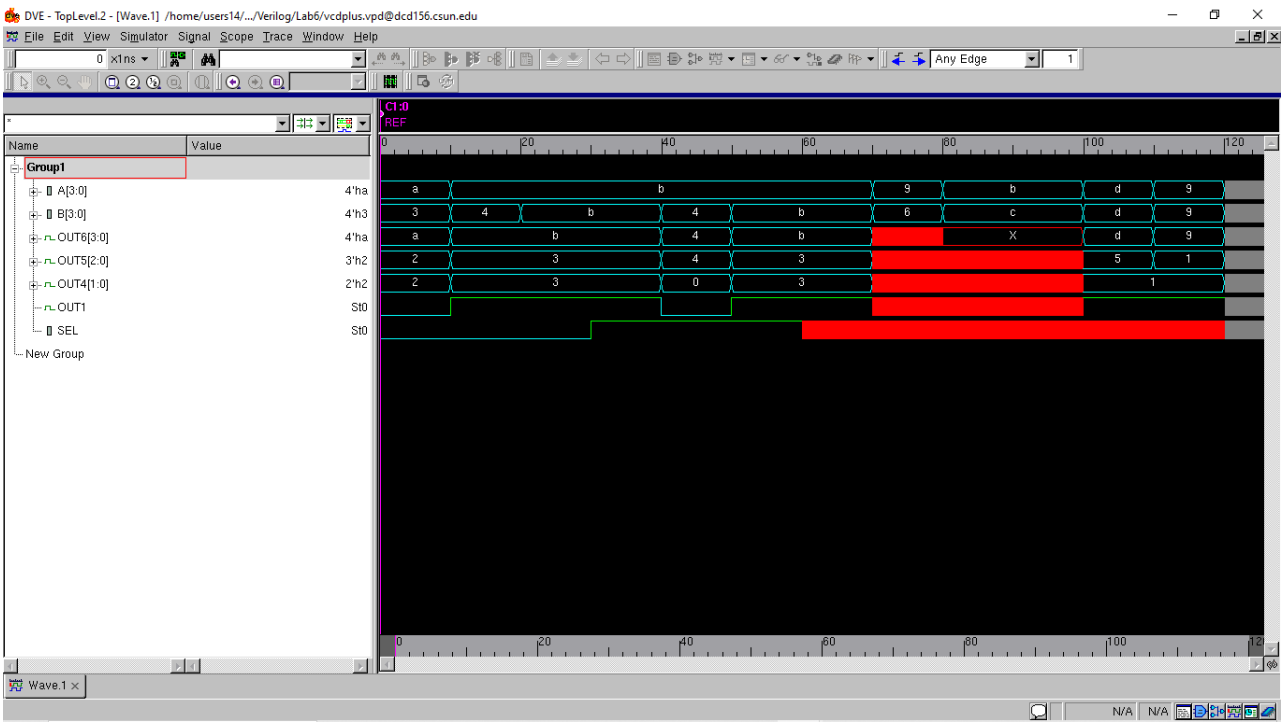
```
riter N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
************************* SEL = 0 ******************************
           0 A = 1010 B = 0011 SEL = 0 OUT1 = 0 OUT4 = 10 OUT5 = 010 OUT6 = 1010
          10 A = 1011 B = 0100 SEL = 0 OUT1 = 1 OUT4 = 11 OUT5 = 011 OUT6 = 1011
************************* SEL = 1 ******************************
          20 A = 1011 B = 1011 SEL = 0 OUT1 = 1 OUT4 = 11 OUT5 = 011 OUT6 = 1011
          30 A = 1011 B = 1011 SEL = 1 OUT1 = 1 OUT4 = 11 OUT5 = 011 OUT6 = 1011
          40 A = 1011 B = 0100 SEL = 1 OUT1 = 0 OUT4 = 00 OUT5 = 100 OUT6 = 0100
************************* A ≠ B ******************************
          50 A = 1011 B = 1011 SEL = 1 OUT1 = 1 OUT4 = 11 OUT5 = 011 OUT6 = 1011
          60 A = 1011 B = 1011 SEL = x OUT1 = 1 OUT4 = 11 OUT5 = 011 OUT6 = 1011
          70 A = 1001 B = 0110 SEL = x OUT1 = x OUT4 = xx OUT5 = xxx OUT6 = xxxx
************************* A = B ******************************
          80 A = 1011 B = 1100 SEL = x OUT1 = x OUT4 = xx OUT5 = xxx OUT6 = 1xxx
         100 A = 1101 B = 1101 SEL = x OUT1 = 1 OUT4 = 01 OUT5 = 101 OUT6 = 1101
         110 A = 1001 B = 1001 SEL = x OUT1 = 1 OUT4 = 01 OUT5 = 001 OUT6 = 1001
h called from file "mux_tb.v", line 60.
h at simulation time                  120
    V C S   S i m u l a t i o n   R e p o r t
```

e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab6.log” command.

f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.

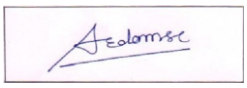


Conclusion:

The functionality of the scalable multiplexer coded in this lab was successfully verified. In addition to the normal features of a multiplexer, it has the capability to resolve conflicting bits upon setting SEL to x. The instances were also successfully created with the parameters modified according to specification.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 5-April-2023