California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 3 Report

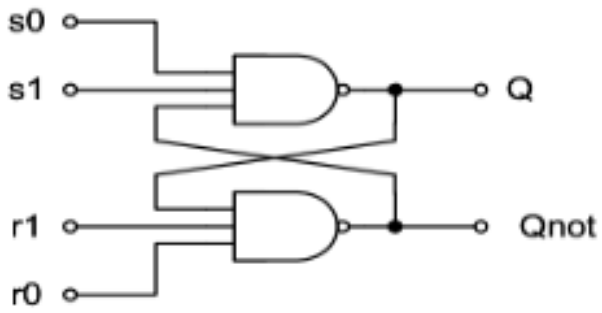
By

Avinash Damse

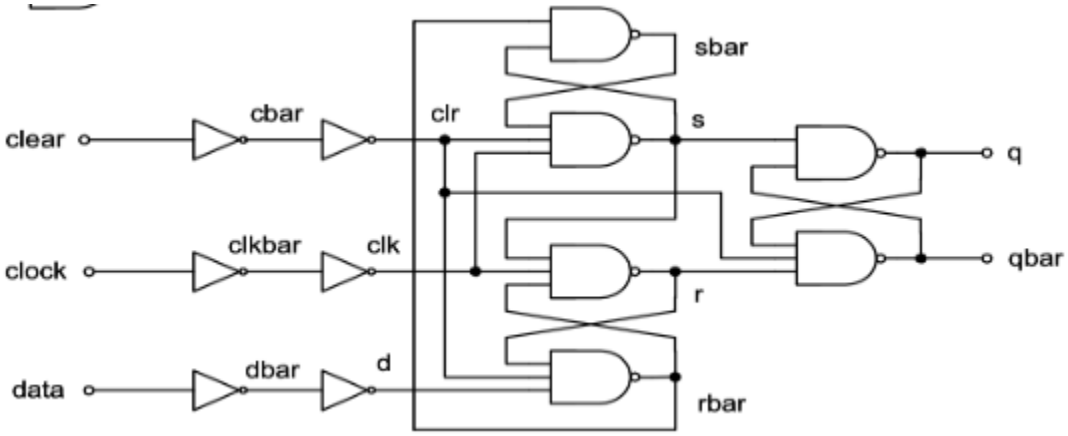
CSUN ID- 203131064

1: Introduction

The objective of this lab is to build an edge triggered D Flipflop using a hierarchical modeling approach.



Here initially we have to implement the SR Latch as shown in the figure then using hierarchical method we have to implement an edge triggered D Flipflop as shown in the below diagram.



Truth table

The D Flip-flop should function as shown in the given truth table

DATA	CLEAR	CLOCK	Q	QBAR	State
x	0	x	0	1	(Asynchronous Clear)
0	1	posedge	0	1	
1	1	posedge	1	0	
x	1	Not posedge	Q	QBAR	(No Change)

Delays : These are the delay we are going to use for this Lab

Primary_out	2.0 ns
Fan_out_1	0.5 ns
Fan_out_2	0.8 ns
Fan_out_3	1.0 ns
Time_delay_1	3 ns
Time_delay_2	4 ns
Time_delay_3	5 ns

2: Procedure

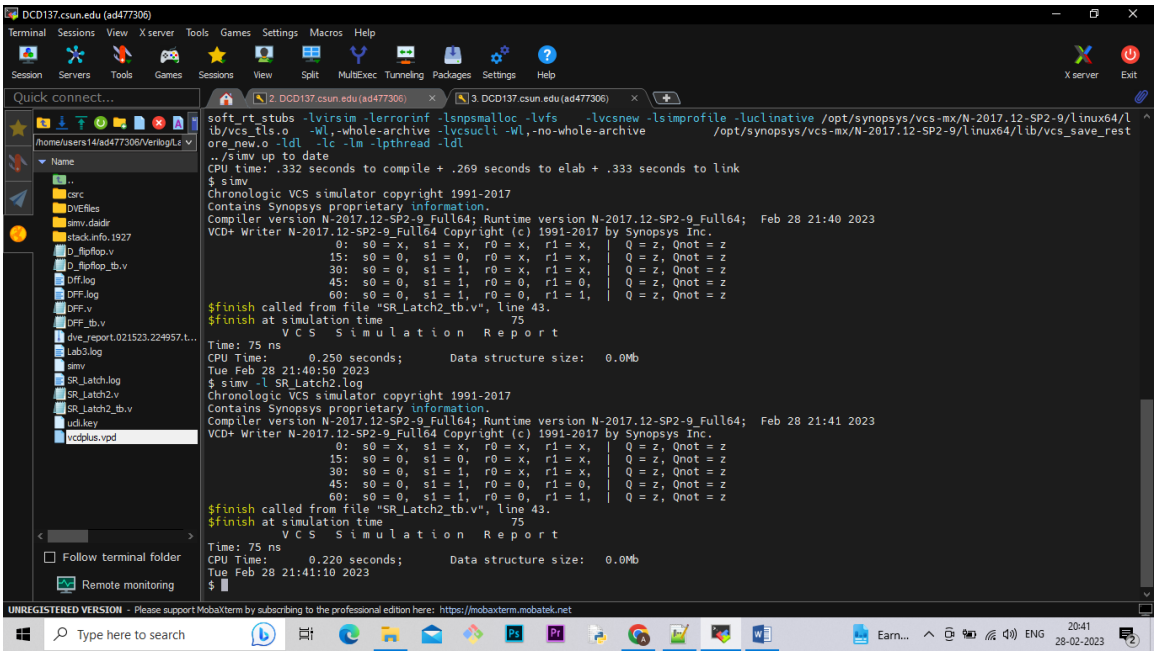
a. Part 1: Creating SR_Latch2 Module

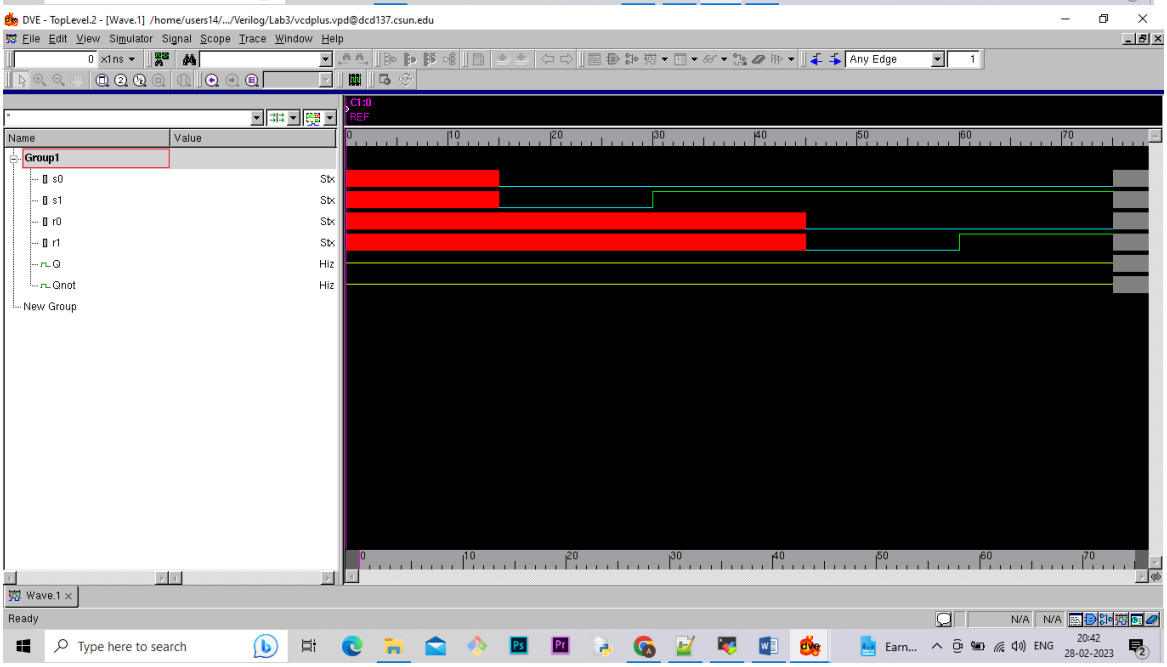
In this lab I have created a module of a given SR Latch circuit. Inside the module I have assigned “s0”,”s1”, “r0”,”r1” as input variables and “Q”,Qnot” as output variables. Then I performed two “NAND” operations. According to the circuit given in the diagram. After completing the code I ended the module using and saved the file with name “SR_Latch2.v”.

b. Part 2: Creating SRLatch2_tb Module

I have written the test bench for the SR_Latch2 module code after creating my module. We require test bench just to make sure that the module we have created is working properly. In this lab, I have written the test bench and saved the file as “SR_Latch2_tb.v”.

Simulation Of SR_Latch





c. Part 3: Creating the D Flipflop Module

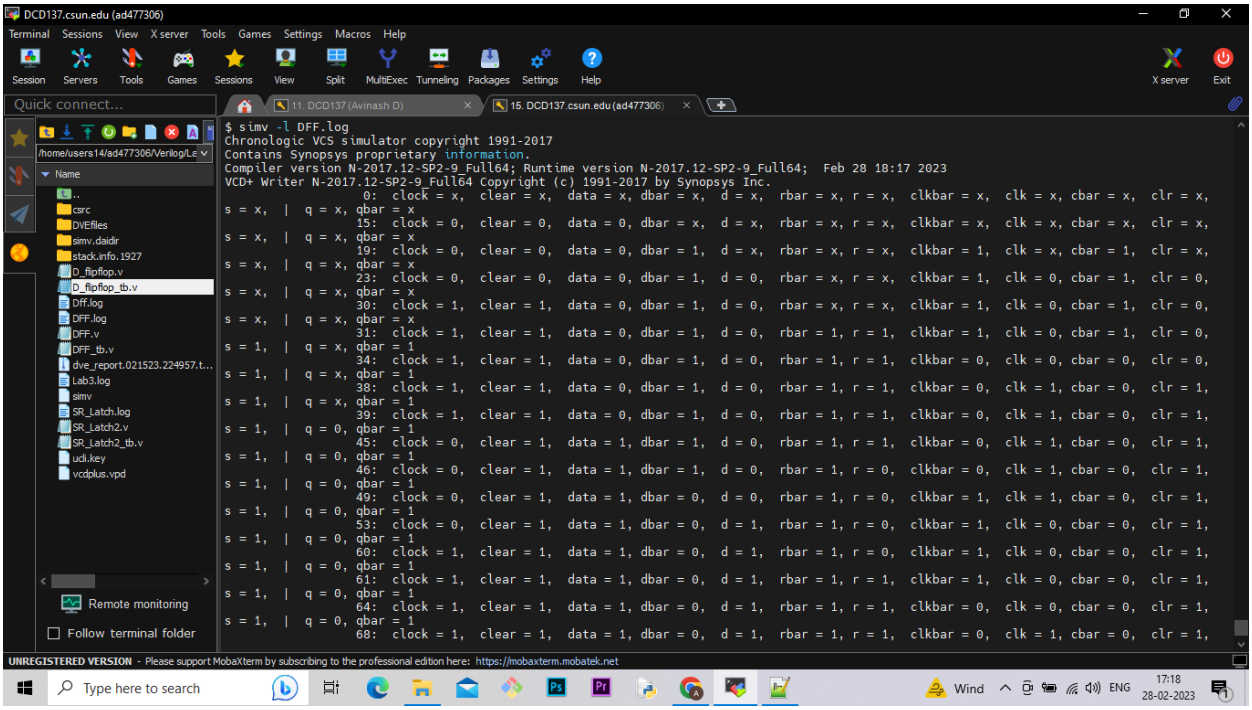
After completing the SR_Latch module and test bench module, I checked if the code is running properly or not. After making sure that SR_Latch code is working properly, I created a module of a given D Flip-flop circuit . Inside the module I have assigned “clock”, ”data”, “clear” as input variables and “q”,qbar” as output variables. Then I used SR_Latch module for 3 times using hierarchical method according to the circuit given in the diagram. After completing the code I ended the module using and saved the file with name “DFF.v”.

d. Part 4: Creating DFF_tb Module

I have written the test bench for the DFF module code after creating my module. We require test bench just to make sure that the module we have created is working properly. In this lab, I have written the test bench and saved the file as “DFF_tb.v”.

e. Part 5: Simulation

After completing the code and test bench for DFF_tb I have run the command “simv” for simulation.

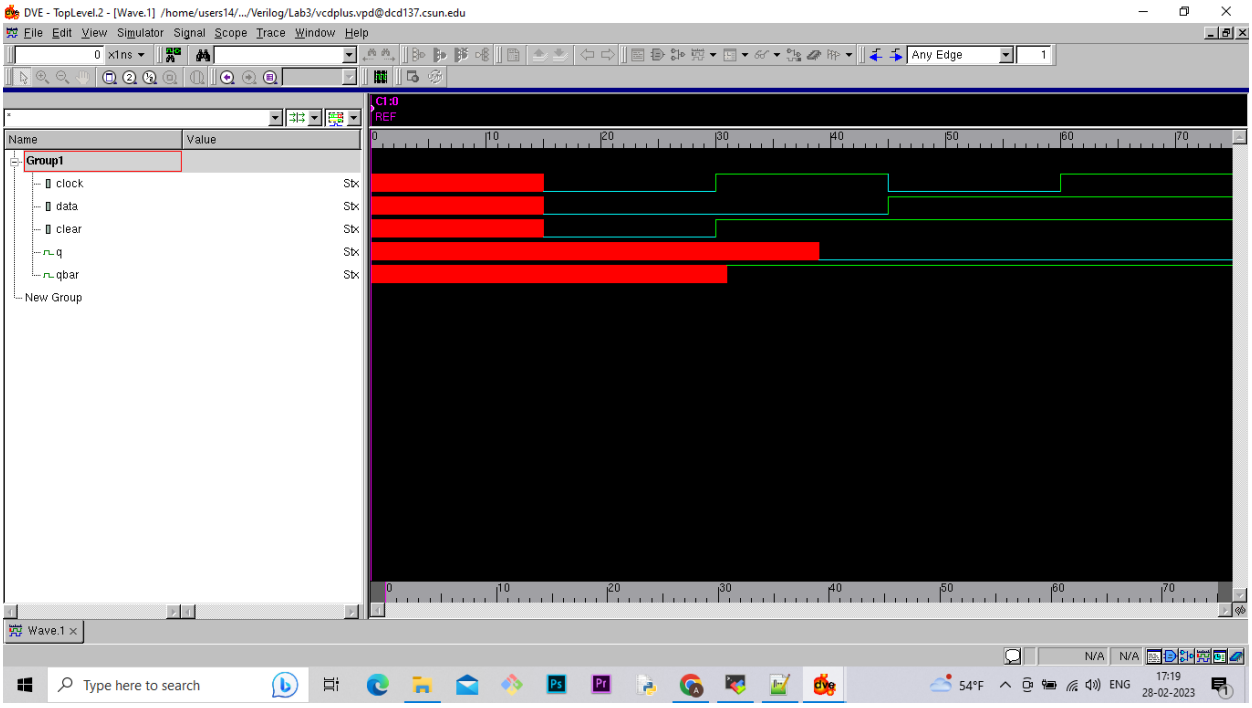


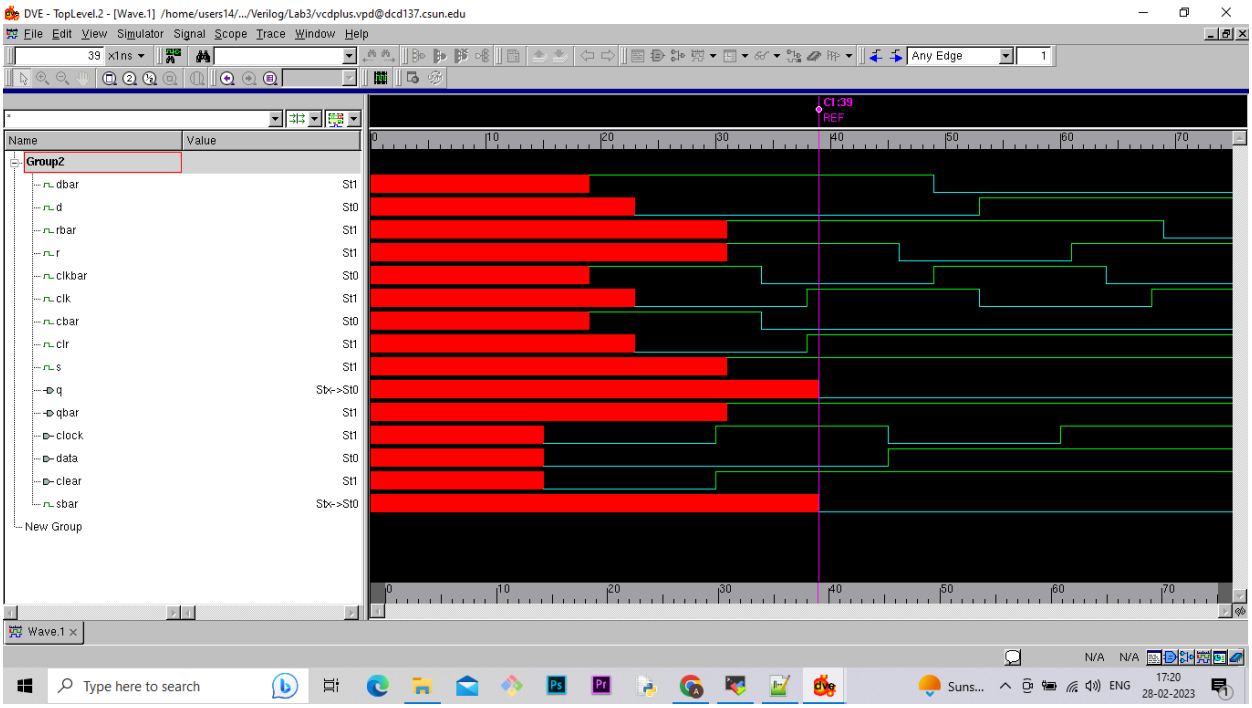
e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l DFF.log” command.

f. Part 6: Seeing the waveform.

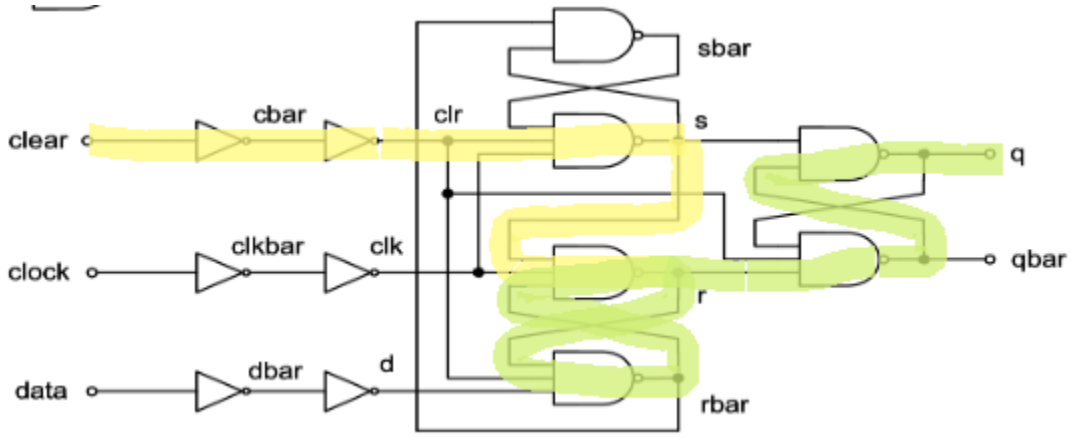
After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.





Lab report question: What's the critical path (longest delay) of this design?

1.The critical path for the circuit is highlighted below.



The Longest delay is 45.5 ns.

2.What is the maximum operating frequency for your circuit?

The maximum operating frequency for circuit is=1/ shortest delay ….(modified equation)

= 1/20.3

= 0.04926 x 10^9 Hz

= 4.926 x 10^7 Hz

Conclusion:

In this lab I learned how to design SR latch using some inputs, delay with combination of gates in Verilog. This lab taught me how to use hierarchical method to build any kind of circuit diagram in Verilog. And in this lab I learn how to calculate the maximum operating frequency of given circuit.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 27-02-2023