California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 7 Report

By

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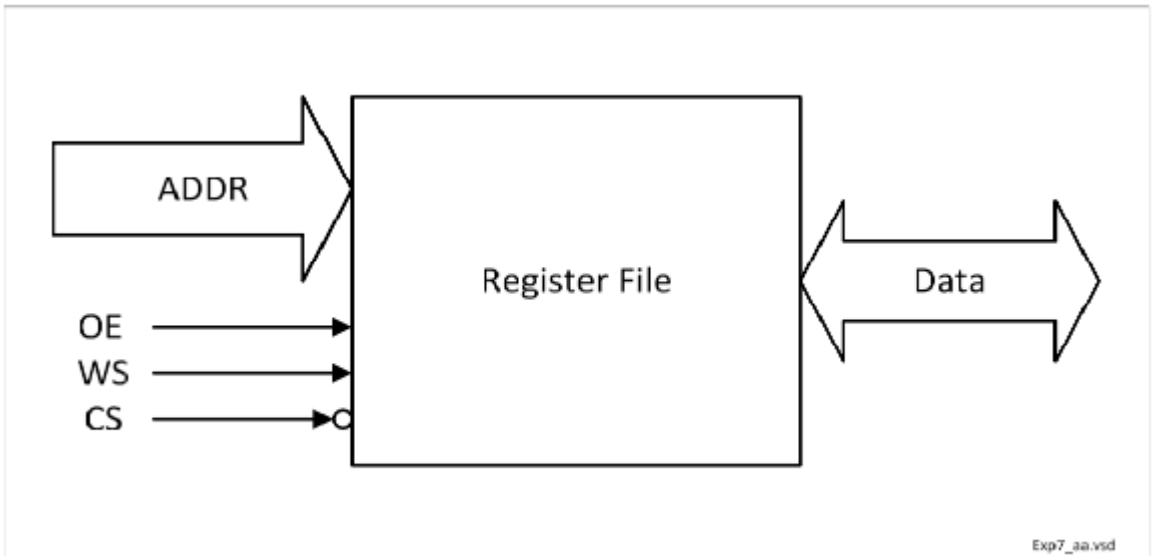
CSUN ID- 203131064

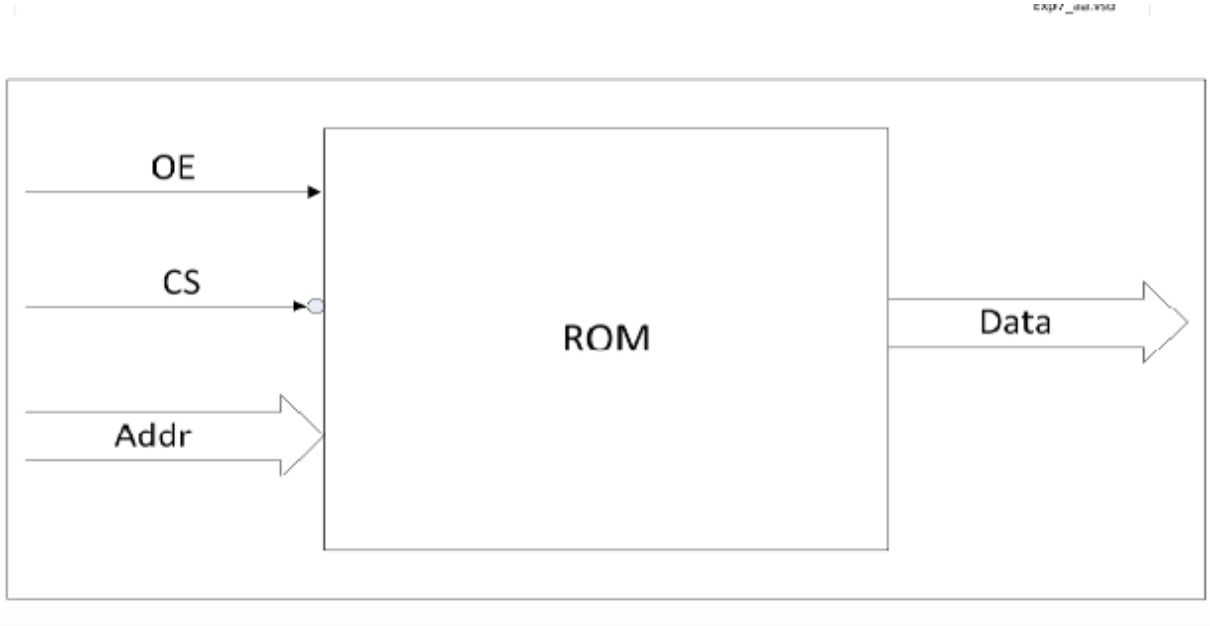
1: Introduction

The objective of this lab is to construct a scalable register file with a bidirectional data bus line and Initializing memory from file.

Here we have to use following diagram to build scalable register.



Which will be used as Random Access Memory.



2: Procedure

a. Part 1: Creating REG_F Module

In this lab I have created a REG_F module for scalable register. Inside the module I have assigned “WS, OE, CS and ADDR,” as input variables and “DATA” as bidirectional variable. Then I wrote the scalable register logic inside module. After completing the code I ended the module using and saved the file with name “REG_F.v”.

a. Part 1.2: Creating ROM Module

In this lab I have created a ROM module for only read purpose. Inside the module I have assigned “ OE, CS and ADDR,” as input variables and “DATA” as output variable. Then I wrote the read logic inside module. After completing the code I ended the module using and saved the file with name “ROM.v”.

b. Part 2: Creating REG_TB1 Module

I have written the test bench for the REG module. We require test bench just to make sure that the module we have created is working properly. Here, in this testbench I have performed write to and read from operation and demonstrated an individual and block read.

c. Part 3: Creating REG_TB2 Module

I have written the test bench for the REG module. Here, in this testbench I have initialized the memory in hex using $readmemh system task. I put all the addresses and memory in INIT.txt file.

c. Part 3: execution.

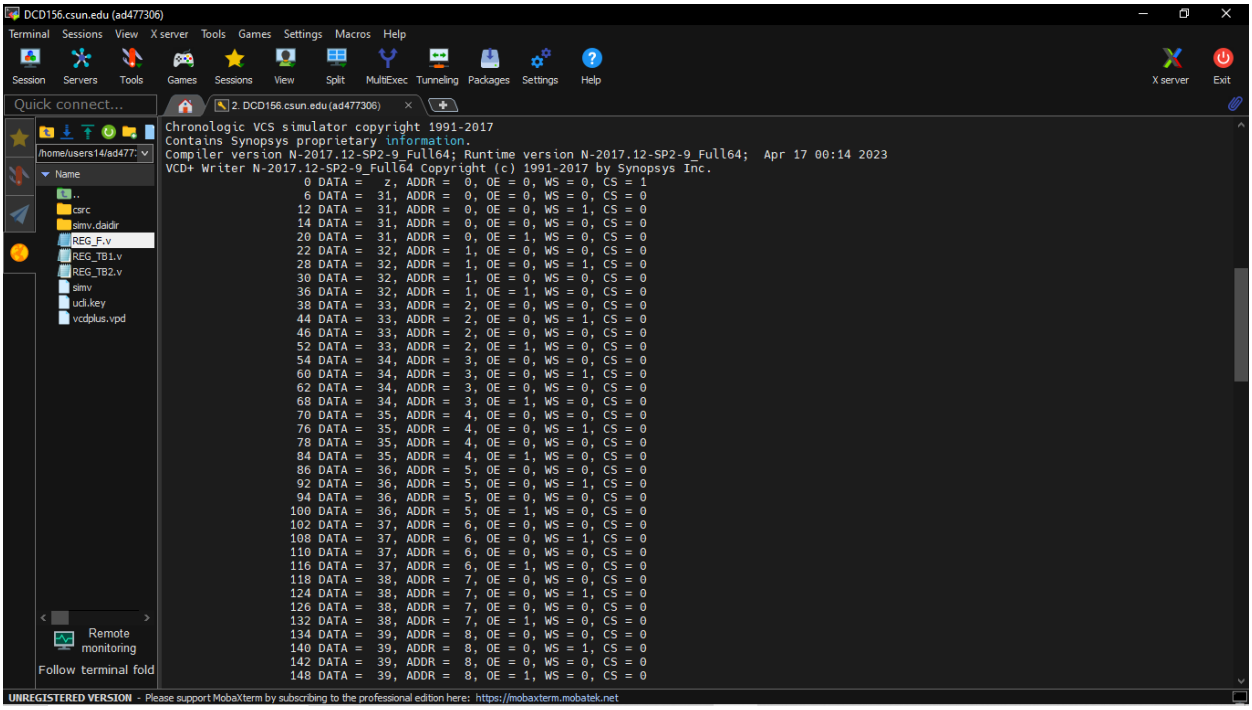
Using “vcs -debug -full64 REG_F.v REG_TB1.v” command I executed first testbench file.

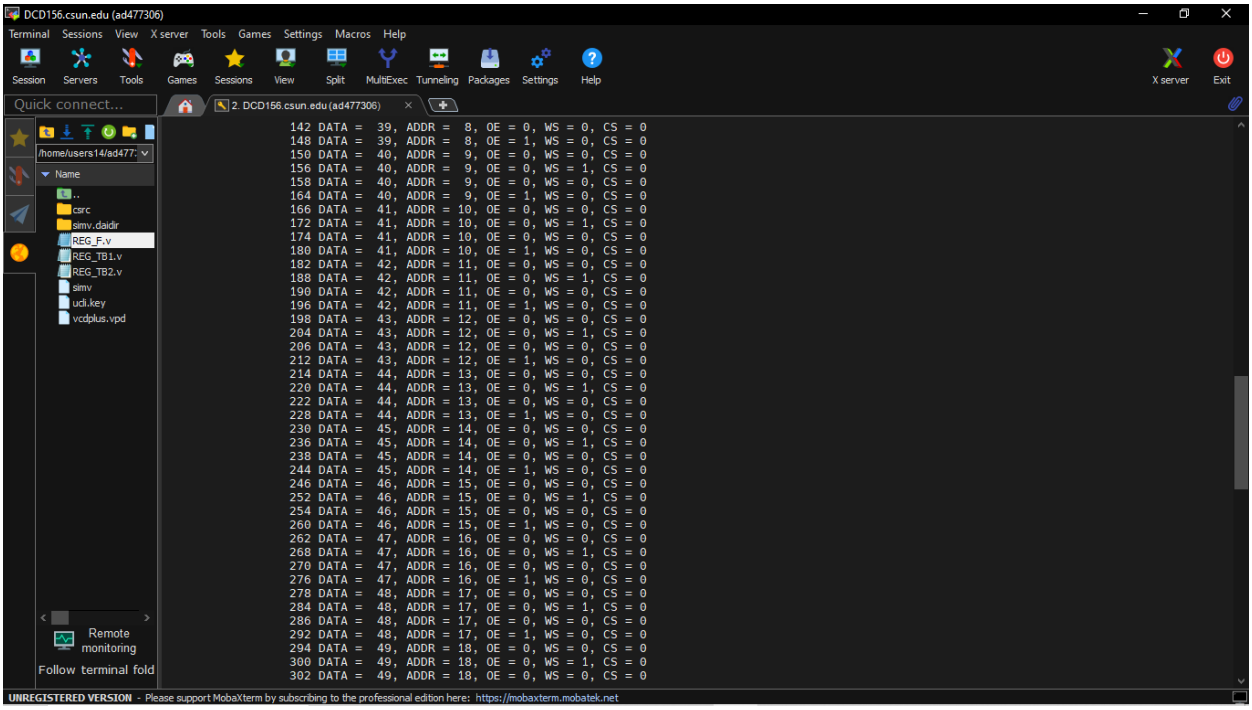
Again using “vcs -debug -full64 REG_F.v REG_TB2.v” command I executed second testbench file.

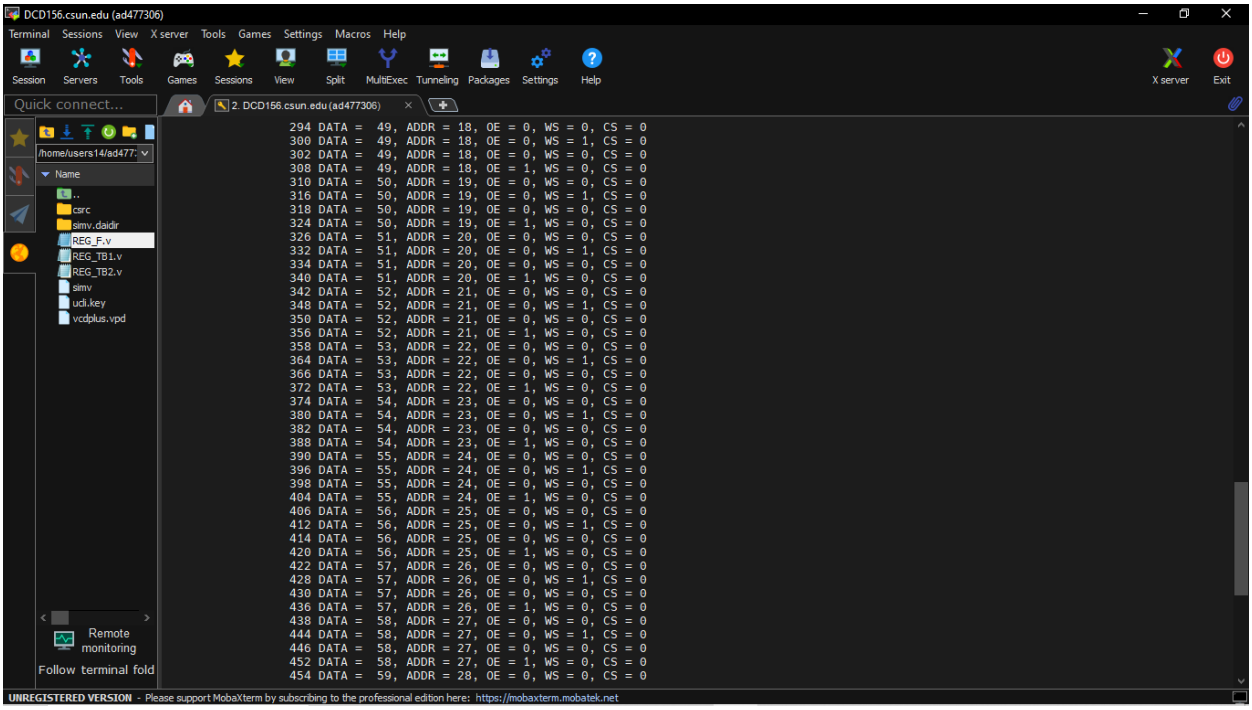
d. Part 4: Simulation

After an execution of all modules, I have run the command “simv” for simulation.

Simulation for Test Strategy 1:




DCD156.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help X server Exit
Quick connect...
2. DCD156.csun.edu (ad477306)
/home/users14/ad477:
Name
..
csrc
simv.daidir
REG_F.v
REG_TB1.v
REG_TB2.v
simv
ucli.key
vcdplus.vpd
Remote monitoring
Follow terminal fold
142 DATA = 39, ADDR = 8, OE = 0, WS = 0, CS = 0
148 DATA = 39, ADDR = 8, OE = 1, WS = 0, CS = 0
150 DATA = 40, ADDR = 9, OE = 0, WS = 0, CS = 0
156 DATA = 40, ADDR = 9, OE = 0, WS = 1, CS = 0
158 DATA = 40, ADDR = 9, OE = 0, WS = 0, CS = 0
164 DATA = 40, ADDR = 9, OE = 1, WS = 0, CS = 0
166 DATA = 41, ADDR = 10, OE = 0, WS = 0, CS = 0
172 DATA = 41, ADDR = 10, OE = 0, WS = 1, CS = 0
174 DATA = 41, ADDR = 10, OE = 0, WS = 0, CS = 0
180 DATA = 41, ADDR = 10, OE = 1, WS = 0, CS = 0
182 DATA = 42, ADDR = 11, OE = 0, WS = 0, CS = 0
188 DATA = 42, ADDR = 11, OE = 0, WS = 1, CS = 0
190 DATA = 42, ADDR = 11, OE = 0, WS = 0, CS = 0
196 DATA = 42, ADDR = 11, OE = 1, WS = 0, CS = 0
198 DATA = 43, ADDR = 12, OE = 0, WS = 0, CS = 0
204 DATA = 43, ADDR = 12, OE = 0, WS = 1, CS = 0
206 DATA = 43, ADDR = 12, OE = 0, WS = 0, CS = 0
212 DATA = 43, ADDR = 12, OE = 1, WS = 0, CS = 0
214 DATA = 44, ADDR = 13, OE = 0, WS = 0, CS = 0
220 DATA = 44, ADDR = 13, OE = 0, WS = 1, CS = 0
222 DATA = 44, ADDR = 13, OE = 0, WS = 0, CS = 0
228 DATA = 44, ADDR = 13, OE = 1, WS = 0, CS = 0
230 DATA = 45, ADDR = 14, OE = 0, WS = 0, CS = 0
236 DATA = 45, ADDR = 14, OE = 0, WS = 1, CS = 0
238 DATA = 45, ADDR = 14, OE = 0, WS = 0, CS = 0
244 DATA = 45, ADDR = 14, OE = 1, WS = 0, CS = 0
246 DATA = 46, ADDR = 15, OE = 0, WS = 0, CS = 0
252 DATA = 46, ADDR = 15, OE = 0, WS = 1, CS = 0
254 DATA = 46, ADDR = 15, OE = 0, WS = 0, CS = 0
260 DATA = 46, ADDR = 15, OE = 1, WS = 0, CS = 0
262 DATA = 47, ADDR = 16, OE = 0, WS = 0, CS = 0
268 DATA = 47, ADDR = 16, OE = 0, WS = 1, CS = 0
270 DATA = 47, ADDR = 16, OE = 0, WS = 0, CS = 0
276 DATA = 47, ADDR = 16, OE = 1, WS = 0, CS = 0
278 DATA = 48, ADDR = 17, OE = 0, WS = 0, CS = 0
284 DATA = 48, ADDR = 17, OE = 0, WS = 1, CS = 0
286 DATA = 48, ADDR = 17, OE = 0, WS = 0, CS = 0
292 DATA = 48, ADDR = 17, OE = 1, WS = 0, CS = 0
294 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
300 DATA = 49, ADDR = 18, OE = 0, WS = 1, CS = 0
302 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net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2. DCD156.csun.edu (ad477306)
/home/users14/ad477:
Name
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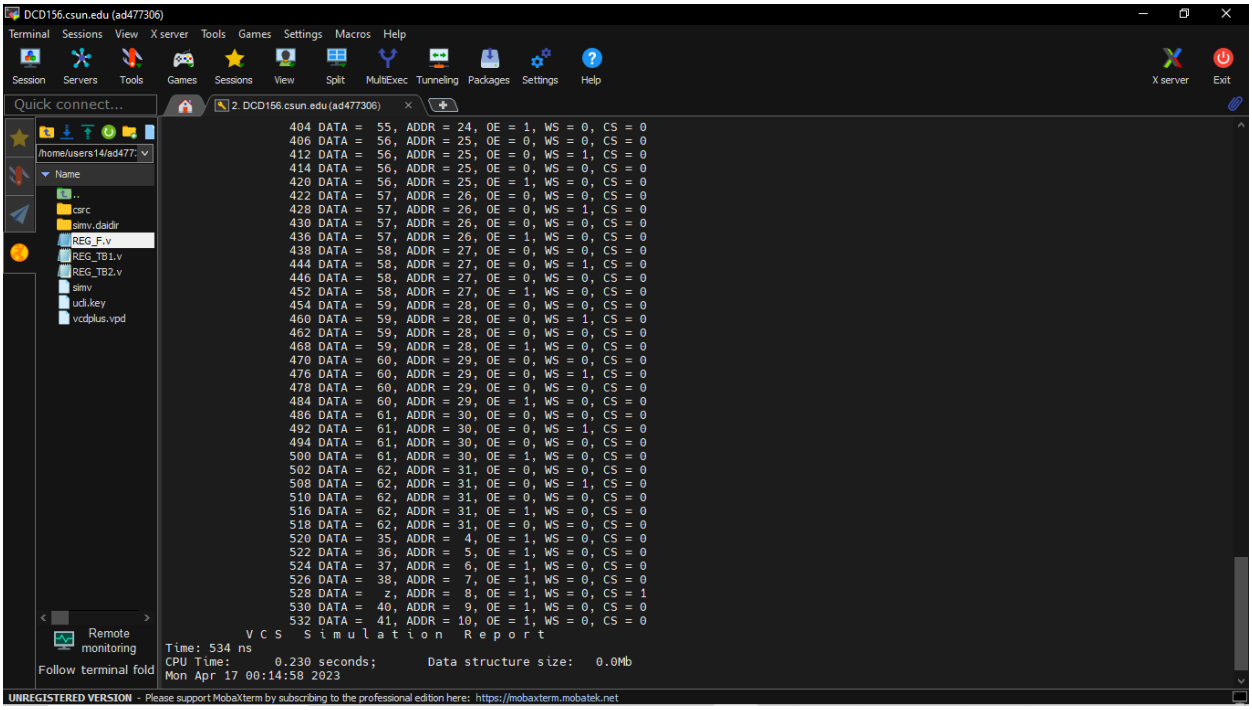
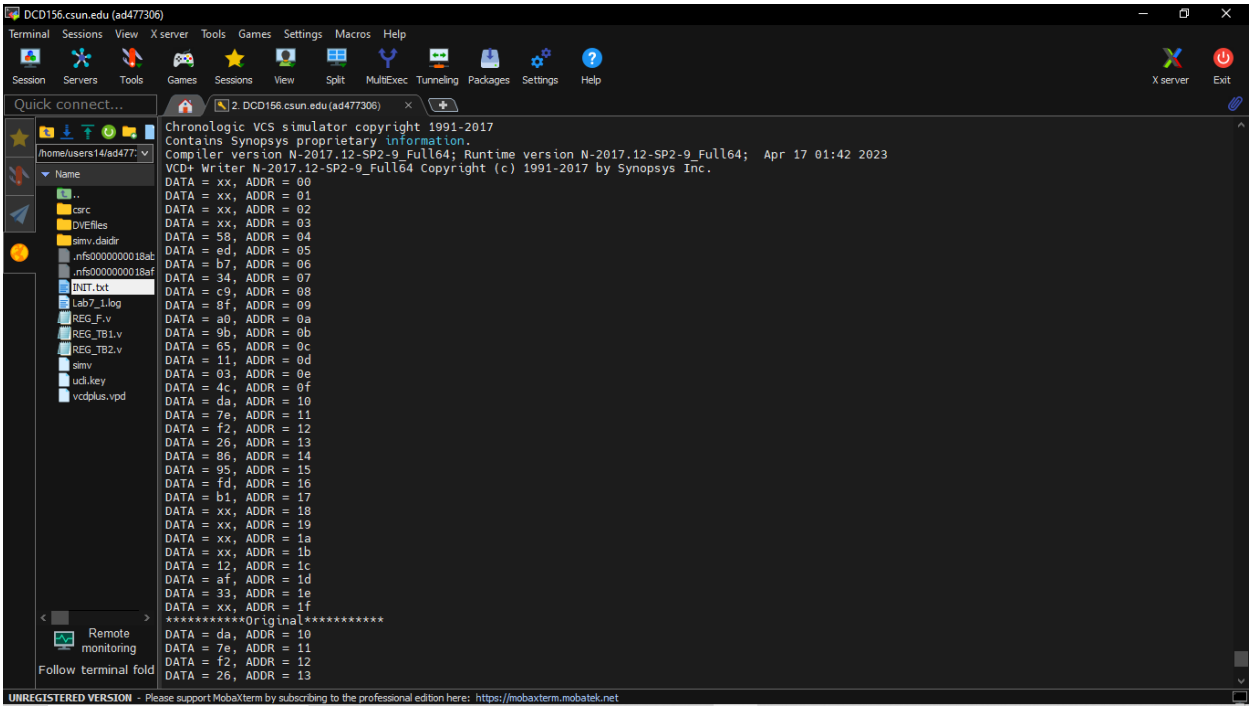
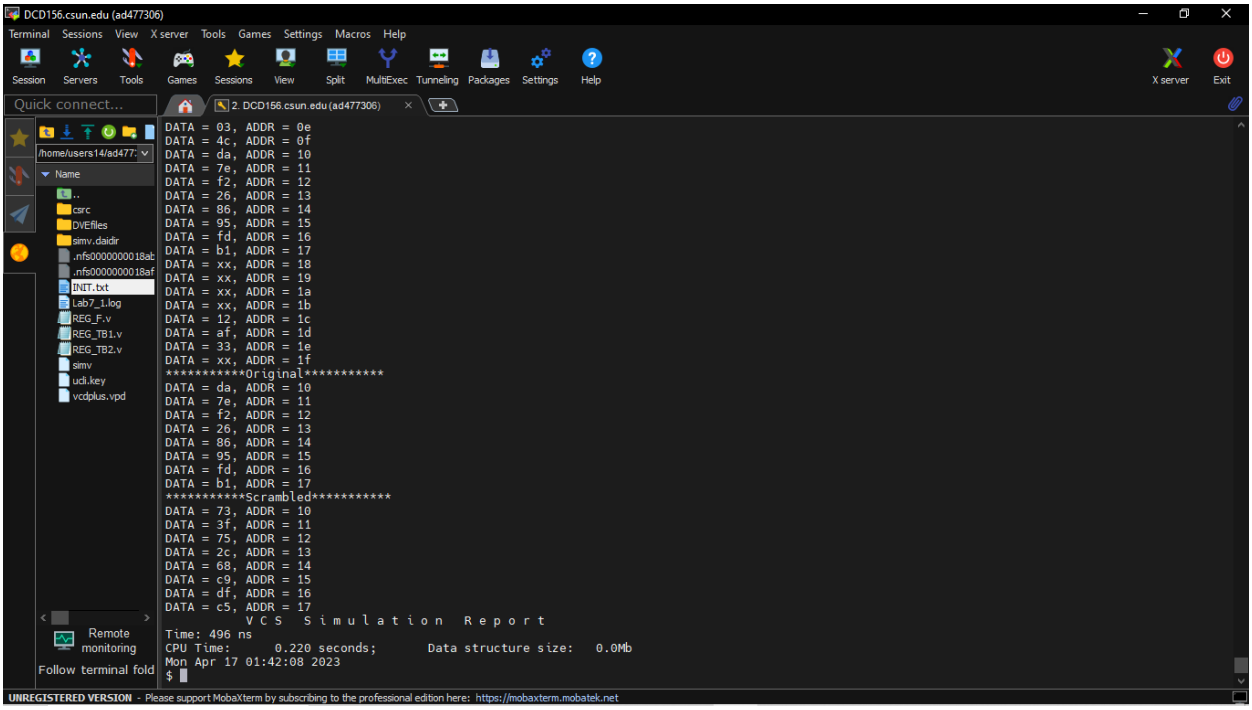
simv.daidir
REG_F.v
REG_TB1.v
REG_TB2.v
simv
ucli.key
vcdplus.vpd
Remote monitoring
Follow terminal fold
294 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
300 DATA = 49, ADDR = 18, OE = 0, WS = 1, CS = 0
302 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
308 DATA = 49, ADDR = 18, OE = 1, WS = 0, CS = 0
310 DATA = 50, ADDR = 19, OE = 0, WS = 0, CS = 0
316 DATA = 50, ADDR = 19, OE = 0, WS = 1, CS = 0
318 DATA = 50, ADDR = 19, OE = 0, WS = 0, CS = 0
324 DATA = 50, ADDR = 19, OE = 1, WS = 0, CS = 0
326 DATA = 51, ADDR = 20, OE = 0, WS = 0, CS = 0
332 DATA = 51, ADDR = 20, OE = 0, WS = 1, CS = 0
334 DATA = 51, ADDR = 20, OE = 0, WS = 0, CS = 0
340 DATA = 51, ADDR = 20, OE = 1, WS = 0, CS = 0
342 DATA = 52, ADDR = 21, OE = 0, WS = 0, CS = 0
348 DATA = 52, ADDR = 21, OE = 0, WS = 1, CS = 0
350 DATA = 52, ADDR = 21, OE = 0, WS = 0, CS = 0
356 DATA = 52, ADDR = 21, OE = 1, WS = 0, CS = 0
358 DATA = 53, ADDR = 22, OE = 0, WS = 0, CS = 0
364 DATA = 53, ADDR = 22, OE = 0, WS = 1, CS = 0
366 DATA = 53, ADDR = 22, OE = 0, WS = 0, CS = 0
372 DATA = 53, ADDR = 22, OE = 1, WS = 0, CS = 0
374 DATA = 54, ADDR = 23, OE = 0, WS = 0, CS = 0
380 DATA = 54, ADDR = 23, OE = 0, WS = 1, CS = 0
382 DATA = 54, ADDR = 23, OE = 0, WS = 0, CS = 0
388 DATA = 54, ADDR = 23, OE = 1, WS = 0, CS = 0
390 DATA = 55, ADDR = 24, OE = 0, WS = 0, CS = 0
396 DATA = 55, ADDR = 24, OE = 0, WS = 1, CS = 0
398 DATA = 55, ADDR = 24, OE = 0, WS = 0, CS = 0
404 DATA = 55, ADDR = 24, OE = 1, WS = 0, CS = 0
406 DATA = 56, ADDR = 25, OE = 0, WS = 0, CS = 0
412 DATA = 56, ADDR = 25, OE = 0, WS = 1, CS = 0
414 DATA = 56, ADDR = 25, OE = 0, WS = 0, CS = 0
420 DATA = 56, ADDR = 25, OE = 1, WS = 0, CS = 0
422 DATA = 57, ADDR = 26, OE = 0, WS = 0, CS = 0
428 DATA = 57, ADDR = 26, OE = 0, WS = 1, CS = 0
430 DATA = 57, ADDR = 26, OE = 0, WS = 0, CS = 0
436 DATA = 57, ADDR = 26, OE = 1, WS = 0, CS = 0
438 DATA = 58, ADDR = 27, OE = 0, WS = 0, CS = 0
444 DATA = 58, ADDR = 27, OE = 0, WS = 1, CS = 0
446 DATA = 58, ADDR = 27, OE = 0, WS = 0, CS = 0
452 DATA = 58, ADDR = 27, OE = 1, WS = 0, CS = 0
454 DATA = 59, ADDR = 28, OE = 0, WS = 0, CS = 0
UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net



Simulation for Test Strategy 2:





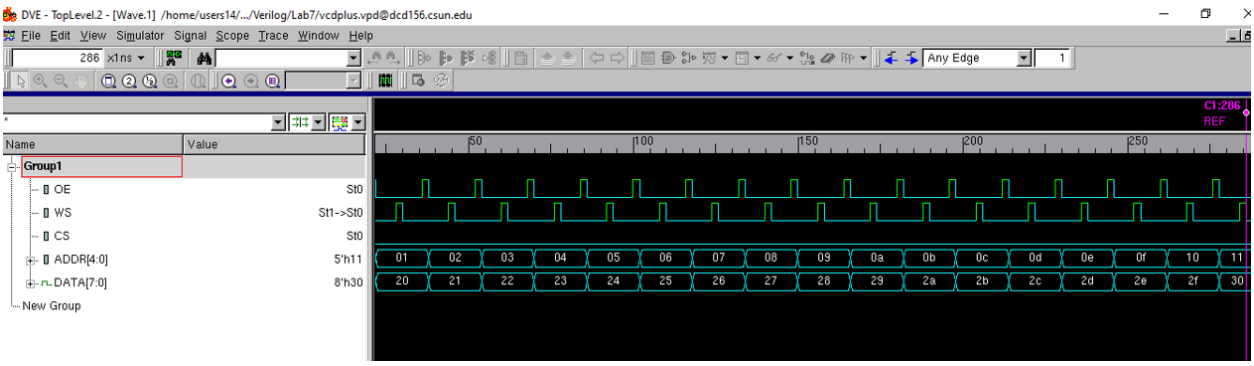
e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab6.log” command.

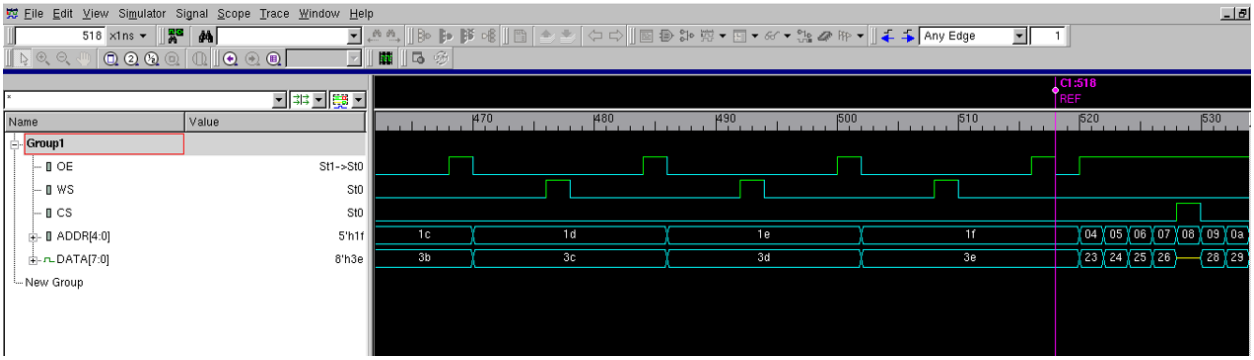
f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.

Test Strategy 1:

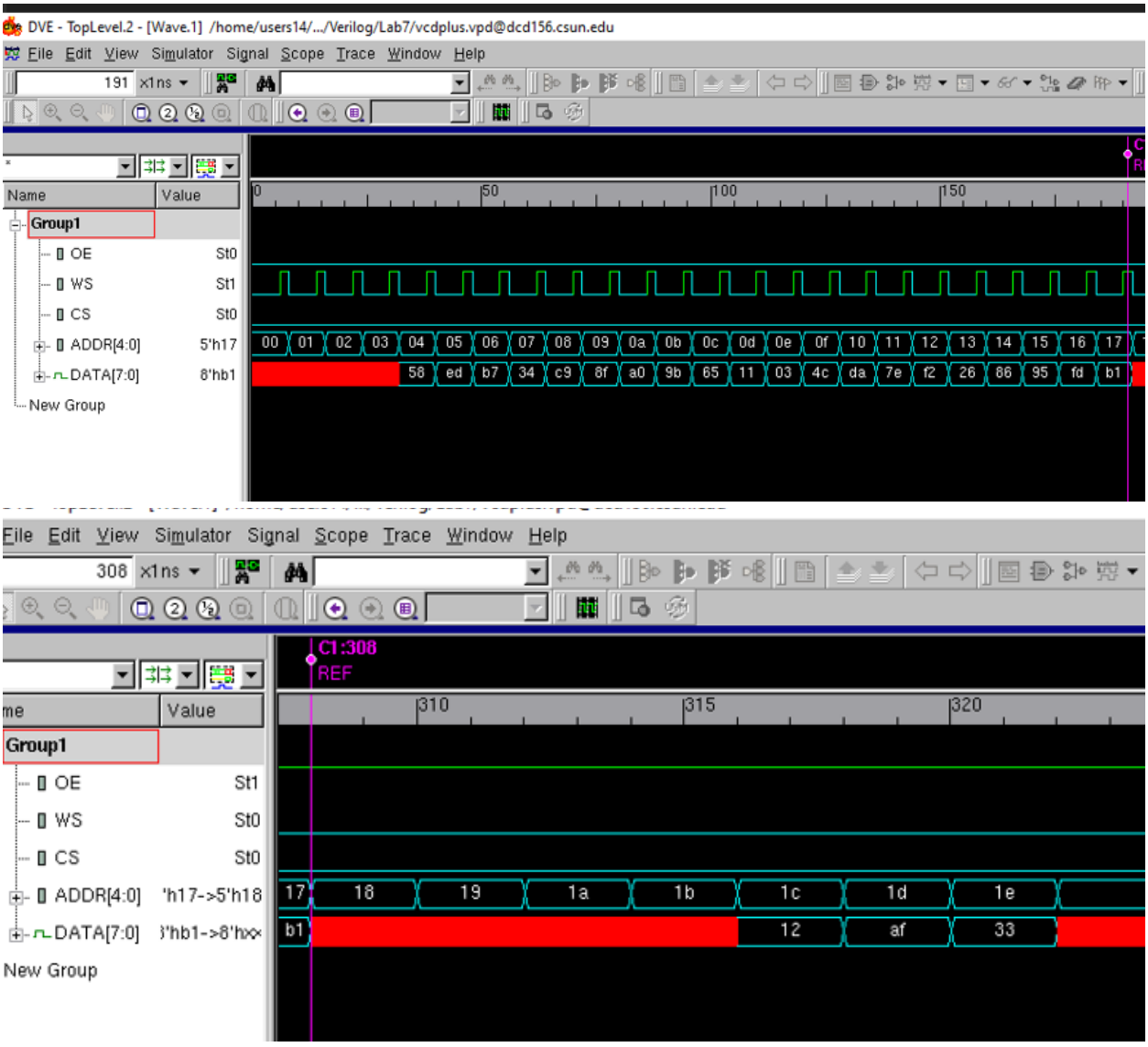


First, the register file was written to with unique values for each address using the first testbench. As shown above, the address starts at 00 (in hex), while the values assigned start at 31 (or 1F in hex) and incremented by 1 each time. Then each address was read from individually after writing to. Note that the data line only started storing upon the enabling of the chip select.

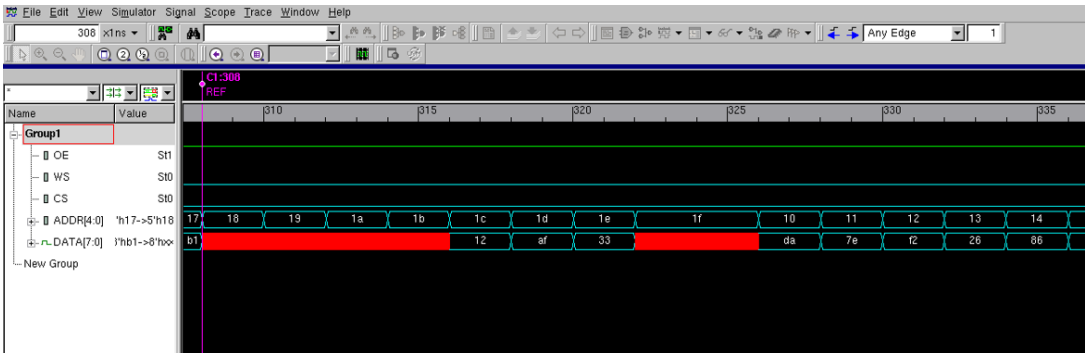


As shown above, the register file’s address ends at 31 (or 1F hex), corresponding to the default width of the register of 32. Each address was filled with unique values.

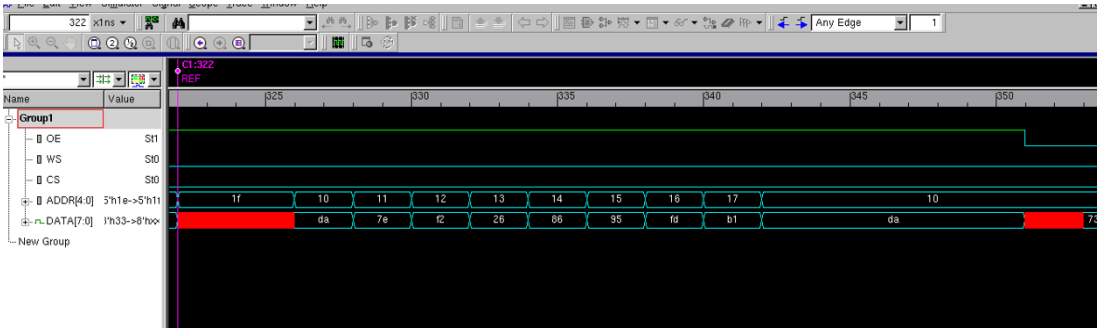
Test Strategy 2:



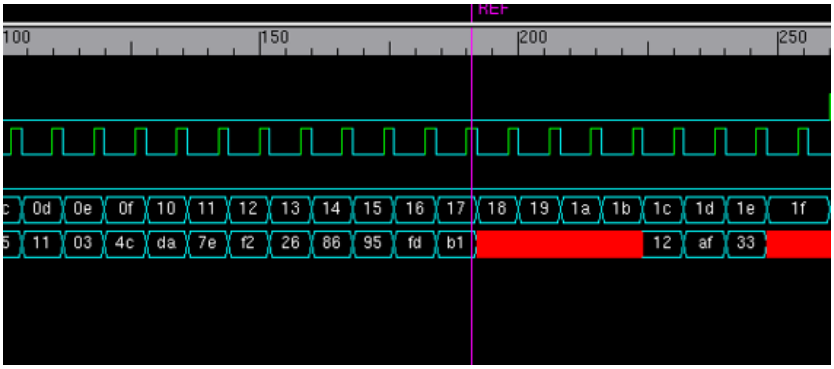
Shown above is the waveform that resulted from applying the second test bench. First the memory in the register model was initialized with the contents of a separate file (“INIT.txt”). All memory locations were accessed, but those without a value as specified in the data file, or have unspecified locations, remained uninitialized. This can be seen in the waveform above as the x construct, i.e. addresses 18 to 1b are x or uninitialized. Shown below is the period that output enable was triggered to high. The values stored were confirmed at this point as the data line is fed with these values during the read cycle.



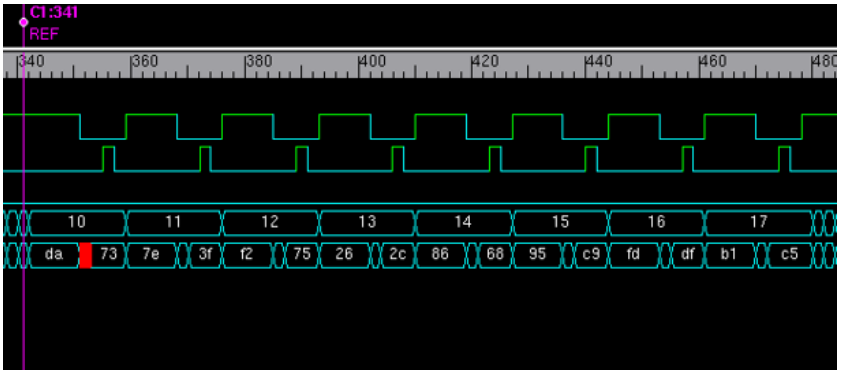
The next functionality demonstrated by the test bench involves scrambling part of the data in the memory. First, an address was read from memory during the read cycle. As the cycle was turned off, the value was scrambled according to instructions. (Below)



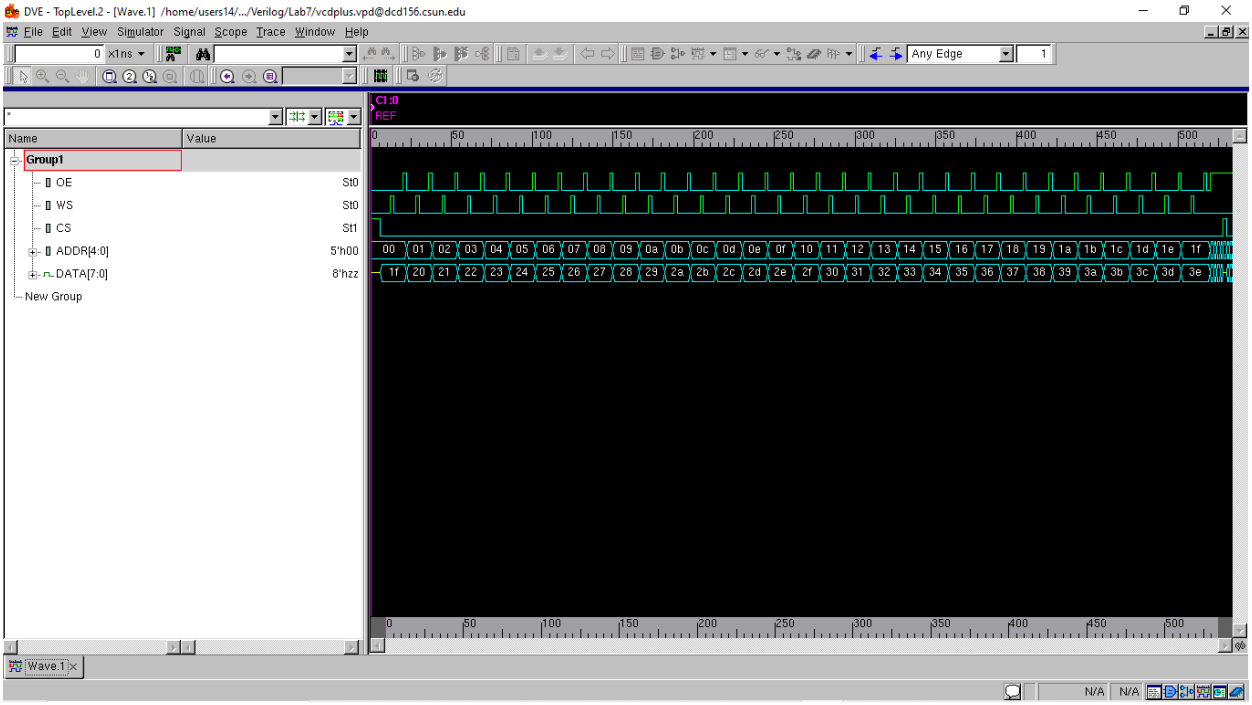
Before Scrambling

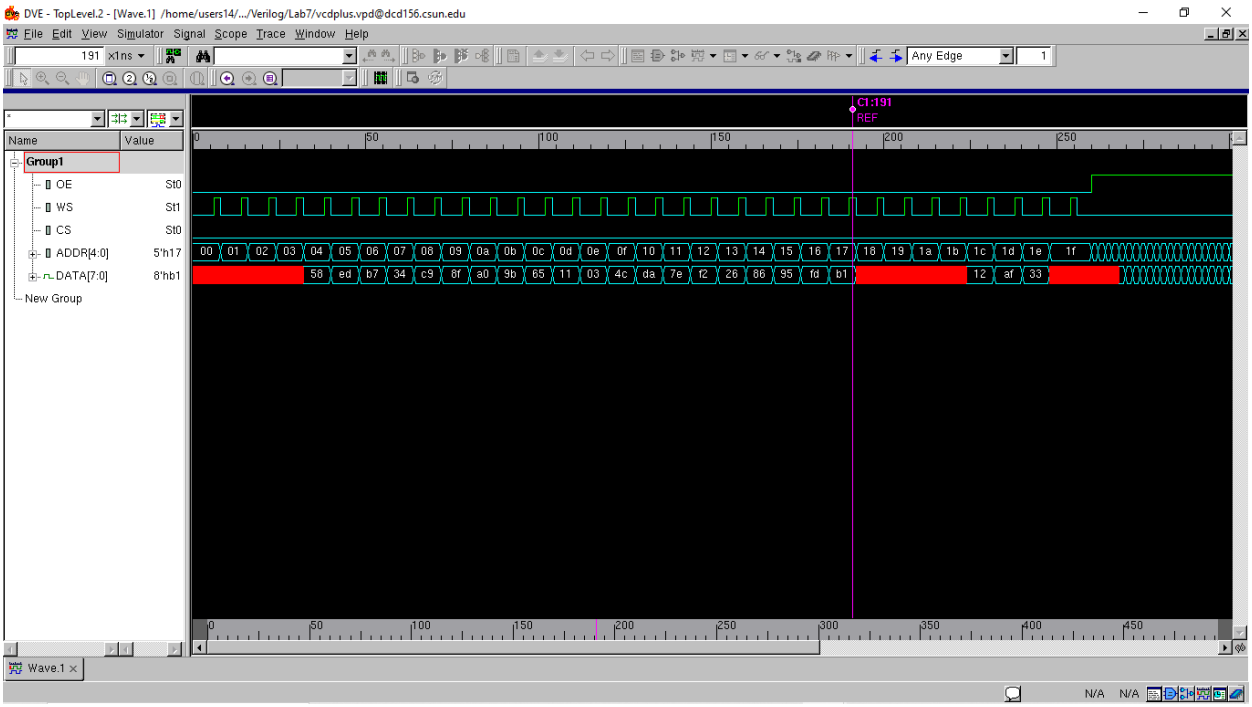


After Scrambling



Waveforms:


DVE - TopLevel.2 - [Wave.1] /home/users14/.../Verilog/Lab7/vcdplus.vpd@dcd156.csun.edu
File Edit View Simulator Signal Scope Trace Window Help
Any Edge
C1:0
REF
Name
Value
Group1
OE
St0
WS
St0
CS
St1
ADDR[4:0]
5'h00
DATA[7:0]
8'hzz
New Group
Wave.1


DVE - TopLevel.2 - [Wave.1] /home/users14/.../Verilog/Lab7/vcdplus.vpd@dcd156.csun.edu
File Edit View Simulator Signal Scope Trace Window Help
Any Edge
C1:191
REF
Name
Value
Group1
OE
St0
WS
St1
CS
St0
ADDR[4:0]
5'h17
DATA[7:0]
8'hb1
New Group
Wave.1

Lab report Extra Credit question: How many edge constructs do you use in your models?
Ans -
I used on edge construct in this model which is “posedge WS”.

Conclusion:

The register file model was successfully tested of its storing capabilities. The bidirectional data line also functioned as intended. All memory locations were successfully written to and read from, while also confirming the overriding functionality of the chip select line (memory enable). Individual and block read capabilities were also tested and confirmed. The read and write functions were confirmed of their functionality further using the second test bench and scrambling a segment of the memory. In this experiment, only one edge construct was used in the register file module.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 16-April-2023