

California State University, Northridge

Department of Electrical & Computer Engineering



ECE 526L

Lab 7 Report

By

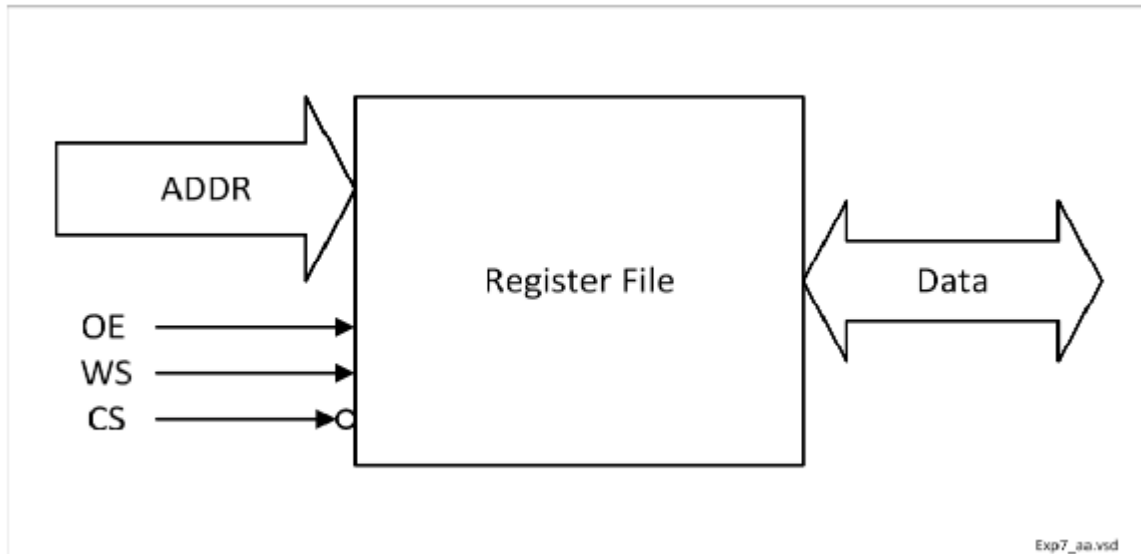
Avinash Damse

CSUN ID- 203131064

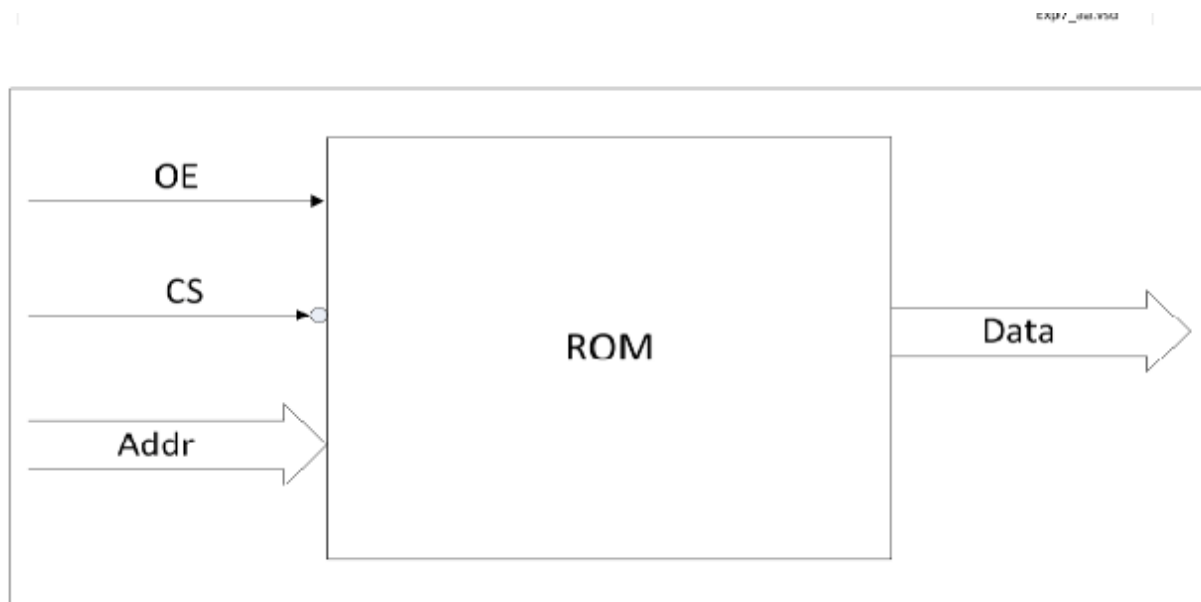
1: Introduction

The objective of this lab is to construct a scalable register file with a bidirectional data bus line and Initializing memory from file.

Here we have to use following diagram to build scalable register.



Which will be used as Random Access Memory.



2: Procedure

a. Part 1: Creating REG_F Module

In this lab I have created a REG_F module for scalable register. Inside the module I have assigned "WS, OE, CS and ADDR," as input variables and "DATA" as bidirectional variable. Then I wrote the scalable register logic inside module. After completing the code I ended the module using and saved the file with name "REG_F.v".

a. Part 1.2: Creating ROM Module

In this lab I have created a ROM module for only read purpose. Inside the module I have assigned "OE, CS and ADDR," as input variables and "DATA" as output variable. Then I wrote the read logic inside module. After completing the code I ended the module using and saved the file with name "ROM.v".

b. Part 2: Creating REG_TB1 Module

I have written the test bench for the REG module. We require test bench just to make sure that the module we have created is working properly. Here, in this testbench I have performed write to and read from operation and demonstrated an individual and block read.

c. Part 3: Creating REG_TB2 Module

I have written the test bench for the REG module. Here, in this testbench I have initialized the memory in hex using \$readmemh system task. I put all the addresses and memory in INIT.txt file.

c. Part 3: execution.

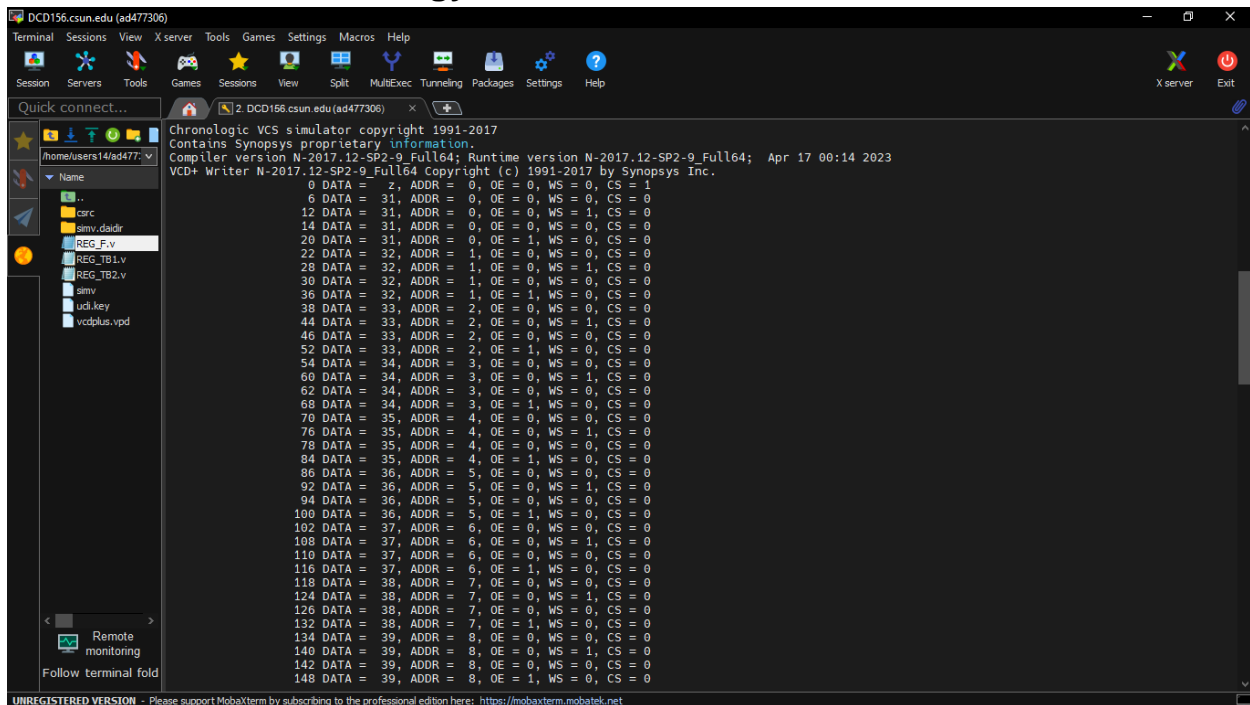
Using "vcs -debug -full64 REG_F.v REG_TB1.v" command I executed first testbench file.

Again using “vcs -debug -full64 REG_F.v REG_TB2.v” command I executed second testbench file.

d. Part 4: Simulation

After an execution of all modules, I have run the command “simv” for simulation.

Simulation for Test Strategy 1:



```
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information
Compiler version N-2017.12-SP2-9-Full64; Runtime version N-2017.12-SP2-9-Full64; Apr 17 00:14 2023
VCD+ Writer N-2017.12-SP2-9-Full64 Copyright (c) 1991-2017 by Synopsys Inc.
0 DATA = 2, ADDR = 0, OE = 0, WS = 0, CS = 1
6 DATA = 31, ADDR = 0, OE = 0, WS = 0, CS = 0
12 DATA = 31, ADDR = 0, OE = 0, WS = 1, CS = 0
14 DATA = 31, ADDR = 0, OE = 0, WS = 0, CS = 0
20 DATA = 31, ADDR = 0, OE = 1, WS = 0, CS = 0
22 DATA = 32, ADDR = 1, OE = 0, WS = 0, CS = 0
28 DATA = 32, ADDR = 1, OE = 0, WS = 1, CS = 0
30 DATA = 32, ADDR = 1, OE = 0, WS = 0, CS = 0
36 DATA = 32, ADDR = 1, OE = 1, WS = 0, CS = 0
38 DATA = 33, ADDR = 2, OE = 0, WS = 0, CS = 0
44 DATA = 33, ADDR = 2, OE = 0, WS = 1, CS = 0
46 DATA = 33, ADDR = 2, OE = 0, WS = 0, CS = 0
52 DATA = 33, ADDR = 2, OE = 1, WS = 0, CS = 0
54 DATA = 34, ADDR = 3, OE = 0, WS = 0, CS = 0
60 DATA = 34, ADDR = 3, OE = 0, WS = 1, CS = 0
62 DATA = 34, ADDR = 3, OE = 0, WS = 0, CS = 0
68 DATA = 34, ADDR = 3, OE = 1, WS = 0, CS = 0
70 DATA = 35, ADDR = 4, OE = 0, WS = 0, CS = 0
76 DATA = 35, ADDR = 4, OE = 0, WS = 1, CS = 0
78 DATA = 35, ADDR = 4, OE = 0, WS = 0, CS = 0
84 DATA = 35, ADDR = 4, OE = 1, WS = 0, CS = 0
86 DATA = 36, ADDR = 5, OE = 0, WS = 0, CS = 0
92 DATA = 36, ADDR = 5, OE = 0, WS = 1, CS = 0
94 DATA = 36, ADDR = 5, OE = 0, WS = 0, CS = 0
100 DATA = 36, ADDR = 5, OE = 1, WS = 0, CS = 0
102 DATA = 37, ADDR = 6, OE = 0, WS = 0, CS = 0
108 DATA = 37, ADDR = 6, OE = 0, WS = 1, CS = 0
110 DATA = 37, ADDR = 6, OE = 0, WS = 0, CS = 0
116 DATA = 37, ADDR = 6, OE = 1, WS = 0, CS = 0
118 DATA = 38, ADDR = 7, OE = 0, WS = 0, CS = 0
124 DATA = 38, ADDR = 7, OE = 0, WS = 1, CS = 0
126 DATA = 38, ADDR = 7, OE = 0, WS = 0, CS = 0
132 DATA = 38, ADDR = 7, OE = 1, WS = 0, CS = 0
134 DATA = 39, ADDR = 8, OE = 0, WS = 0, CS = 0
140 DATA = 39, ADDR = 8, OE = 0, WS = 1, CS = 0
142 DATA = 39, ADDR = 8, OE = 0, WS = 0, CS = 0
148 DATA = 39, ADDR = 8, OE = 1, WS = 0, CS = 0
```

DCD156.csun.edu (ad477306)

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

/home/users14/ad477306

Name

- csrc
- smv.daddr
- REG_F.v
- REG_TB1.v
- REG_TB2.v
- smv
- uci.key
- vcplus.vpd

Remote monitoring

Follow terminal fold

```
142 DATA = 39, ADDR = 8, OE = 0, WS = 0, CS = 0
148 DATA = 39, ADDR = 8, OE = 1, WS = 0, CS = 0
150 DATA = 40, ADDR = 9, OE = 0, WS = 0, CS = 0
156 DATA = 40, ADDR = 9, OE = 0, WS = 1, CS = 0
158 DATA = 40, ADDR = 9, OE = 0, WS = 0, CS = 0
164 DATA = 40, ADDR = 9, OE = 1, WS = 0, CS = 0
166 DATA = 41, ADDR = 10, OE = 0, WS = 0, CS = 0
172 DATA = 41, ADDR = 10, OE = 0, WS = 1, CS = 0
174 DATA = 41, ADDR = 10, OE = 0, WS = 0, CS = 0
180 DATA = 41, ADDR = 10, OE = 1, WS = 0, CS = 0
182 DATA = 42, ADDR = 11, OE = 0, WS = 0, CS = 0
188 DATA = 42, ADDR = 11, OE = 0, WS = 1, CS = 0
190 DATA = 42, ADDR = 11, OE = 0, WS = 0, CS = 0
196 DATA = 42, ADDR = 11, OE = 1, WS = 0, CS = 0
198 DATA = 43, ADDR = 12, OE = 0, WS = 0, CS = 0
204 DATA = 43, ADDR = 12, OE = 0, WS = 1, CS = 0
206 DATA = 43, ADDR = 12, OE = 0, WS = 0, CS = 0
212 DATA = 43, ADDR = 12, OE = 1, WS = 0, CS = 0
214 DATA = 44, ADDR = 13, OE = 1, WS = 0, CS = 0
220 DATA = 44, ADDR = 13, OE = 0, WS = 1, CS = 0
222 DATA = 44, ADDR = 13, OE = 0, WS = 0, CS = 0
228 DATA = 44, ADDR = 13, OE = 1, WS = 0, CS = 0
230 DATA = 45, ADDR = 14, OE = 0, WS = 0, CS = 0
236 DATA = 45, ADDR = 14, OE = 0, WS = 1, CS = 0
238 DATA = 45, ADDR = 14, OE = 0, WS = 0, CS = 0
244 DATA = 45, ADDR = 14, OE = 1, WS = 0, CS = 0
246 DATA = 46, ADDR = 15, OE = 0, WS = 0, CS = 0
252 DATA = 46, ADDR = 15, OE = 0, WS = 1, CS = 0
254 DATA = 46, ADDR = 15, OE = 0, WS = 0, CS = 0
260 DATA = 46, ADDR = 15, OE = 1, WS = 0, CS = 0
262 DATA = 47, ADDR = 16, OE = 0, WS = 0, CS = 0
268 DATA = 47, ADDR = 16, OE = 0, WS = 1, CS = 0
270 DATA = 47, ADDR = 16, OE = 0, WS = 0, CS = 0
276 DATA = 47, ADDR = 16, OE = 1, WS = 0, CS = 0
278 DATA = 48, ADDR = 17, OE = 0, WS = 0, CS = 0
284 DATA = 48, ADDR = 17, OE = 0, WS = 1, CS = 0
286 DATA = 48, ADDR = 17, OE = 0, WS = 0, CS = 0
292 DATA = 48, ADDR = 17, OE = 1, WS = 0, CS = 0
294 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
300 DATA = 49, ADDR = 18, OE = 0, WS = 1, CS = 0
302 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

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Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

/home/users14/ad477306

Name

- csrc
- smv.daddr
- REG_F.v
- REG_TB1.v
- REG_TB2.v
- smv
- uci.key
- vcplus.vpd

Remote monitoring

Follow terminal fold

```
294 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
300 DATA = 49, ADDR = 18, OE = 0, WS = 1, CS = 0
302 DATA = 49, ADDR = 18, OE = 0, WS = 0, CS = 0
308 DATA = 49, ADDR = 18, OE = 1, WS = 0, CS = 0
310 DATA = 50, ADDR = 19, OE = 0, WS = 0, CS = 0
316 DATA = 50, ADDR = 19, OE = 0, WS = 1, CS = 0
318 DATA = 50, ADDR = 19, OE = 0, WS = 0, CS = 0
324 DATA = 50, ADDR = 19, OE = 1, WS = 0, CS = 0
326 DATA = 51, ADDR = 20, OE = 0, WS = 0, CS = 0
332 DATA = 51, ADDR = 20, OE = 0, WS = 1, CS = 0
334 DATA = 51, ADDR = 20, OE = 0, WS = 0, CS = 0
340 DATA = 51, ADDR = 20, OE = 1, WS = 0, CS = 0
342 DATA = 52, ADDR = 21, OE = 0, WS = 0, CS = 0
348 DATA = 52, ADDR = 21, OE = 0, WS = 1, CS = 0
350 DATA = 52, ADDR = 21, OE = 0, WS = 0, CS = 0
356 DATA = 52, ADDR = 21, OE = 1, WS = 0, CS = 0
358 DATA = 53, ADDR = 22, OE = 0, WS = 0, CS = 0
364 DATA = 53, ADDR = 22, OE = 0, WS = 1, CS = 0
366 DATA = 53, ADDR = 22, OE = 0, WS = 0, CS = 0
372 DATA = 53, ADDR = 22, OE = 1, WS = 0, CS = 0
374 DATA = 54, ADDR = 23, OE = 0, WS = 0, CS = 0
380 DATA = 54, ADDR = 23, OE = 0, WS = 1, CS = 0
382 DATA = 54, ADDR = 23, OE = 0, WS = 0, CS = 0
388 DATA = 54, ADDR = 23, OE = 1, WS = 0, CS = 0
390 DATA = 55, ADDR = 24, OE = 0, WS = 0, CS = 0
396 DATA = 55, ADDR = 24, OE = 0, WS = 1, CS = 0
398 DATA = 55, ADDR = 24, OE = 0, WS = 0, CS = 0
404 DATA = 55, ADDR = 24, OE = 1, WS = 0, CS = 0
406 DATA = 56, ADDR = 25, OE = 0, WS = 0, CS = 0
412 DATA = 56, ADDR = 25, OE = 0, WS = 1, CS = 0
414 DATA = 56, ADDR = 25, OE = 0, WS = 0, CS = 0
420 DATA = 56, ADDR = 25, OE = 1, WS = 0, CS = 0
422 DATA = 57, ADDR = 26, OE = 0, WS = 0, CS = 0
428 DATA = 57, ADDR = 26, OE = 0, WS = 1, CS = 0
430 DATA = 57, ADDR = 26, OE = 0, WS = 0, CS = 0
436 DATA = 57, ADDR = 26, OE = 1, WS = 0, CS = 0
438 DATA = 58, ADDR = 27, OE = 0, WS = 0, CS = 0
444 DATA = 58, ADDR = 27, OE = 0, WS = 1, CS = 0
446 DATA = 58, ADDR = 27, OE = 0, WS = 0, CS = 0
452 DATA = 58, ADDR = 27, OE = 1, WS = 0, CS = 0
454 DATA = 59, ADDR = 28, OE = 0, WS = 0, CS = 0
```

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

The screenshot shows the MobaXterm interface with a terminal window titled "2. DCD156.csun.edu (ad477306)". The terminal displays a "V C S S i m u l a t i o n R e p o r t" with the following data:

Line	DATA	ADDR	OE	WS	CS
404	55	24	1	0	0
406	56	25	0	0	0
412	56	25	0	1	0
414	56	25	0	0	0
420	56	25	1	0	0
422	57	26	0	0	0
428	57	26	0	1	0
430	57	26	0	0	0
436	57	26	1	0	0
438	58	27	0	0	0
444	58	27	0	1	0
446	58	27	0	0	0
452	58	27	1	0	0
454	59	28	0	0	0
460	59	28	0	1	0
462	59	28	0	0	0
468	59	28	1	0	0
470	60	29	0	0	0
476	60	29	0	1	0
478	60	29	0	0	0
484	60	29	1	0	0
486	61	30	0	0	0
492	61	30	0	1	0
494	61	30	0	0	0
500	61	30	1	0	0
502	62	31	0	0	0
508	62	31	0	1	0
510	62	31	0	0	0
516	62	31	1	0	0
518	62	31	0	0	0
520	35	4	1	0	0
522	36	5	1	0	0
524	37	6	1	0	0
526	38	7	1	0	0
528	z	8	1	0	1
530	40	9	1	0	0
532	41	10	1	0	0

Summary statistics at the bottom of the report:

- Time: 534 ns
- CPU Time: 0.230 seconds;
- Data structure size: 0.0Mb
- Mon Apr 17 00:14:58 2023

The interface also shows a file explorer on the left with a tree view containing folders like "csrc", "snv_dadr", and files like "REG_F.v", "REG_TB1.v", "REG_TB2.v", "snv", "udi.key", and "vcdplus.vpd". The status bar at the bottom indicates "UNREGISTERED VERSION" and provides a link to the professional edition.

Simulation for Test Strategy 2:

```
DCD156.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/home/users14/ad477-
Name
csrc
DVEfiles
smv.daidr
.nfs00000000018ab
.nfs00000000018af
INIT.txt
lab7_1.log
REG_F.v
REG_TB1.v
REG_TB2.v
smv
ucd.key
vcdplus.vpd

Remote monitoring
Follow terminal fold

Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-SP2-9_Full64; Runtime version N-2017.12-SP2-9_Full64; Apr 17 01:42 2023
VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
DATA = xx, ADDR = 00
DATA = xx, ADDR = 01
DATA = xx, ADDR = 02
DATA = xx, ADDR = 03
DATA = 58, ADDR = 04
DATA = ed, ADDR = 05
DATA = b7, ADDR = 06
DATA = 34, ADDR = 07
DATA = c9, ADDR = 08
DATA = 8f, ADDR = 09
DATA = a0, ADDR = 0a
DATA = 9b, ADDR = 0b
DATA = 65, ADDR = 0c
DATA = 11, ADDR = 0d
DATA = 03, ADDR = 0e
DATA = 4c, ADDR = 0f
DATA = da, ADDR = 10
DATA = 7e, ADDR = 11
DATA = f2, ADDR = 12
DATA = 26, ADDR = 13
DATA = 86, ADDR = 14
DATA = 95, ADDR = 15
DATA = fd, ADDR = 16
DATA = b1, ADDR = 17
DATA = xx, ADDR = 18
DATA = xx, ADDR = 19
DATA = xx, ADDR = 1a
DATA = xx, ADDR = 1b
DATA = 12, ADDR = 1c
DATA = af, ADDR = 1d
DATA = 33, ADDR = 1e
DATA = xx, ADDR = 1f
*****Original*****
DATA = da, ADDR = 10
DATA = 7e, ADDR = 11
DATA = f2, ADDR = 12
DATA = 26, ADDR = 13
DATA = 03, ADDR = 0e
DATA = 4c, ADDR = 0f
DATA = da, ADDR = 10
DATA = 7e, ADDR = 11
DATA = f2, ADDR = 12
DATA = 26, ADDR = 13
DATA = 86, ADDR = 14
DATA = 95, ADDR = 15
DATA = fd, ADDR = 16
DATA = b1, ADDR = 17
DATA = xx, ADDR = 18
DATA = xx, ADDR = 19
DATA = xx, ADDR = 1a
DATA = xx, ADDR = 1b
DATA = 12, ADDR = 1c
DATA = af, ADDR = 1d
DATA = 33, ADDR = 1e
DATA = xx, ADDR = 1f
*****Original*****
DATA = da, ADDR = 10
DATA = 7e, ADDR = 11
DATA = f2, ADDR = 12
DATA = 26, ADDR = 13
DATA = 86, ADDR = 14
DATA = 95, ADDR = 15
DATA = fd, ADDR = 16
DATA = b1, ADDR = 17
*****Scrambled*****
DATA = 73, ADDR = 10
DATA = 3f, ADDR = 11
DATA = 75, ADDR = 12
DATA = 2c, ADDR = 13
DATA = 68, ADDR = 14
DATA = c9, ADDR = 15
DATA = df, ADDR = 16
DATA = c5, ADDR = 17
VCS Simulation Report
Time: 496 ns
CPU Time: 0.220 seconds; Data structure size: 0.0Mb
Mon Apr 17 01:42:08 2023
$
```

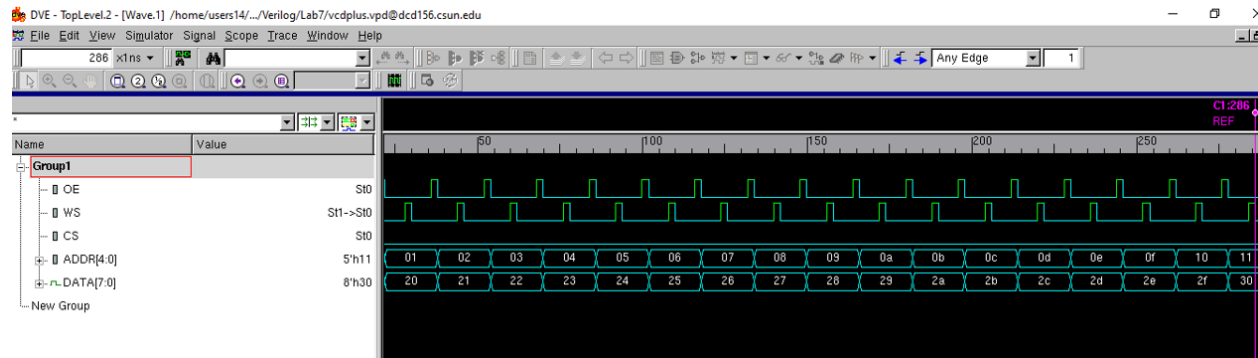
e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab6.log” command.

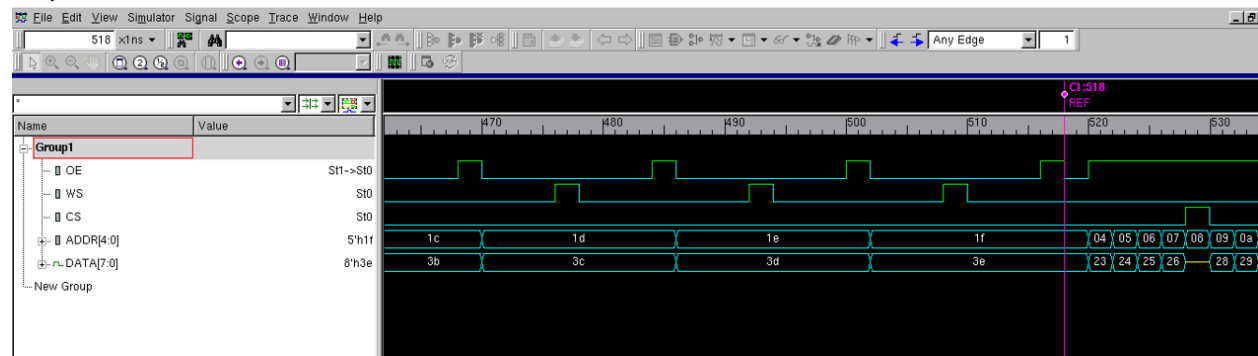
f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.

Test Strategy 1:

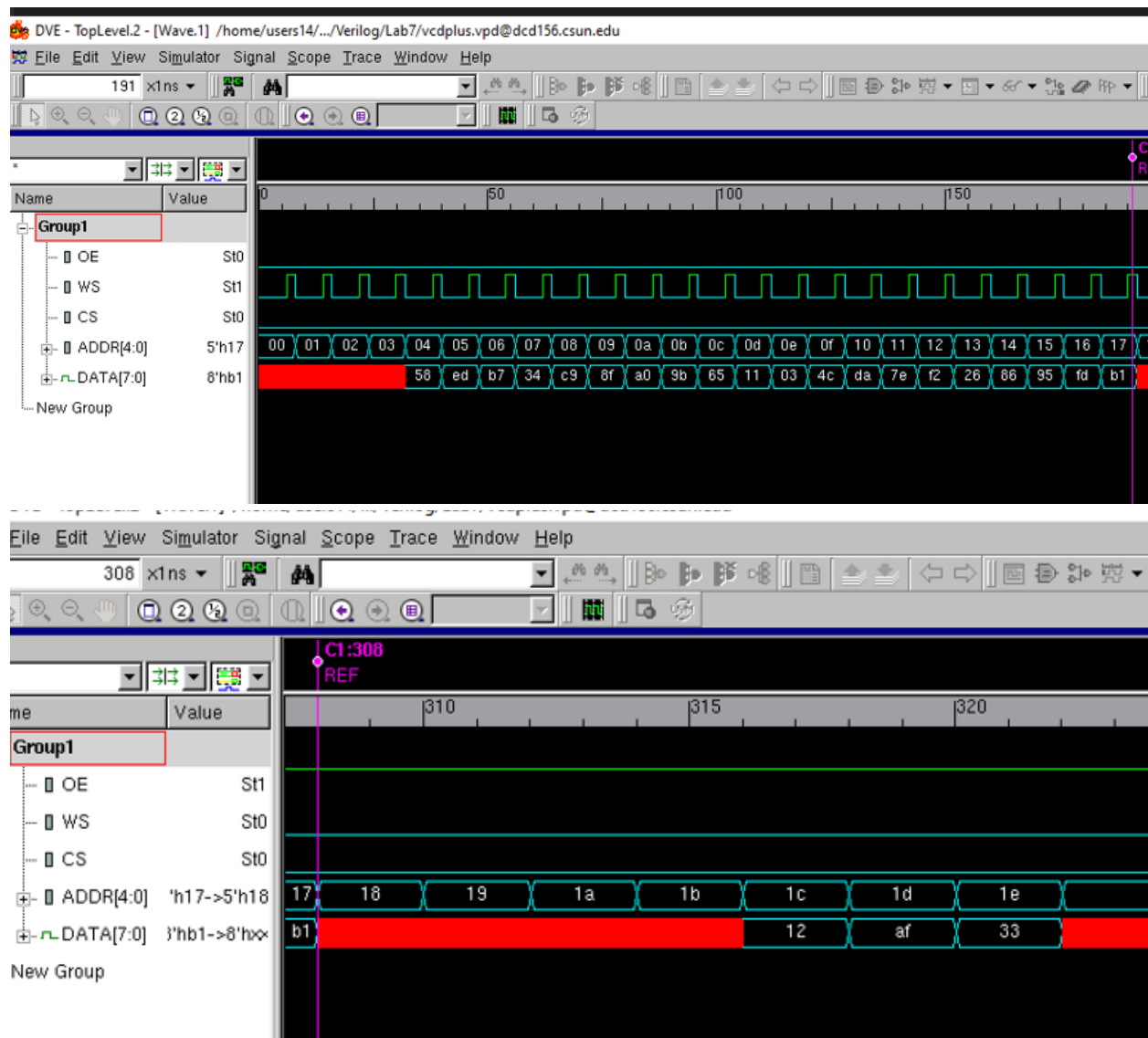


First, the register file was written to with unique values for each address using the first testbench. As shown above, the address starts at 00 (in hex), while the values assigned start at 31 (or 1F in hex) and incremented by 1 each time. Then each address was read from individually after writing to. Note that the data line only started storing upon the enabling of the chip select.

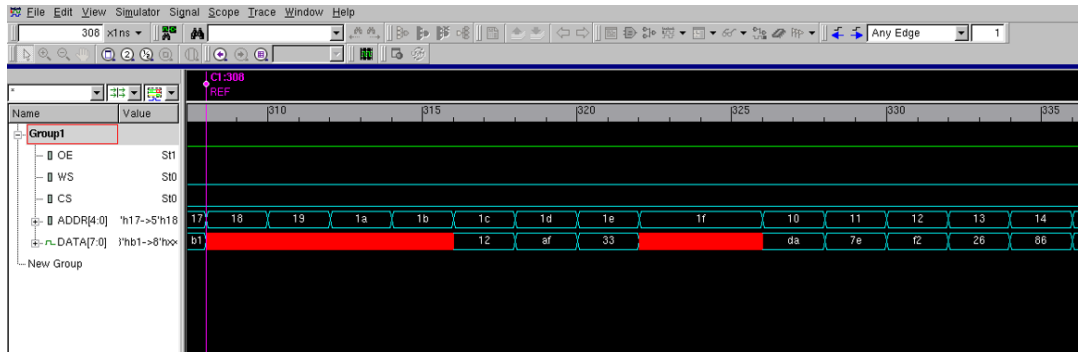


As shown above, the register file’s address ends at 31 (or 1F hex), corresponding to the default width of the register of 32. Each address was filled with unique values.

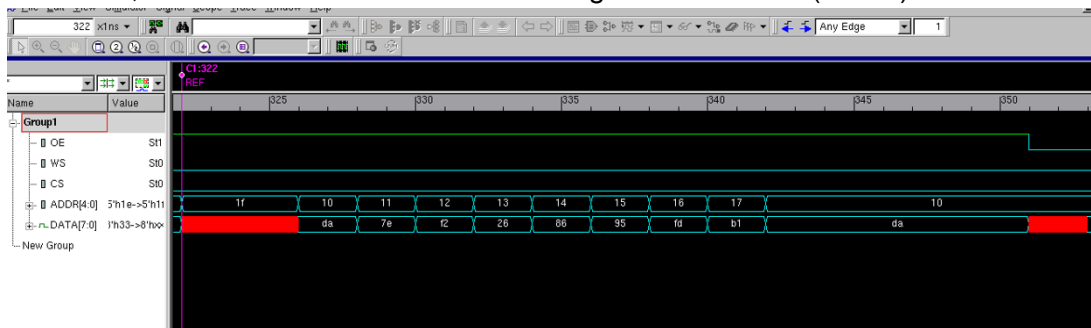
Test Strategy 2:



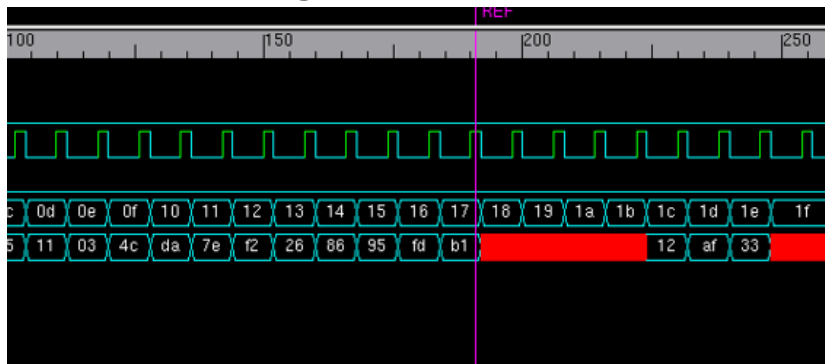
Shown above is the waveform that resulted from applying the second test bench. First the memory in the register model was initialized with the contents of a separate file ("INIT.txt"). All memory locations were accessed, but those without a value as specified in the data file, or have unspecified locations, remained uninitialized. This can be seen in the waveform above as the x construct, i.e. addresses 18 to 1b are x or uninitialized. Shown below is the period that output enable was triggered to high. The values stored were confirmed at this point as the data line is fed with these values during the read cycle.



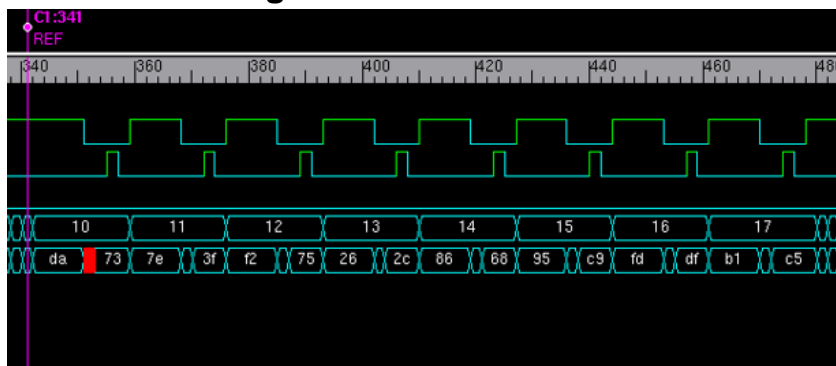
The next functionality demonstrated by the test bench involves scrambling part of the data in the memory. First, an address was read from memory during the read cycle. As the cycle was turned off, the value was scrambled according to instructions. (Below)



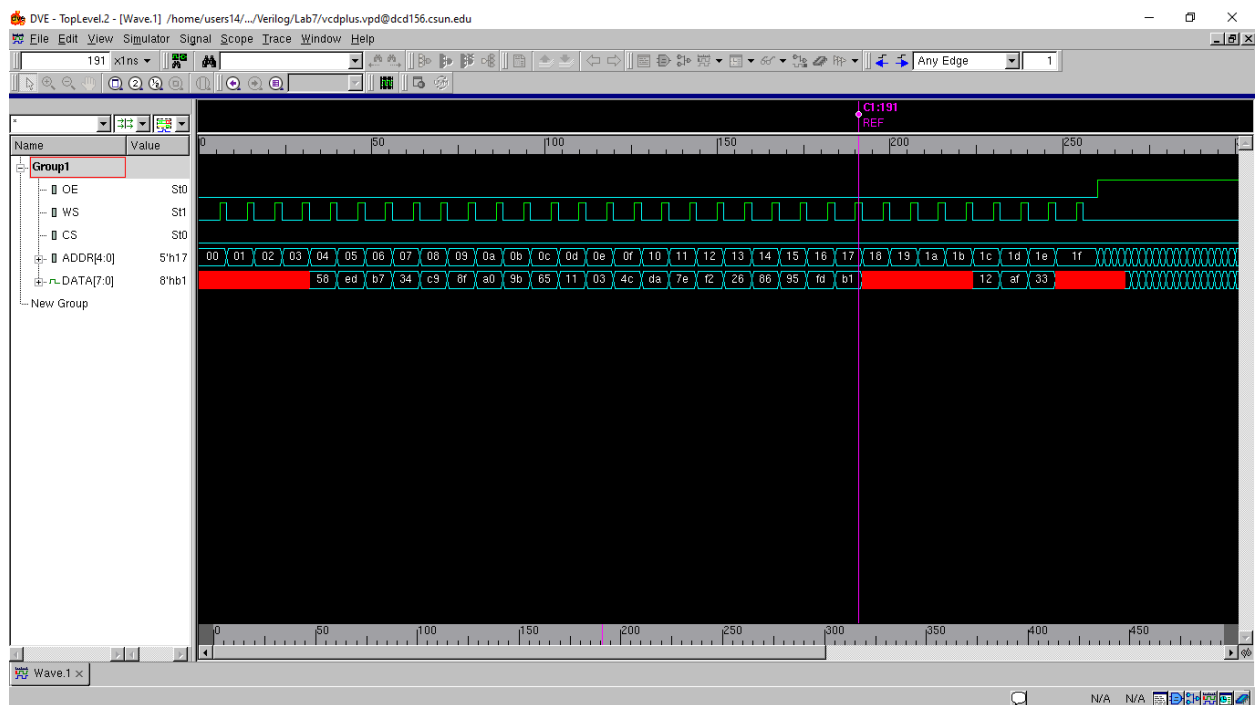
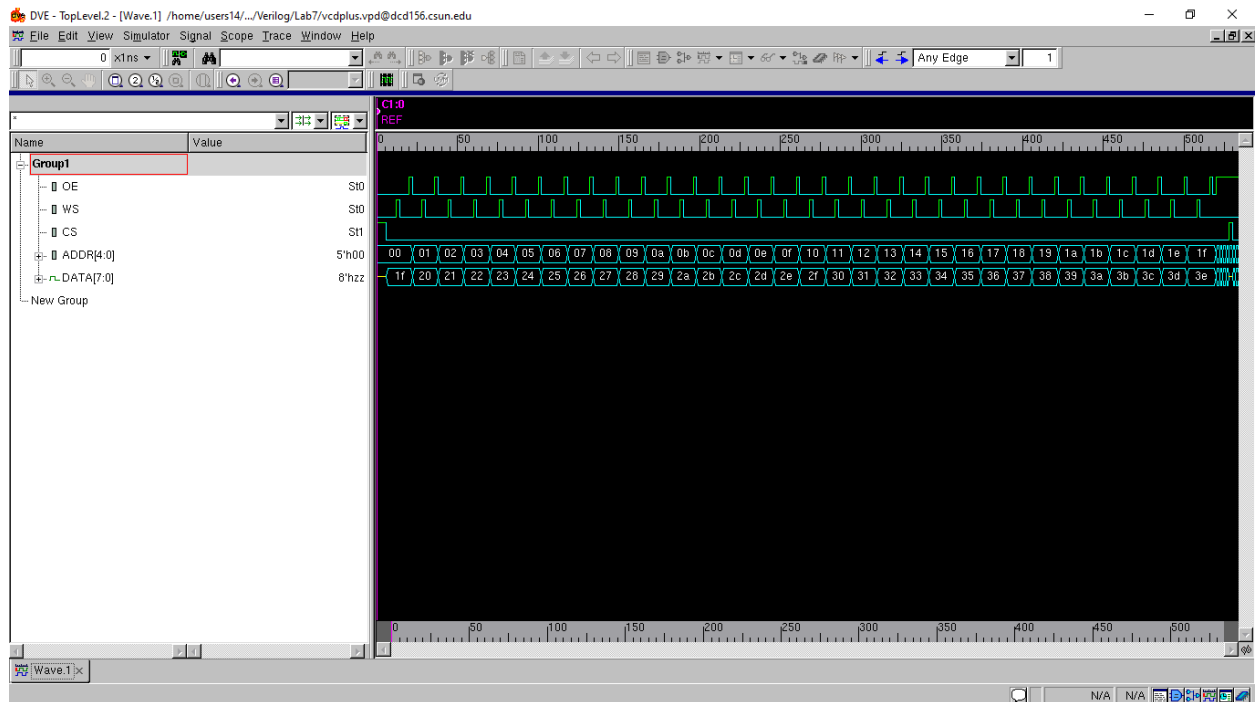
Before Scrambling



After Scrambling



Waveforms:



Lab report Extra Credit question: How many edge constructs do you use in your models?

Ans -

I used one edge construct in this model which is "posedge WS".

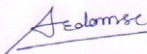
Conclusion:

The register file model was successfully tested of its storing capabilities. The bidirectional data line also functioned as intended. All memory locations were successfully written to and read from, while also confirming the overriding functionality of the chip select line (memory enable). Individual and block read capabilities were also tested and confirmed. The read and write functions were confirmed of their functionality further using the second test bench and scrambling a segment of the memory. In this experiment, only one edge construct was used in the register file module.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)



Date : 16-April-2023

