

# California State University, Northridge

Department of Electrical & Computer Engineering



ECE 526L

Lab 4 Report

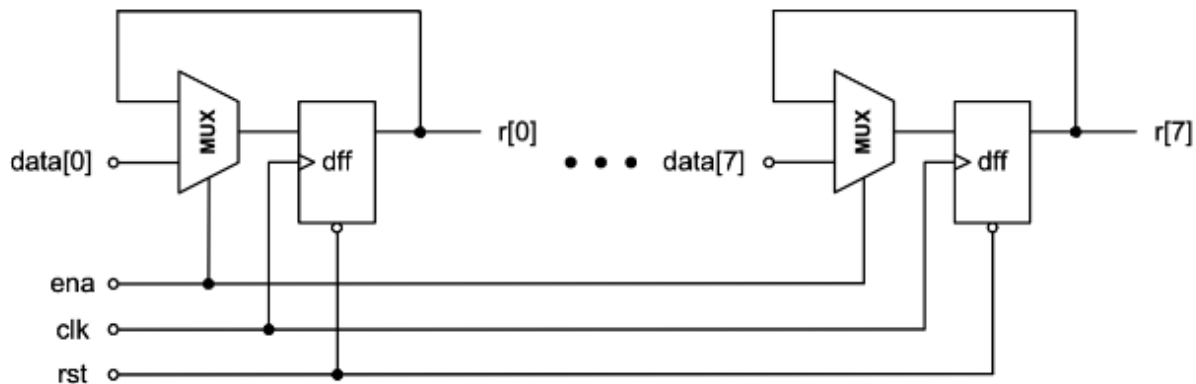
By

Avinash Damse

CSUN ID- 203131064

## 1: Introduction

The objective of this lab is to build Verilog model for 8-Bit Register using an edge triggered D Flipflop which I have already implemented in Lab 3 and verify the functionality of 8 Bit register.



**Schematic for 8-bit Register with Clear**  
**Figure 3**

Here we have to use one more module that is MUX2\_1 and DFF which we already used in LAB3.

**Delays :** These are the delays we are going to use for this Lab 4

Primary_out	2.0 ns
Fan_out_1	0.5 ns
Fan_out_2	0.8 ns
Fan_out_3	1.0 ns
Time_delay_1	3 ns
Time_delay_2	4 ns
Time_delay_3	5 ns

## **2: Procedure**

### **a. Part 1: Creating MUX2\_1 Module**

In this lab I have created a MUX2\_1 module for 2 to 1 multiplexer. Inside the module I have assigned "A, B and SEL" as input variables and "OUT" as output variables. Then I performed "NOT", two "AND" and "OR" operations according to the circuit of 2\_1 MUX. After completing the code I ended the module using and saved the file with name "MUX2\_1.v".

### **b. Part 2: Creating Register Module**

In this lab I have created a module of a given Register circuit. Inside the module I have assigned "CLK, ENA, RST and DATA" as input variables and "R" as output variables. Then I performed operations using MUX2\_1 module and D Flipflop which I created for LAB3 . After completing the code I ended the module using and saved the file with name "REGISTER.v".

### **c. Part 3: Creating REG\_test Module**

I have written the test bench for the REGISTER module code after creating my module. We require test bench just to make sure that the module we have created is working properly. In this lab, I have written the test bench and saved the file as "REG\_test.v".

### **d. Part 4: Creating ".f " file for execution.**

I have created Lab4.f file and wrote "vcs -debug -full64 SR\_Latch2.v DFF.v MUX2\_1.v REGISTER.v REG\_test.v" command in that file.

Now using "chmod +x Lab4.f" followed by "./Lab4.f" command I executed the file.

## e. Part 5: Simulation

After an execution of all modules, I have run the command “simv” for simulation.

The image displays two screenshots of a MobaXterm terminal window, showing the execution of a Verilog simulation. The terminal window is titled "DCD156.csun.edu (ad477306)". The left sidebar shows a file explorer with various files, including "simv.dadr", "DVEfiles", "csrc", "vcdplus.vpd", "vcdkey", "SR\_Latch2.v", "simv", "REGISTER.v", "REG\_test.v", "MUX2\_1.v", "Lab4.log", "Lab4.f", and "DFF.v". The main terminal area shows the output of the simulation, which is a series of lines representing the state of the simulation at different time steps. The output is divided into two sections: "\*\*\*\*\*Simulation\*\*\*\*\*" and "\*\*\*\*\*ENABLE LOW\*\*\*\*\*". The first section shows the initial state of the simulation, with values for "R=" and "DATA=" for various components. The second section shows the simulation progress, with values for "HIGHT=" and "DATA=" for various components. The simulation is running on a system with 3.00GB of RAM and 3.00GB of free space. The terminal window also shows a status bar at the bottom with the text "UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net".

```
DCD156.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/home/users14/ad477306/VerilogLe
Name
simv.dadr
DVEfiles
csrc
vcdplus.vpd
vcdkey
SR_Latch2.v
simv
REGISTER.v
REG_test.v
MUX2_1.v
Lab4.log
Lab4.f
DFF.v
Remote monitoring
Follow terminal folder

VCD+ Writer N-2017.12-SP2-9_Full64 Copyright (c) 1991-2017 by Synopsys Inc.
*****Simulation*****
20 R= xxxxxxxx CLK = 1 DATA = xxxxxxxx
24 R= 00000000 CLK = 1 DATA = xxxxxxxx
40 R= 00000000 CLK = 0 DATA = xxxxxxxx
60 R= 00000000 CLK = 1 DATA = xxxxxxxx
80 R= 00000000 CLK = 0 DATA = xxxxxxxx
100 R= 00000000 CLK = 1 DATA = 00000000
120 R= 00000000 CLK = 0 DATA = 00000000
140 R= 00000000 CLK = 1 DATA = 00000000
160 R= 00000000 CLK = 0 DATA = 00000000
180 R= 00000000 CLK = 1 DATA = 00000000
*****ENABLE LOW*****
220 R= 00000000 CLK = 1 DATA = 11111111
240 R= 00000000 CLK = 0 DATA = 11111111
260 R= 00000000 CLK = 1 DATA = 11111111
280 R= 00000000 CLK = 0 DATA = 11111111
300 R= 00000000 CLK = 1 DATA = 11111111
320 R= 00000000 CLK = 0 DATA = 11111111
340 R= 00000000 CLK = 1 DATA = 11111111
360 R= 00000000 CLK = 0 DATA = 10101010
380 R= 00000000 CLK = 1 DATA = 10101010
400 R= 00000000 CLK = 0 DATA = 10101010
416 R= 10101010 CLK = 0 DATA = 10101010
420 R= 10101010 CLK = 1 DATA = 10101010
440 R= 10101010 CLK = 0 DATA = 10101010
460 R= 10101010 CLK = 1 DATA = 10101010
480 R= 10101010 CLK = 0 DATA = 10101010
500 R= 10101010 CLK = 1 DATA = 10101010
520 R= 10101010 CLK = 0 DATA = 00001111
540 R= 10101010 CLK = 1 DATA = 00001111
560 R= 10101010 CLK = 0 DATA = 00001111
572 R= 00001111 CLK = 0 DATA = 00001111
580 R= 00001111 CLK = 1 DATA = 00001111
600 R= 00001111 CLK = 0 DATA = 00001111
620 R= 00001111 CLK = 1 DATA = 00001111
640 R= 00001111 CLK = 0 DATA = 00001111
660 R= 00001111 CLK = 1 DATA = 00001111

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

Type here to search
56°F
22:23
09-03-2023

DCD156.csun.edu (ad477306)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/home/users14/ad477306/VerilogLe
Name
simv.dadr
DVEfiles
csrc
vcdplus.vpd
vcdkey
SR_Latch2.v
simv
REGISTER.v
REG_test.v
MUX2_1.v
Lab4.log
Lab4.f
DFF.v
Remote monitoring
Follow terminal folder

800 R= 11110000 CLK = 0 DATA = 11110000
820 R= 11110000 CLK = 1 DATA = 11110000
*****ENABLE HIGH*****
860 R= 11110000 CLK = 1 DATA = 11111111
880 R= 11110000 CLK = 0 DATA = 11111111
892 R= 11111111 CLK = 0 DATA = 11111111
900 R= 11111111 CLK = 1 DATA = 11111111
920 R= 11111111 CLK = 0 DATA = 11111111
940 R= 11111111 CLK = 1 DATA = 11111111
960 R= 11111111 CLK = 0 DATA = 11111111
980 R= 11111111 CLK = 1 DATA = 11111111
1000 R= 11111111 CLK = 0 DATA = 10101010
1020 R= 11111111 CLK = 1 DATA = 10101010
1040 R= 11111111 CLK = 0 DATA = 10101010
1060 R= 11111111 CLK = 1 DATA = 10101010
1080 R= 11111111 CLK = 0 DATA = 10101010
1100 R= 11111111 CLK = 1 DATA = 10101010
1120 R= 11111111 CLK = 0 DATA = 10101010
1140 R= 11111111 CLK = 1 DATA = 10101010
1160 R= 11111111 CLK = 0 DATA = 00001111
1180 R= 11111111 CLK = 1 DATA = 00001111
1200 R= 11111111 CLK = 0 DATA = 00001111
1220 R= 11111111 CLK = 1 DATA = 00001111
1240 R= 11111111 CLK = 0 DATA = 00001111
1260 R= 11111111 CLK = 1 DATA = 00001111
1280 R= 11111111 CLK = 0 DATA = 00001111
1300 R= 11111111 CLK = 1 DATA = 00001111
1320 R= 11111111 CLK = 0 DATA = 11110000
1340 R= 11111111 CLK = 1 DATA = 11110000
1360 R= 11111111 CLK = 0 DATA = 11110000
1380 R= 11111111 CLK = 1 DATA = 11110000
1400 R= 11111111 CLK = 0 DATA = 11110000
1420 R= 11111111 CLK = 1 DATA = 11110000
1440 R= 11111111 CLK = 0 DATA = 11110000
1460 R= 11111111 CLK = 1 DATA = 11110000
1480 R= 11111111
1500 R= 11111111 CLK = 1 DATA = 11111111
1520 R= 11111111 CLK = 0 DATA = 11111111

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: https://mobaxterm.mobatek.net

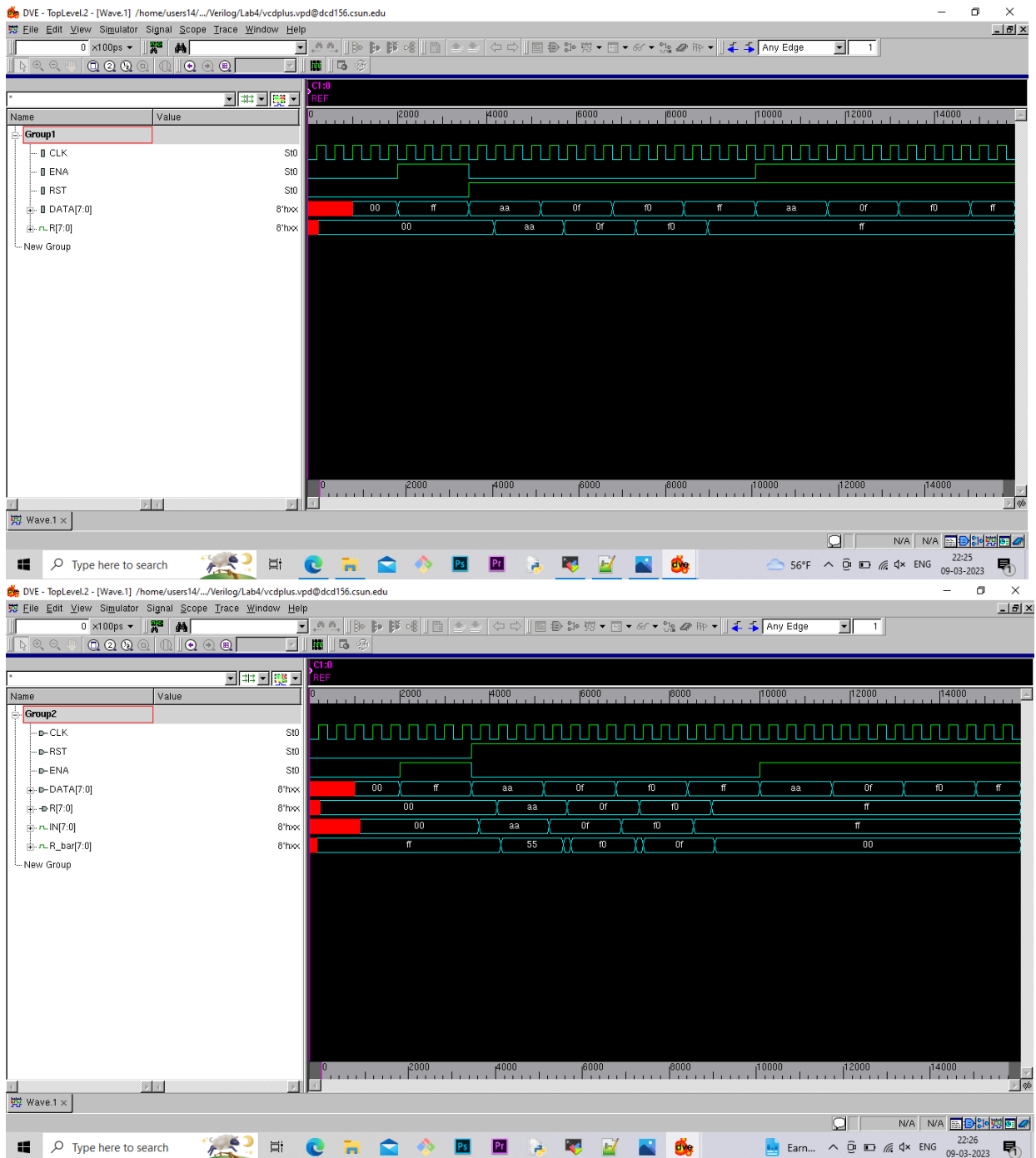
Type here to search
56°F
22:23
09-03-2023
```

### e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab4.log” command.

### f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.



## Lab report question

### What is the maximum operating frequency for your circuit?

The Longest delay of DFF is 43.1 ns.

The Longest Delay of MUX is 14.5 ns.

Total Delay of whole circuit = 57.6 ns.

The maximum operating frequency for circuit is  $= 1 / \text{longest delay}$

$$= 1/57.6$$

$$= 0.01736 \times 10^9 \text{ Hz}$$

$$= 1.7 \times 10^7 \text{ Hz}$$

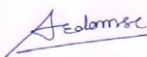
## Conclusion:

The 8-bit register designed in this experiment was verified for its asynchronous reset function as well as its synchronous enable line. The calculated maximum operating frequency also corresponded to the timing simulation of the design. Exceeding the maximum operating frequency produces a random propagation of the software construct 'X', or unknown, through the output.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)

A handwritten signature in blue ink, appearing to read 'Avinash Damse', is enclosed within a light purple rectangular box.

Date : 09-03-2023