California State University, Northridge

Department of Electrical & Computer Engineering

ECE 526L

Lab 4 Report

By

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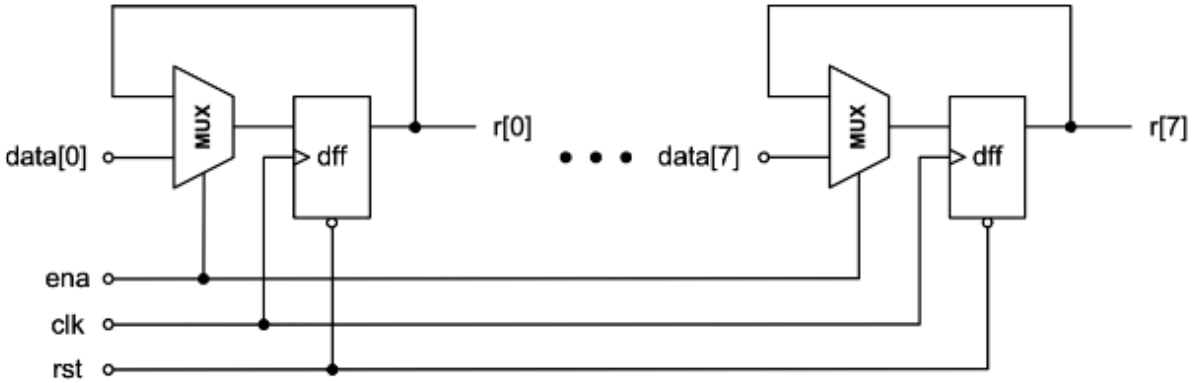
1: Introduction

The objective of this lab is to build Verilog model for 8-Bit Register using an edge triggered D Flipflop which I have already implemented in Lab 3 and verify the functionality of 8 Bit register.



Schematic for 8-bit Register with Clear
Figure 3

Here we have to use one more module that is MUX2_1 and DFF wich we already used in LAB3.

Delays : These are the delay we are going to use for this Lab 4

Primary_out	2.0 ns
Fan_out_1	0.5 ns
Fan_out_2	0.8 ns
Fan_out_3	1.0 ns
Time_delay_1	3 ns
Time_delay_2	4 ns
Time_delay_3	5 ns

2: Procedure

a. Part 1: Creating MUX2_1 Module

In this lab I have created a MUX2_1 module for 2 to 1 multiplexer. Inside the module I have assigned “A, B and SEL” as input variables and “OUT” as output variables. Then I performed “NOT”, two “AND” and “OR”operations according to the circuit of 2_1 MUX. After completing the code I ended the module using and saved the file with name “MUX2_1.v”.

b. Part 2: Creating Register Module

In this lab I have created a module of a given Register circuit. Inside the module I have assigned “CLK, ENA, RST and DATA” as input variables and “R” as output variables. Then I performed operations using MUX2_1 module and D Flipflop which I created for LAB3 . After completing the code I ended the module using and saved the file with name “REGISTER.v”.

c. Part 3: Creating REG_test Module

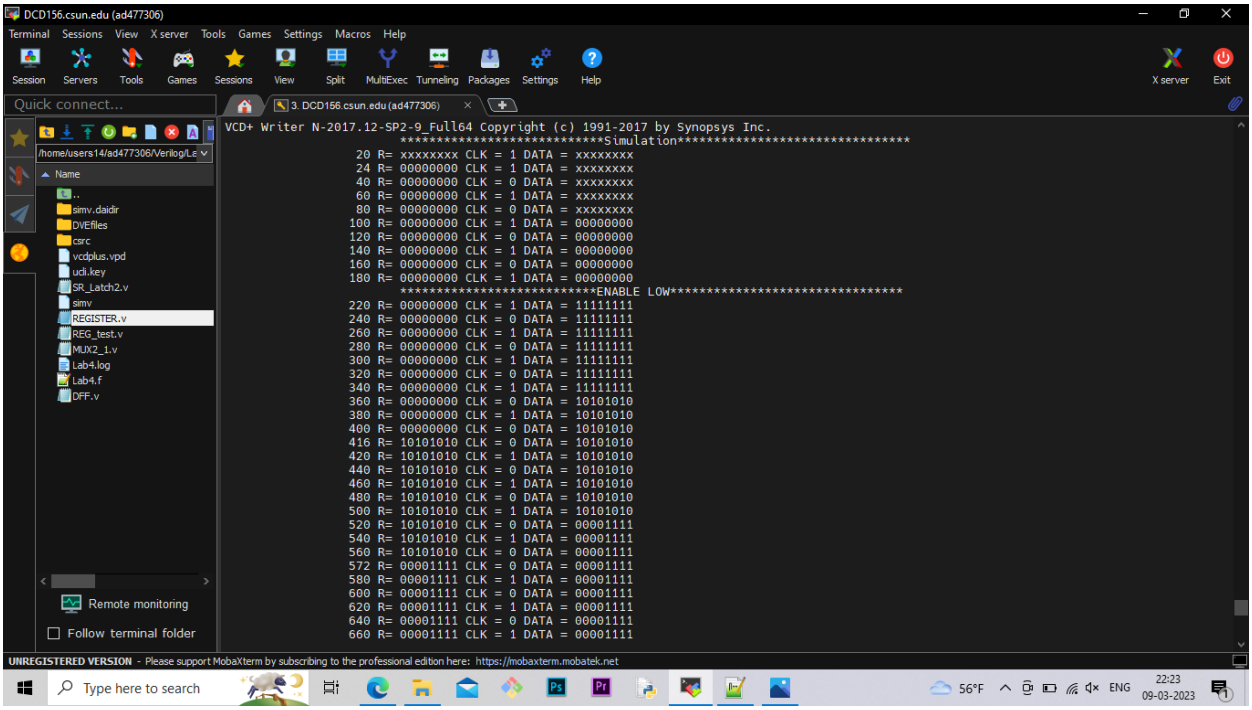
I have written the test bench for the REGISTER module code after creating my module. We require test bench just to make sure that the module we have created is working properly. In this lab, I have written the test bench and saved the file as “REG_test.v”.

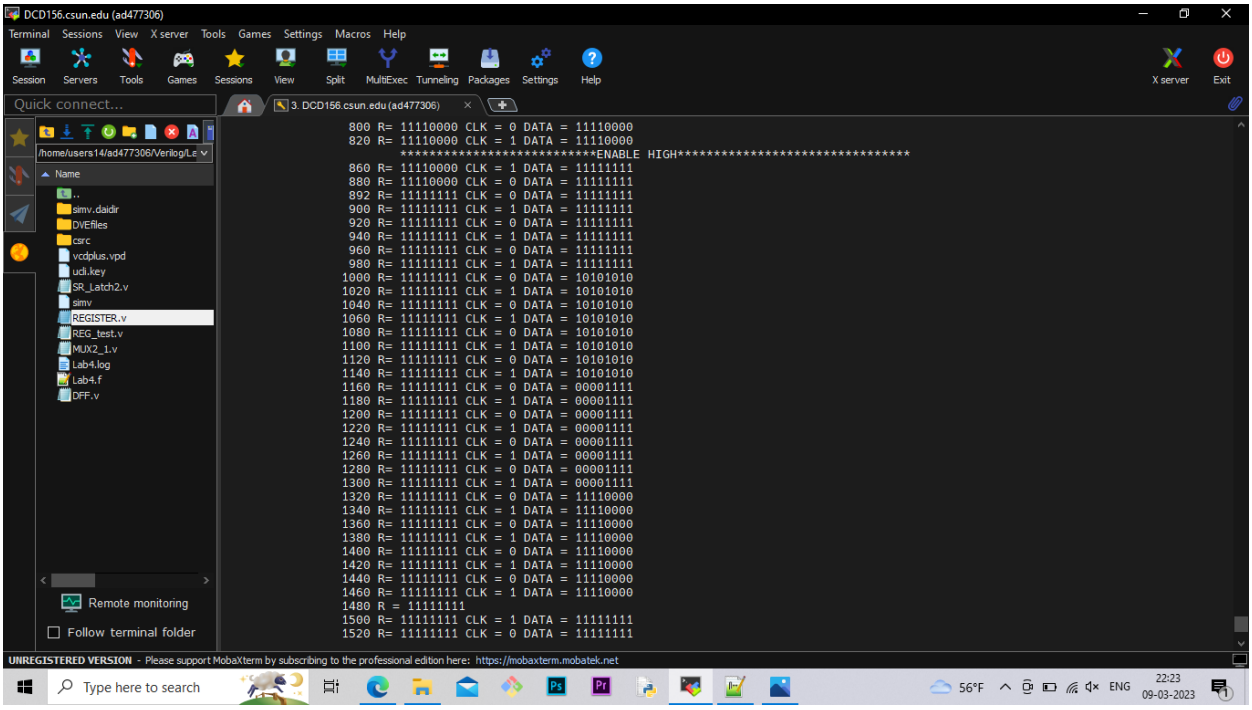
d. Part 4: Creating “.f ” file for execution.

I have created Lab4.f file and wrote “vcs -debug -full64 SR_Latch2.v DFF.v MUX2_1.v REGISTER.v REG_test.v” command in that file.
Now using “chmod +x Lab4.f” followed by “./Lab4.f” command I executed the file.

e. Part 5: Simulation

After an execution of all modules, I have run the command “simv” for simulation.



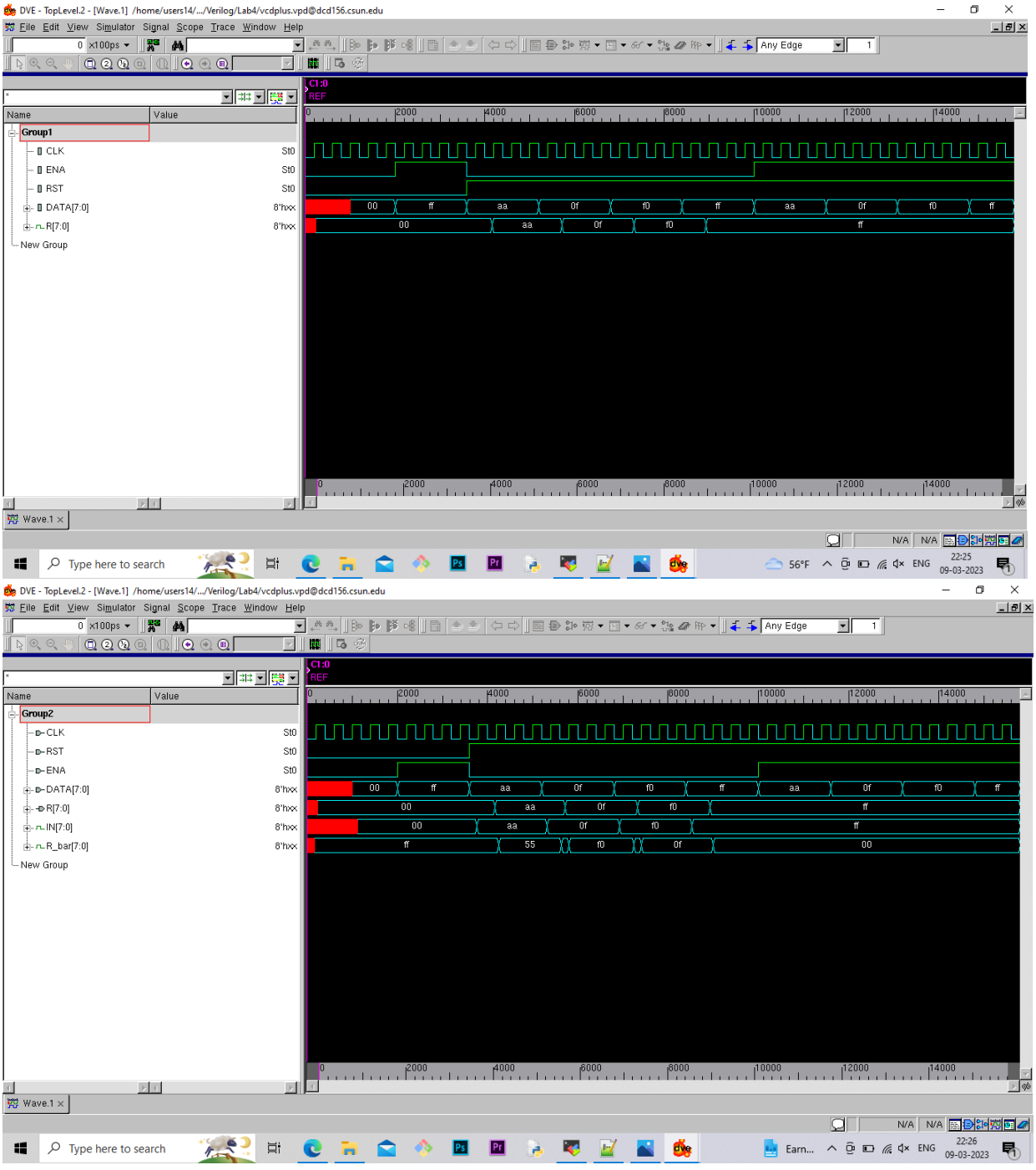


e. Part 5: Creating Log File

After running the simulation I created the log file using the “simv -l Lab4.log” command.

f. Part 6: Seeing the waveform.

After creating the log file I opened the DVE using “dve -full64 &” command to see the waveforms.



Lab report question

What is the maximum operating frequency for your circuit?

The Longest delay of DFF is 43.1 ns.
The Longest Delay of MUX is 14.5 ns.

Total Delay of whole circuit = 57.6 ns.

The maximum operating frequency for circuit is=1/ longest delay

$$= 1/57.6$$
$$= 0.01736 \times 10^{9}\ \text{Hz}$$
$$= 1.7 \times 10^{7}\ \text{Hz}$$

Conclusion:

The 8-bit register designed in this experiment was verified for its asynchronous reset function as well as its synchronous enable line. The calculated maximum operating frequency also corresponded to the timing simulation of the design. Exceeding the maximum operating frequency produces a random propagation of the software construct 'X', or unknown, through the output.

I hereby attest that this lab report is entirely my own work. I have not copied either code or text from anyone, nor have I allowed or will I allow anyone to copy my work.

Name (printed) Avinash Damse

Name(signed)  Date : 09-03-2023