

# PIC18F2420/2520/4420/4520

## 5.3.4 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. SFRs start at the top of data memory (FFFh) and extend downward to occupy the top half of Bank 15 (F80h to FFFh). A list of these registers is given in Table 5-1 and Table 5-2.

The SFRs can be classified into two sets: those associated with the “core” device functionality (ALU, Resets and interrupts) and those related to the peripheral functions. The Reset and Interrupt registers are described in their respective chapters, while the ALU’s STATUS register is described later in this section. Registers related to the operation of a peripheral feature are described in the chapter for that peripheral.

The SFRs are typically distributed among the peripherals whose functions they control. Unused SFR locations are unimplemented and read as ‘0’s.

**TABLE 5-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2420/2520/4420/4520 DEVICES**

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2 <sup>(1)</sup>	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2 <sup>(1)</sup>	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2 <sup>(1)</sup>	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2 <sup>(1)</sup>	FBCh	CCPR2H	F9Ch	— <sup>(2)</sup>
FFBh	PCLATU	FDBh	PLUSW2 <sup>(1)</sup>	FBHh	CCPR2L	F9Bh	OSCTUNE
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	— <sup>(2)</sup>
FF9h	PCL	FD9h	FSR2L	FB9h	— <sup>(2)</sup>	F99h	— <sup>(2)</sup>
FF8h	TBLPTRU	FD8h	STATUS	FB8h	BAUDCON	F98h	— <sup>(2)</sup>
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	PWM1CON <sup>(3)</sup>	F97h	— <sup>(2)</sup>
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	ECCP1AS <sup>(3)</sup>	F96h	TRISE <sup>(3)</sup>
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD <sup>(3)</sup>
FF4h	PRODH	FD4h	— <sup>(2)</sup>	FB4h	CMCON	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	HLVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	— <sup>(2)</sup>
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	— <sup>(2)</sup>
FEFh	INDF0 <sup>(1)</sup>	FCFh	TMR1H	FAFh	SPBRG	F8Fh	— <sup>(2)</sup>
FEEh	POSTINC0 <sup>(1)</sup>	FCEh	TMR1L	FAEh	RCREG	F8Eh	— <sup>(2)</sup>
FEDh	POSTDEC0 <sup>(1)</sup>	FCDh	T1CON	FADh	TXREG	F8Dh	LATE <sup>(3)</sup>
FECh	PREINC0 <sup>(1)</sup>	FCCh	TMR2	FACH	TXSTA	F8Ch	LATD <sup>(3)</sup>
FEBh	PLUSW0 <sup>(1)</sup>	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	— <sup>(2)</sup>	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADDD	FA8h	EEDATA	F88h	— <sup>(2)</sup>
FE7h	INDF1 <sup>(1)</sup>	FC7h	SSPSTAT	FA7h	EECON2 <sup>(1)</sup>	F87h	— <sup>(2)</sup>
FE6h	POSTINC1 <sup>(1)</sup>	FC6h	SSPCON1	FA6h	EECON1	F86h	— <sup>(2)</sup>
FE5h	POSTDEC1 <sup>(1)</sup>	FC5h	SSPCON2	FA5h	— <sup>(2)</sup>	F85h	— <sup>(2)</sup>
FE4h	PREINC1 <sup>(1)</sup>	FC4h	ADRESH	FA4h	— <sup>(2)</sup>	F84h	PORTE <sup>(3)</sup>
FE3h	PLUSW1 <sup>(1)</sup>	FC3h	ADRESL	FA3h	— <sup>(2)</sup>	F83h	PORTD <sup>(3)</sup>
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA

- Note 1:** This is not a physical register.  
**2:** Unimplemented registers are read as ‘0’.  
**3:** This register is not available on 28-pin devices.

# PIC18F2420/2520/4420/4520

**TABLE 5-2: PIC18F2420/2520/4420/4520 REGISTER FILE SUMMARY**

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TOSU	—	—	—	Top-of-Stack Upper Byte (TOS<20:16>)					---0 0000	49, 54
TOSH	Top-of-Stack High Byte (TOS<15:8>)								0000 0000	49, 54
TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	49, 54
STKPTR	STKFUL	STKUNF	—	SP4	SP3	SP2	SP1	SP0	00-0 0000	49, 55
PCLATU	—	—	—	Holding Register for PC<20:16>					---0 0000	49, 54
PCLATH	Holding Register for PC<15:8>								0000 0000	49, 54
PCL	PC Low Byte (PC<7:0>)								0000 0000	49, 54
TBLPTRU	—	—	bit 21	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					--00 0000	49, 76
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)								0000 0000	49, 76
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	49, 76
TABLAT	Program Memory Table Latch								0000 0000	49, 76
PRODH	Product Register High Byte								xxxx xx	49, 89
PRODL	Product Register Low Byte								xxxx xx	49, 89
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	49, 93
INTCON2	RBPV	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	1111 -1-1	49, 94
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	11-0 0-00	49, 95
INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)								N/A	49, 69
POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)								N/A	49, 69
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)								N/A	49, 69
PREINC0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register)								N/A	49, 69
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								N/A	49, 69
FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0 High Byte				---- 0000	49, 69
FSR0L	Indirect Data Memory Address Pointer 0 Low Byte								xxxx xxxx	49, 69
WREG	Working Register								xxxx xxxx	49
INDF1	Uses contents of FSR1 to address data memory – value of FSR1 not changed (not a physical register)								N/A	49, 69
POSTINC1	Uses contents of FSR1 to address data memory – value of FSR1 post-incremented (not a physical register)								N/A	49, 69
POSTDEC1	Uses contents of FSR1 to address data memory – value of FSR1 post-decremented (not a physical register)								N/A	49, 69
PREINC1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register)								N/A	49, 69
PLUSW1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register) – value of FSR1 offset by W								N/A	49, 69
FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1 High Byte				---- 0000	50, 69
FSR1L	Indirect Data Memory Address Pointer 1 Low Byte								xxxx xxxx	50, 69
BSR	—	—	—	—	Bank Select Register				---- 0000	50, 59
INDF2	Uses contents of FSR2 to address data memory – value of FSR2 not changed (not a physical register)								N/A	50, 69
POSTINC2	Uses contents of FSR2 to address data memory – value of FSR2 post-incremented (not a physical register)								N/A	50, 69
POSTDEC2	Uses contents of FSR2 to address data memory – value of FSR2 post-decremented (not a physical register)								N/A	50, 69
PREINC2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register)								N/A	50, 69
PLUSW2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register) – value of FSR2 offset by W								N/A	50, 69
FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2 High Byte				---- 0000	50, 69
FSR2L	Indirect Data Memory Address Pointer 2 Low Byte								xxxx xxxx	50, 69
STATUS	—	—	—	N	OV	Z	DC	C	---x xxxx	50, 67

**Legend:** x = unknown, u = unchanged, – = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

- Note 1:** The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, it is disabled and reads as '0'. See **Section 4.4 “Brown-out Reset (BOR)”**.
- 2:** These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '–'.
- 3:** The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 “PLL in INTOSC Modes”**.
- 4:** The RE3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0); otherwise, RE3 reads as '0'. This bit is read-only.
- 5:** RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

# PIC18F2420/2520/4420/4520

**TABLE 5-2: PIC18F2420/2520/4420/4520 REGISTER FILE SUMMARY (CONTINUED)**

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TMR0H	Timer0 Register High Byte								0000 0000	50, 125
TMR0L	Timer0 Register Low Byte								xxxx xxxx	50, 125
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111	50, 123
OSCCON	IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0	0100 q000	30, 50
HLVDCON	VDIRMAG	—	IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0	0-00 0101	50, 245
WDTCON	—	—	—	—	—	—	—	SWDTEN	--- --0	50, 259
RCON	IPEN	SBOREN <sup>(1)</sup>	—	RI	TO	PD	POR	BOR	0q-1 11q0	42, 48, 102
TMR1H	Timer1 Register High Byte								xxxx xxxx	50, 132
TMR1L	Timer1 Register Low Bytes								xxxx xxxx	50, 132
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	50, 127
TMR2	Timer2 Register								0000 0000	50, 134
PR2	Timer2 Period Register								1111 1111	50, 134
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	50, 133
SSPBUF	MSSP Receive Buffer/Transmit Register								xxxx xxxx	50, 169, 170
SSPADD	MSSP Address Register in I <sup>2</sup> C™ Slave Mode. MSSP Baud Rate Reload Register in I <sup>2</sup> C Master Mode.								0000 0000	50, 170
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	50, 162, 171
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	50, 163, 172
SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	50, 173
ADRESH	A/D Result Register High Byte								xxxx xxxx	51, 232
ADRESL	A/D Result Register Low Byte								xxxx xxxx	51, 232
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	--00 0000	51, 223
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0qqq	51, 224
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	0-00 0000	51, 225
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	51, 140
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	51, 140
CCP1CON	P1M1 <sup>(2)</sup>	P1M0 <sup>(2)</sup>	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	51, 139, 147
CCPR2H	Capture/Compare/PWM Register 2 High Byte								xxxx xxxx	51, 140
CCPR2L	Capture/Compare/PWM Register 2 Low Byte								xxxx xxxx	51, 140
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	51, 139
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	0100 0-00	51, 204
PWM1CON	PRSEN	PDC6 <sup>(2)</sup>	PDC5 <sup>(2)</sup>	PDC4 <sup>(2)</sup>	PDC3 <sup>(2)</sup>	PDC2 <sup>(2)</sup>	PDC1 <sup>(2)</sup>	PDC0 <sup>(2)</sup>	0000 0000	51, 156
ECCP1AS	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1 <sup>(2)</sup>	PSSBD0 <sup>(2)</sup>	0000 0000	51, 157
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	51, 239
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	51, 233
TMR3H	Timer3 Register High Byte								xxxx xxxx	51, 137
TMR3L	Timer3 Register Low Byte								xxxx xxxx	51, 137
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	51, 135

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

**Note 1:** The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, it is disabled and reads as '0'. See **Section 4.4 "Brown-out Reset (BOR)"**.

**2:** These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '—'.

**3:** The PLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 "PLL in INTOSC Modes"**.

**4:** The RE3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0); otherwise, RE3 reads as '0'. This bit is read-only.

**5:** RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

# PIC18F2420/2520/4420/4520

**TABLE 5-2: PIC18F2420/2520/4420/4520 REGISTER FILE SUMMARY (CONTINUED)**

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
SPBRGH	EUSART Baud Rate Generator Register High Byte								0000 0000	51, 206
SPBRG	EUSART Baud Rate Generator Register Low Byte								0000 0000	51, 206
RCREG	EUSART Receive Register								0000 0000	51, 213
TXREG	EUSART Transmit Register								0000 0000	51, 211
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	51, 202
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	51, 203
EEADR	EEPROM Address Register								0000 0000	51, 74, 83
EEDATA	EEPROM Data Register								0000 0000	51, 74, 83
EECON2	EEPROM Control Register 2 (not a physical register)								0000 0000	51, 74, 83
EECON1	EEPGD	CFGFS	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	51, 75, 84
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	11-1 1111	52, 101
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	00-0 0000	52, 97
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	00-0 0000	52, 99
IPR1	PSPIP <sup>(2)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	1111 1111	52, 100
PIR1	PSPIF <sup>(2)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	52, 96
PIE1	PSPIE <sup>(2)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	52, 98
OSCTUNE	INTSRC	PLLEN <sup>(3)</sup>	—	TUN4	TUN3	TUN2	TUN1	TUN0	0q-0 0000	27, 52
TRISE <sup>(2)</sup>	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	0000 -111	52, 118
TRISD <sup>(2)</sup>	PORTD Data Direction Register								1111 1111	52, 114
TRISC	PORTC Data Direction Register								1111 1111	52, 111
TRISB	PORTB Data Direction Register								1111 1111	52, 108
TRISA	TRISA7 <sup>(5)</sup>	TRISA6 <sup>(5)</sup>	PORTA Data Direction Register						1111 1111	52, 105
LATE <sup>(2)</sup>	—	—	—	—	—	PORTE Data Latch Register (Read and Write to Data Latch)			---- -xxx	52, 117
LATD <sup>(2)</sup>	PORTD Data Latch Register (Read and Write to Data Latch)								xxxx xxxx	52, 114
LATC	PORTC Data Latch Register (Read and Write to Data Latch)								xxxx xxxx	52, 111
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								xxxx xxxx	52, 108
LATA	LATA7 <sup>(5)</sup>	LATA6 <sup>(5)</sup>	PORTA Data Latch Register (Read and Write to Data Latch)						xxxx xxxx	52, 105
PORTE	—	—	—	—	RE3 <sup>(4)</sup>	RE2 <sup>(2)</sup>	RE1 <sup>(2)</sup>	RE0 <sup>(2)</sup>	---- xxxx	52, 117
PORTD <sup>(2)</sup>	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	52, 114
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	52, 111
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	52, 108
PORTA	RA7 <sup>(5)</sup>	RA6 <sup>(5)</sup>	RA5	RA4	RA3	RA2	RA1	RA0	xx0x 0000	52, 105

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition. Shaded cells are unimplemented, read as '0'.

**Note 1:** The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, it is disabled and reads as '0'. See

**Section 4.4 “Brown-out Reset (BOR)”**.

**2:** These registers and/or bits are not implemented on 28-pin devices and are read as '0'. Reset values are shown for 40/44-pin devices; individual unimplemented bits should be interpreted as '—'.

**3:** The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 “PLL in INTOSC Modes”**.

**4:** The RE3 bit is only available when Master Clear Reset is disabled (MCLRE Configuration bit = 0); otherwise, RE3 reads as '0'. This bit is read-only.

**5:** RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.