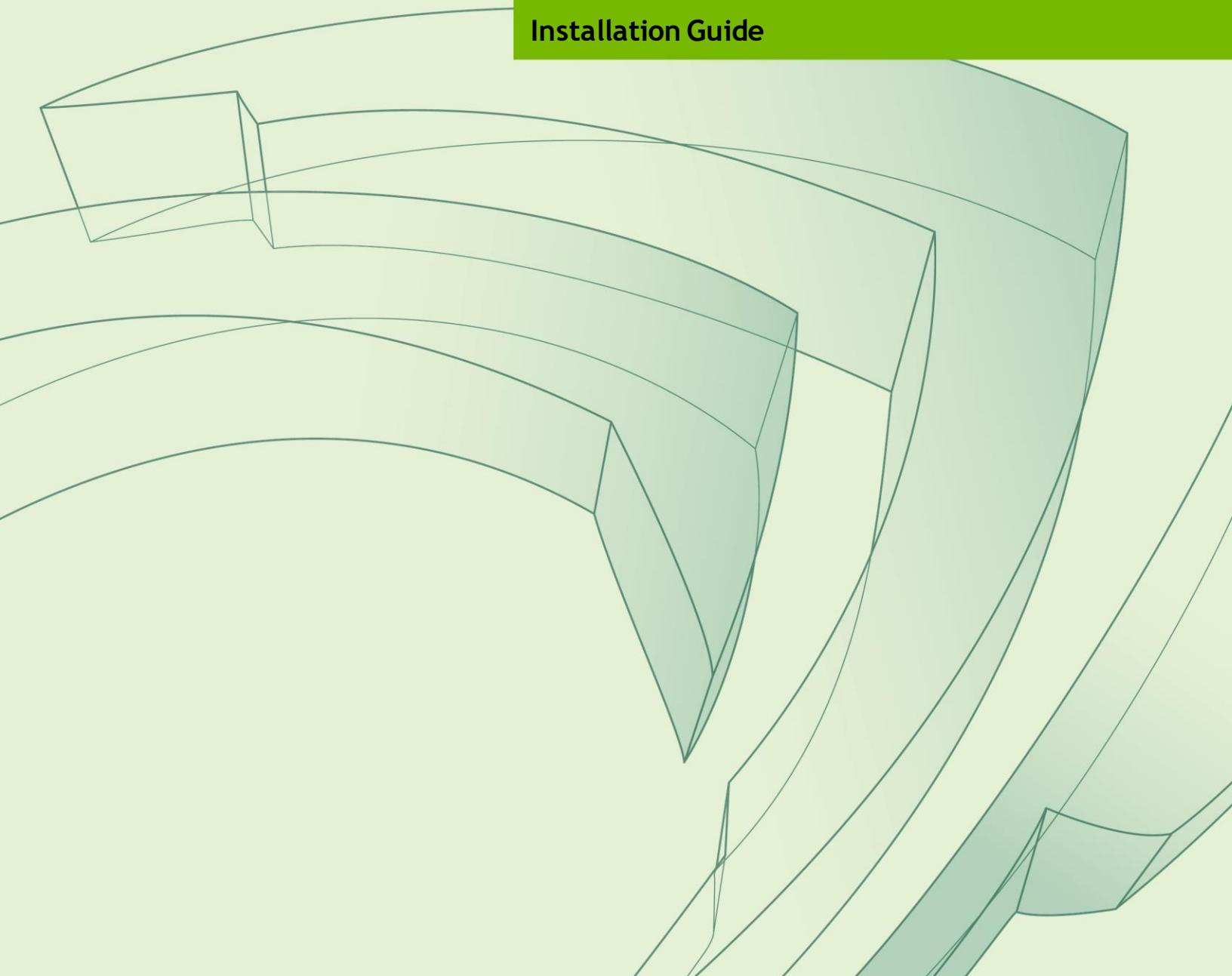




# NVIDIA DRIVE AGX SYSTEM MECHANICAL INSTALLATION GUIDE

DI-08957-001\_v09 | August 2020  
NVIDIA CONFIDENTIAL | Prepared and Provided Under NDA

## Installation Guide



## DOCUMENT CHANGE HISTORY

DI-08957-001\_v09

Version	Date	Authors	Description of Change
01	March 21, 2018	JH, VS	Initial release
02	May 31, 2018	JH, VS	<ul style="list-style-type: none"> <li>• Updated figures with the new thicker baseplate</li> <li>• Updated the 3D CAD model (see attachment)</li> <li>• Updated Table 2 numbers</li> </ul>
03	August 29, 2018	JH, VS	<ul style="list-style-type: none"> <li>• Added note for installing DDP horizontally</li> <li>• Added note for the power supply when installing DDP with configuration that includes GV100 or COM Express modules</li> <li>• Added maximum peak current requirements</li> </ul>
04	September 21, 2018	JH, VS	<ul style="list-style-type: none"> <li>• Updated nomenclature from DRIVE Development Platform (DDP) to DRIVE™ AGX Developer System</li> <li>• Minor changes to the notes in Chapter 1</li> <li>• Added inrush current and updated EDP numbers</li> </ul>
05	November 30, 2018	JH, VS	<ul style="list-style-type: none"> <li>• Added Chapter 3 for interface connections</li> <li>• Updated cable harness information</li> <li>• Updated ambient temperature information</li> </ul>
06	June 17, 2019	JH, VS	<ul style="list-style-type: none"> <li>• Updated nomenclature from NVIDIA DRIVE AGX Developer System to NVIDIA DRIVE AGX System (<i>simply referred to as “developer system” within the document</i>)</li> <li>• Corrected 10GBASE-T1 to 10GBASE-T in Table 3-10</li> <li>• Added LED information in Chapter 2</li> <li>• Updated Table 3-2 to show the cable harness CAN connections to the MCU/XA/XB/CVM CAN ports.att</li> <li>• Updated shock and vibration information</li> <li>• Updated Table 3-1 to show GMSL and GMSL2 cable lengths</li> <li>• Added note for power cycle wait time requirement</li> </ul>

Version	Date	Authors	Description of Change
07	November 11, 2019	JH, VS	<ul style="list-style-type: none"> <li>•Section 1.2: Added note regarding dimensions tolerance</li> <li>•Updated Figure 2-1 to avoid using left and right terms</li> <li>•Updated Section 3.1.3.6: KL15 Connector; updated the 125mA fuse requirement for KL15</li> <li>•Updated Section 3.1.3.1: CAN Connectors throughout; added a Table 3-5 in Section 3.1.3.1 to show CAN bus/port mapping</li> <li>•Deleted Table: GPIO Connector Pinout-32-pin Cable Harness</li> <li>•Added Table 3-8: GPIO Electrical Characteristics</li> <li>•Section 4.1: Added vibration frequency range and humidity information</li> </ul>
08	May 29, 2020	JH, VS	<ul style="list-style-type: none"> <li>•Added the required airflow specification and the airflow direction in Chapter 2.</li> <li>•Added Table 3-10: UART Connectors on Cable Harness.</li> </ul>
09	August 28, 2020	JH, VS	<ul style="list-style-type: none"> <li>•Updated Table 5-1 to highlight that 24V battery is not supported.</li> <li>•Updated Section 3.1.3.6 to add document references for information related to the KL15 function.</li> </ul>

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# Chapter 1. MECHANICAL DIMENSIONS

The NVIDIA DRIVE™ AGX Developer Kit ships with an NVIDIA DRIVE™ AGX System (hereinafter referred to simply as “**developer system**”). This developer system has a baseplate mounted at the bottom for installing the unit into the vehicle. The recommended location of mounting the developer system in the vehicle is the trunk.

The developer system includes a cooling solution to meet full performance specifications of the SOCs and provide limited redundancy protection in case a section of the thermal solution fails.

The 3D CAD model of the developer system in STEP format is provided as the following attachment to this document:

► **DDP-B03-CAD\_asm.nvzip**



**Note:** To access the attached file:

1. *Download* this PDF file to your local drive.
2. *Click* on the Attachment tab of the downloaded PDF (or the paper clip icon depending on your version of Acrobat Reader).
3. *Select* the file and use the Tool Bar options (Open, Save) to retrieve the documents.
4. *Rename* the .nvzip file to .zip before it can be extracted.

## 1.1 BASEPLATE

Figure 1-1 shows a pre-assembled developer system with its bottom baseplate.



Figure 1-1. Pre-assembled NVIDIA DRIVE AGX System

Figure 1-2 shows only the developer system baseplate, which is used for installing the unit into the vehicle.

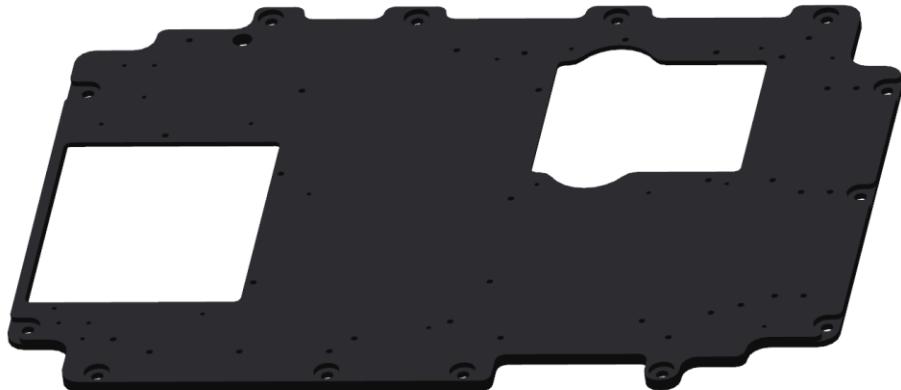


Figure 1-2. NVIDIA DRIVE AGX System Baseplate

## 1.2 TOP AND BOTTOM VIEWS WITH BASEPLATE MOUNTING DIMENSIONS

Figure 1-3 and Figure 1-4 show the top and bottom views of the developer system. The locations of the mounting holes on the baseplate are also shown in Figure 1-3.

**Note:**

1. The detailed dimensions of the developer system are showing in Figure 1-3 , Figure 1-5, Figure 1-6 and Figure 1-7.
2. The dimension unit is **mm** in all the figures in this document.
3. All dimensions shown have a tolerance of  $+/ -0.25$  mm for installation purposes.

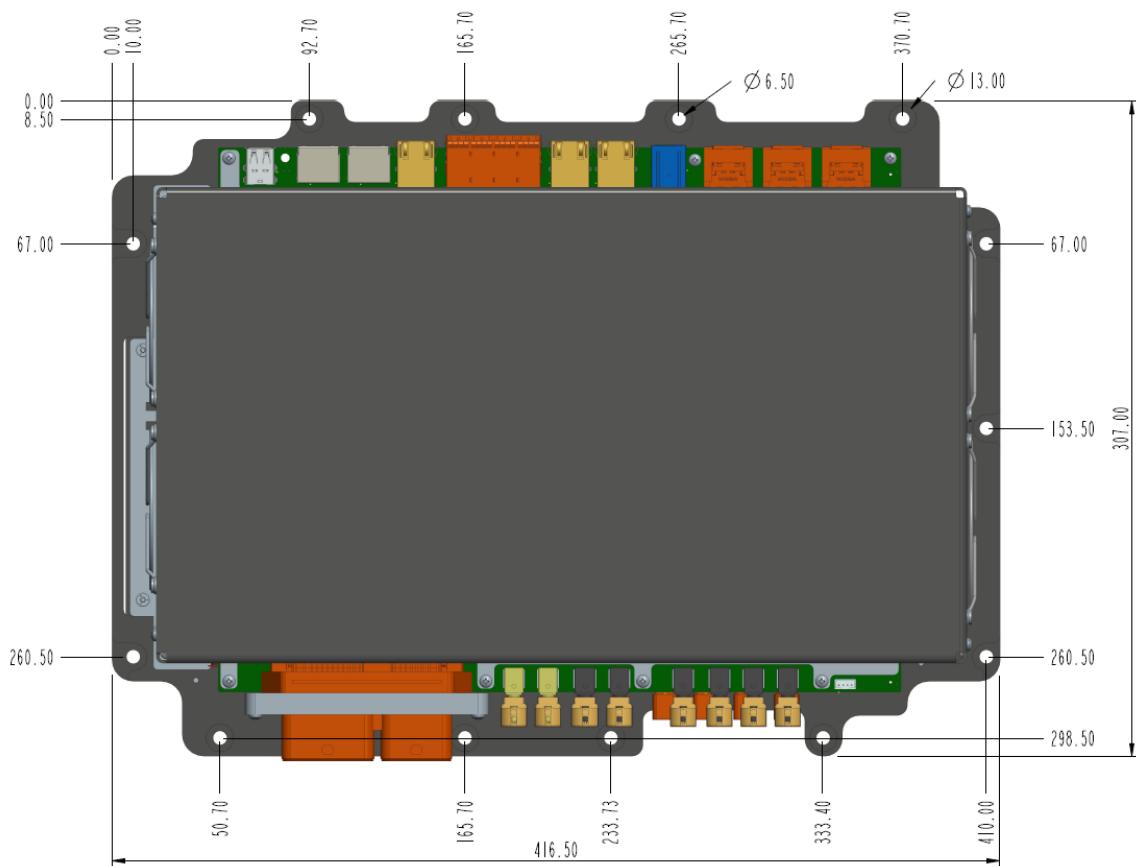


Figure 1-3. Baseplate Mechanical Dimensions and Developer System Top View

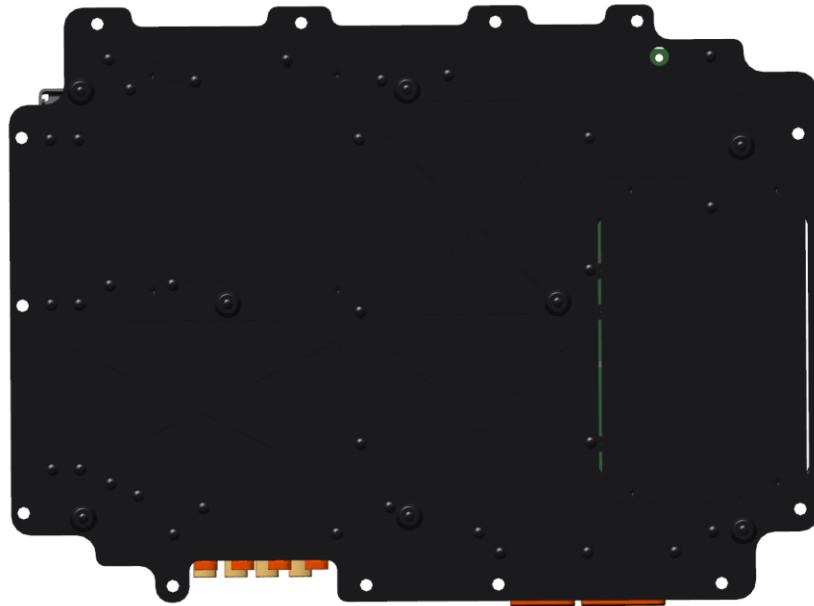


Figure 1-4. Developer System Bottom View

## 1.3 FRONT AND REAR VIEWS WITH INTERFACE CONNECTOR LOCATIONS

Figure 1-5 and Figure 1-6 illustrate the developer system connector locations.

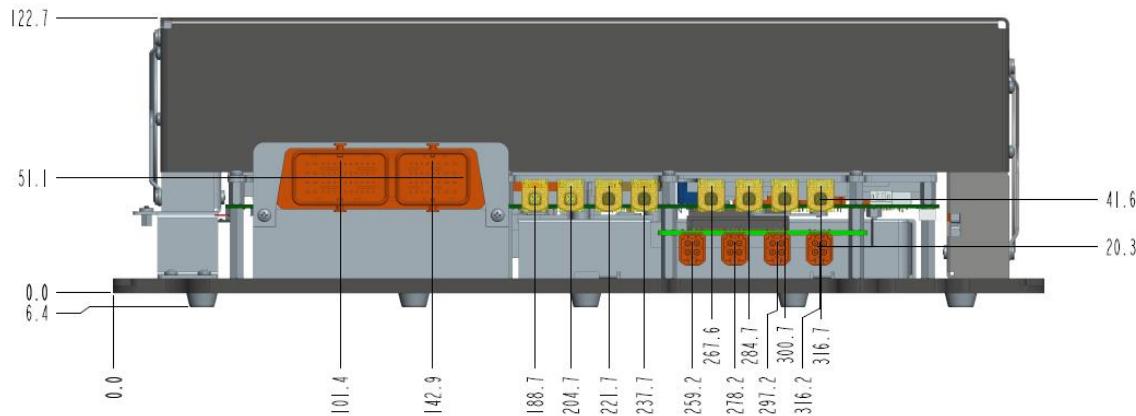


Figure 1-5. Developer System Front View with Interface Connector Locations

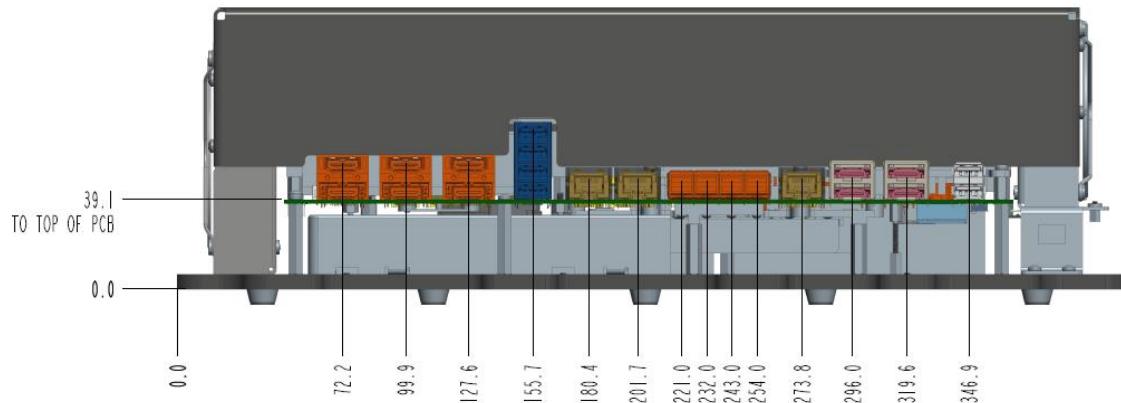


Figure 1-6. Developer System Rear View with Interface Connector Locations

## 1.4 SIDE VIEWS WITH INTERFACE CONNECTOR PROFILES

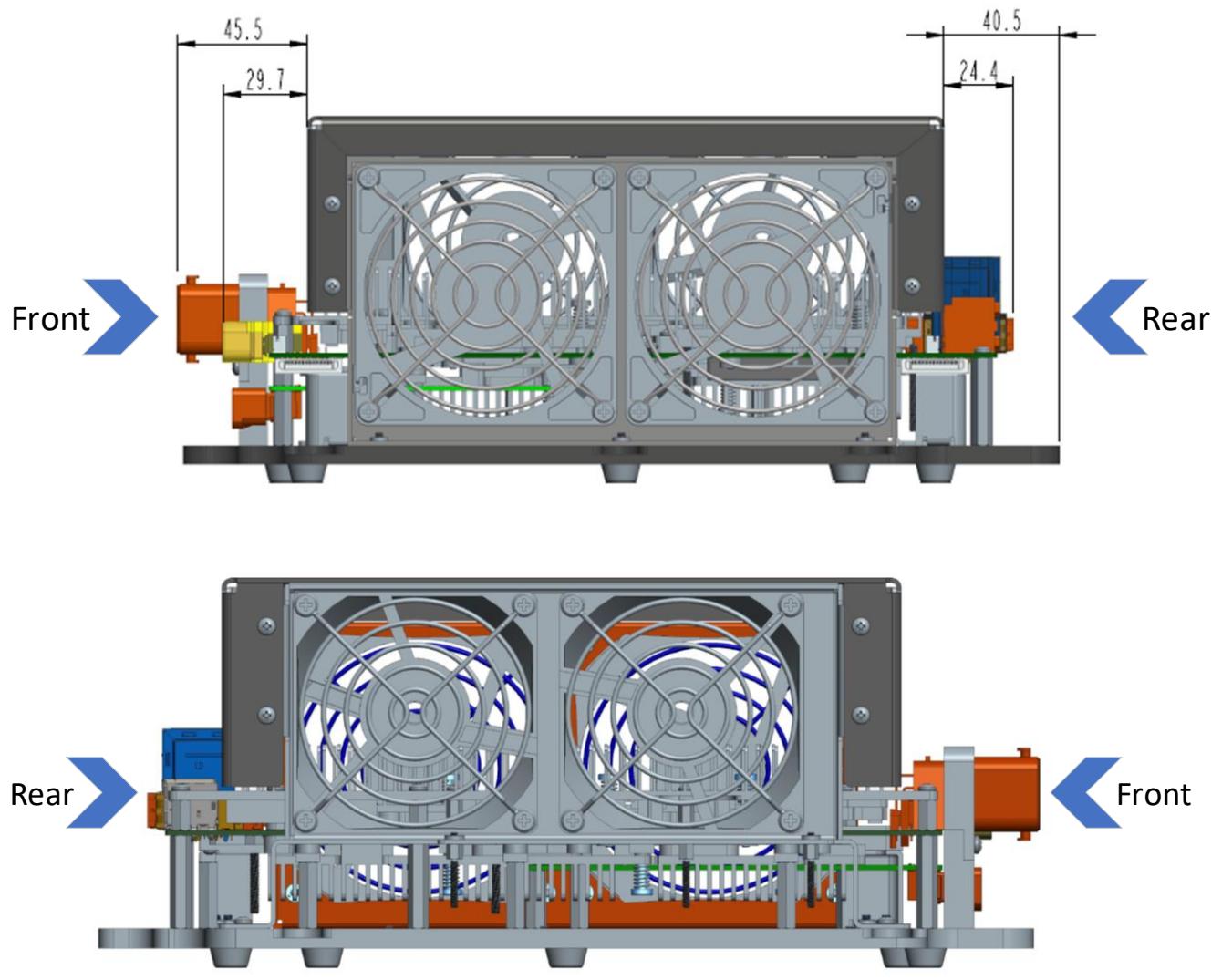


Figure 1-7. Developer System Side Views

# Chapter 2. MOUNTING CONSIDERATIONS

The developer system assembly is shown in Figure 2-1. When mounting the assembly, make sure there are no obstructions on all sides since it includes a cooling solution with fans on both the right and the left sides. There must be enough clearance around the fan openings for the cooling solution. The airflow rate required for the developer system is 80 cfm. With proper clearance, the developer system fans are capable of delivering greater than 80 cfm at max RPM. See Figure 2-2 for the airflow direction and Table 2-1 for the recommended clearance for all four sides.

The front and rear panels also need clearance for plugging and unplugging the cables as well as accommodating for cable bend radius.



**Note:**

The developer system must be mounted horizontally with the baseplate facing downwards. **DO NOT** mount in any other orientation.

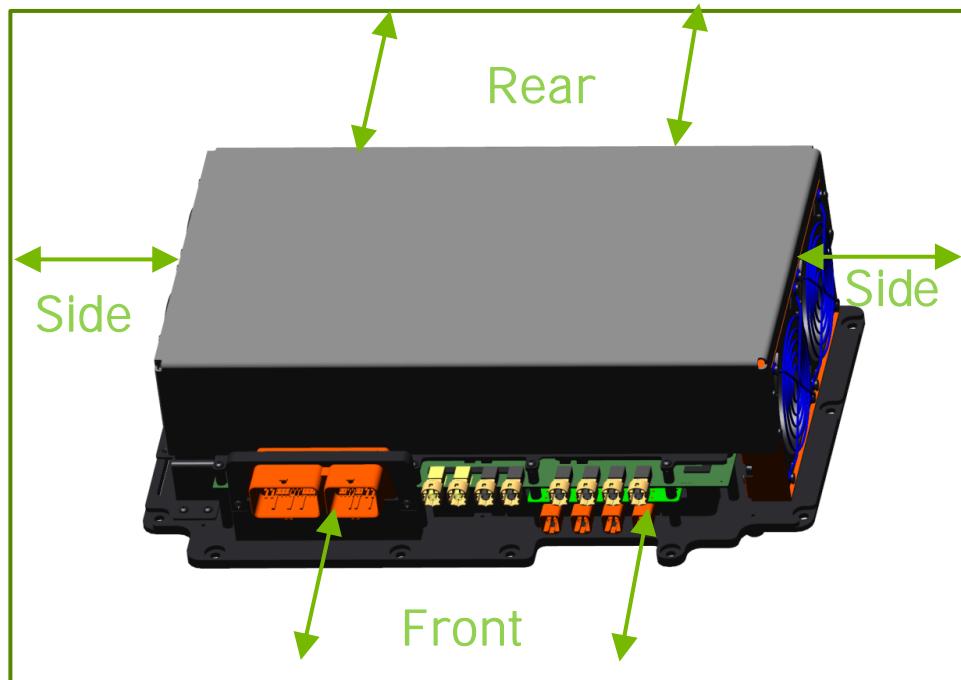


Figure 2-1. Keep-out Clearance Around All Sides



Figure 2-2. Airflow Direction

Table 2-1. Clearance Recommendation

Panel	Clearance (mm)
Front	120
Rear	100
Side	100

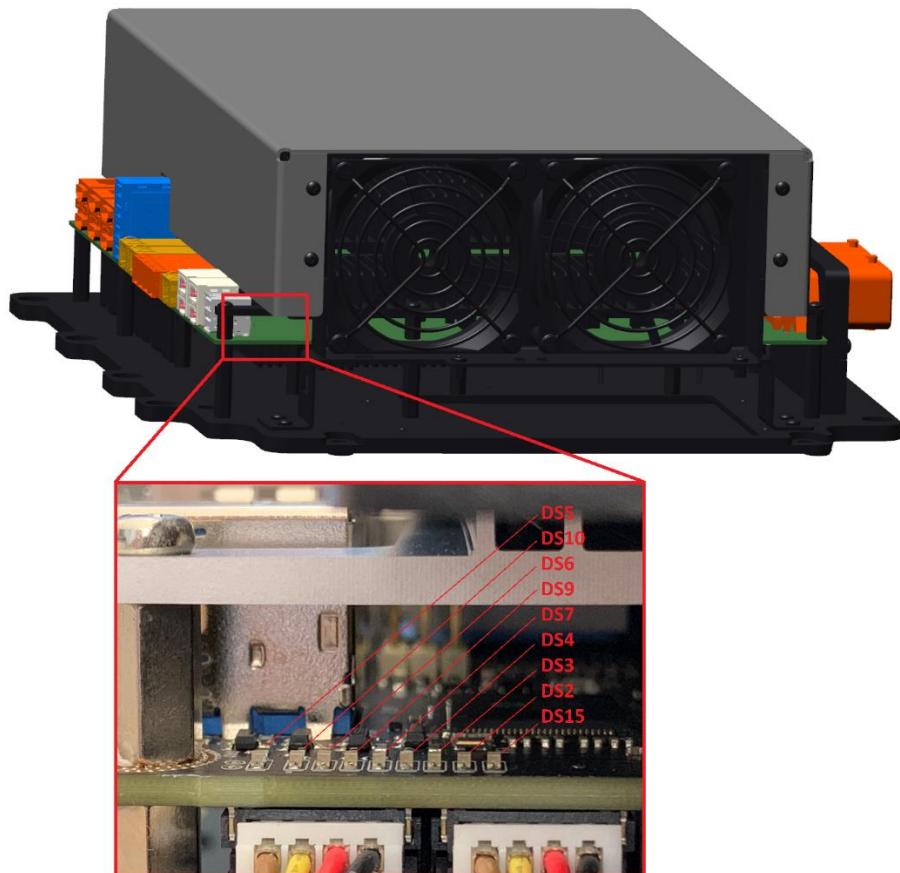
The dimensions and the weight of developer system are shown in Table 2-2.

The weight depends on the SKU number because the developer system may be shipped with or without the two SXM2 form factor dGPU modules.

**Table 2-2. Dimensions and Weight**

<b>Dimensions (mm)</b>	
Length	307.00
Width	416.50
Height (without rubber feet)	122.70
<b>Weight (Kg)</b>	
With dGPU modules	7.98 ± 3%
Without dGPU modules	5.99 ± 3%

The other consideration when mounting the developer system is to avoid blocking the view to the LED indication. There are 9 LEDs that can be seen from the corner as indicated in Figure 2-3 below. The functions of these LEDs are listed in Table 2-3.



**Figure 2-3. LED Locations**

**Table 2-3. LED Status Description**

LED	Color	Description
DS5	Green	Controlled by Xavier A code
DS10	Green	Turns ON when XA_5V/XA_VDD_SOC are both powered
DS6	Green	Turns ON when AURIX_3V3/AURIX_1V3 are both powered
DS9	Green	Turns ON when SYS_5V is powered
DS7	Green	Turns ON when KL30_POWER/AURIX_5V are both powered
DS4	Green	Turns ON when AURIX_3V3 is powered
DS3	Green	Turns ON when VBAT_SYS is powered
DS2	Green	Controlled by Aurix MCU code
DS15	Green	Controlled by Aurix MCU code

# Chapter 3. INTERFACE CONNECTIONS

The developer system has connectors on both the front and the rear panels.

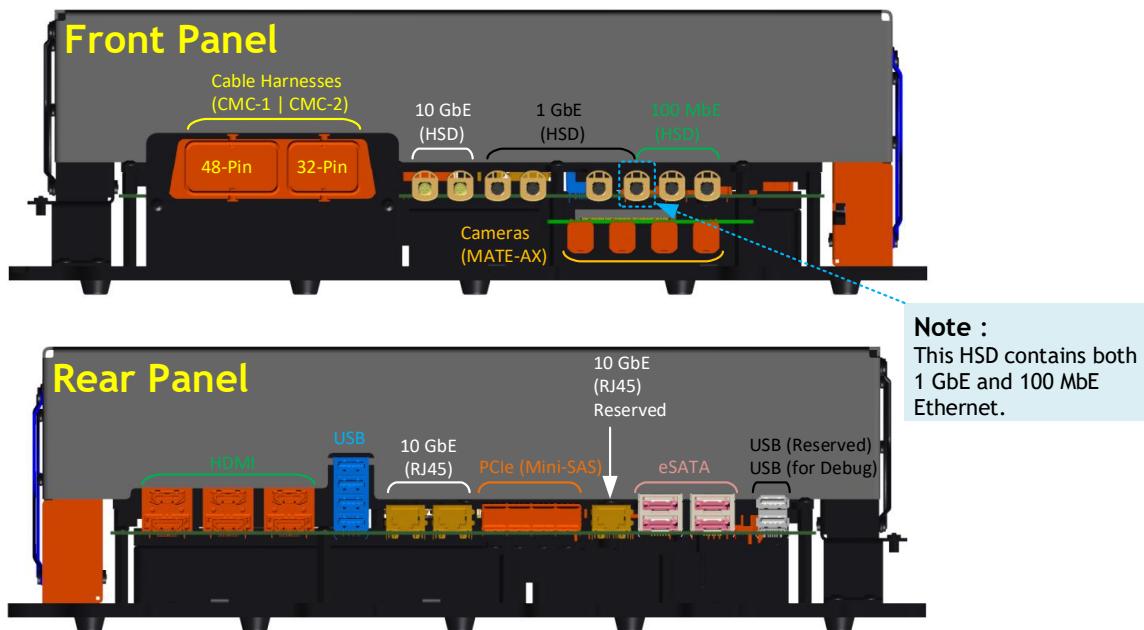


Figure 3-1. Front Panel and Rear Panel Connectors

The connectors on the rear panel are all industry standard connectors for development and debug purpose. The connectors on the front panel are connected to the vehicle. The connector and cable part numbers, along with the maximum tested cable lengths, are listed in Table 3-1.

Table 3-1. Interface Connectors and Cables

Connector	Manufacturer and Part Number	Location	Cable or Cable Assembly	Maximum Cable Length (Tested)
Cable Harness Connector	Molex CMC 502225-0801	Front	Cable Harness	See Figure 3-3
10 GbE Connector	Rosenberger HSD D4S20L-40MA5-B (White)	Front	LEONI Dacar® 636	15 meters
1 GbE Connector	Rosenberger HSD D4S20L-40MA5-A (Black)	Front	LEONI Dacar® 636	15 meters
100 MbE Connector	Rosenberger HSD D4S20L-40MA5-E (Green)	Front	LEONI Dacar® 636	15 meters
Quad Camera Connector	TE Connectivity MATE-AX 0-2304168-9	Front	LEONI Dacar® 302 (via the FAKRA Jacks on the Quad Camera Breakout Cable, as in Figure 3-6)	10 meters <sup>1</sup> (GMSL) 8 meters <sup>2</sup> (GMSL2)
PCIe Connector (Mini-SAS)	TE Connectivity Mini-SAS HD 1x4 2149375-1	Rear	Amphenol 10117949-3010HLF	1 meter
USB Connector	Lotes AUSB0290 (Quad) Wieson G3509CE04-006-H (Dual)	Rear	Standard USB Cable	1 meter
Notes:				
<ol style="list-style-type: none"> <li>The 10 meter cable length applies to GMSL at 1.5Gbps.</li> <li>The 8 meter cable length applies to GMSL2 at 6Gbps.</li> </ol>				

## 3.1 VEHICLE CABLE HARNESS

The developer system uses Molex **CMC** connector for cable harness connections. As in Figure 3-3, each cable harness includes a mating connector to the **CMC** connector showing in Figure 3-2. The **CMC** connector includes a primary 48-pin connector (**CMC-1**) and a secondary 32-pin connector (**CMC-2**). The other end of the cable harness is wired to connectors labeled with different interfaces for connecting the developer system signals

to the other electronic modules in the vehicle. Please refer to section 3.1.3 for the pinouts of these interface connectors.

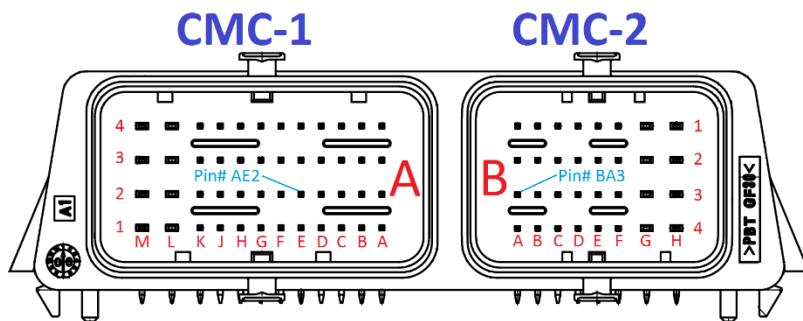


Figure 3-2. CMC-1 and CMC-2 Cable Harness Connector Pinout

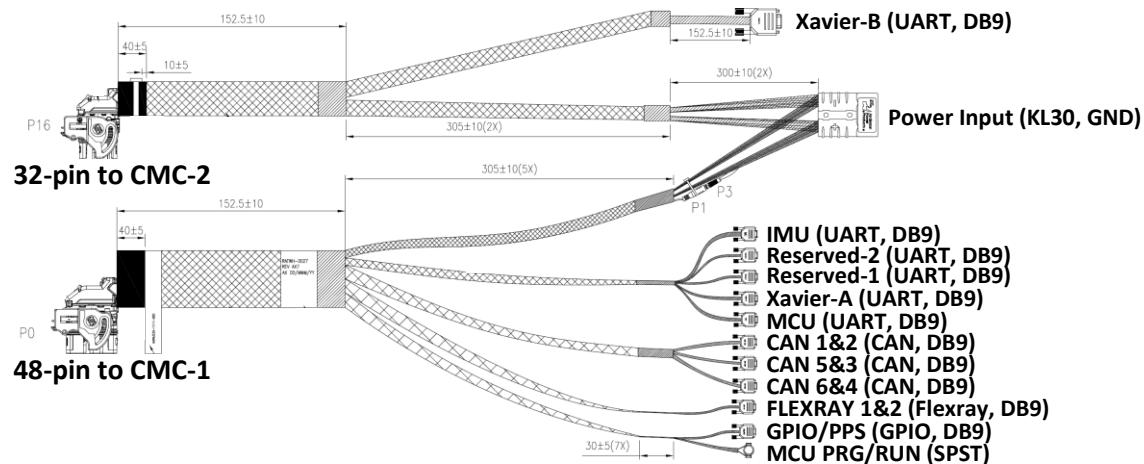


Figure 3-3. 48-pin and 32-pin Cable Harnesses

### 3.1.1 Vehicle 48-pin Cable Harness Connector CMC-1

The 48-pin cable harness includes the connections to the following interfaces:

- ▶ 6x CAN Ports (three DB9 female connectors)
- ▶ 2x FlexRay (a single DB9 female connector)
- ▶ 4x GPIO (a single DB9 female connector)
- ▶ 5x UART (five DB9 female connectors)
- ▶ Hardware Configuration / MCU Debug (SPST switch for Program/Run)
- ▶ KL15\_POWER (Banana Plug)
- ▶ KL30\_VBAT Vehicle Power/Ground (Anderson SB50 connector)

Table 3-2 shows the 48-pin cable harness connections.

**Table 3-2. Interfaces on the 48-pin Cable Harness Connector CMC-1**

CMC-1 Pin #	Wire Group	Signal Name	Connector (Label)	Connector Pin #	Signal Description
AL1	Power	KL30_VBAT		Pin noted “+”	KL30_VBAT (Vehicle Main Battery)
AL2	Power				
AM1	Power				
AM2	Power				
AM3	Power				
AL3	GND	Anderson SB50		Pin noted “-”	Ground
AL4	GND				
AM4	GND				
AK1	GND				
AJ1	GND				
AF3	GND				
AF4	GND				
AA1	GND				
AA3	GND	GND	DB9 and SPST Switch (shared GND)	N/A	Ground
AC4	GND				
AD2	GND				
AF2	Power	KL15_POWER	Banana Plug	N/A	KL15_POWER
AC3	FR	FR1_BP	DB9 (FLEXRAY 1&2)	7	FlexRay 1 Bus Plus (MCU)
AB3	FR	FR1_BM		2	FlexRay 1 Bus Minus (MCU)
AE3	FR	FR2_BP		8	FlexRay 2 Bus Plus (MCU)
AD3	FR	FR2_BM		1	FlexRay 2 Bus Minus (MCU)
AH4	CAN	CAN1_H	DB9 (CAN 1&2)	7	CAN 1 High (MCU)
AG4	CAN	CAN1_L		2	CAN 1 Low (MCU)
AJ4	CAN	CAN2_H		8	CAN 2 High (MCU/XA-CAN0/XB-CAN0/CVM)
AK4	CAN	CAN2_L		1	CAN 2 Low (MCU/XA-CAN0/XB-CAN0/CVM)
AK3	CAN	CAN5_H	DB9 (CAN 5&3)	7	CAN 5 High (MCU)
AJ3	CAN	CAN5_L		2	CAN 5 Low (MCU)
AB4	CAN	CAN3_H		8	CAN 3 High (MCU)
AA4	CAN	CAN3_L		1	CAN 3 Low (MCU)
AH3	CAN	CAN6_H	DB9	7	CAN 6 High (MCU/XA-CAN1/XB-CAN1/CVM)

CMC-1 Pin #	Wire Group	Signal Name	Connector (Label)	Connector Pin #	Signal Description
AG3	CAN	CAN6_L	(CAN 6&4)	2	CAN 6 Low (MCU/XA-CAN1 / XB-CAN1/CVM)
AE4	CAN	CAN4_H		8	CAN 4 High (MCU)
AD4	CAN	CAN4_L		1	CAN 4 Low (MCU)
AA2	GPIO	GPIO1/PPS	DB9 (GPIO/PPS)	3	GPIO1/PPS
AB2	GPIO	GPIO2		8	GPIO2
AC2	GPIO	GPIO3		7	GPIO3
AB1	GPIO	GPIO4		6	GPIO4
AH1	UART	UART1_RX	DB9 (IMU)	3	UART 1 Receive
AG1	UART	UART1_TX		2	UART 1 Transmit
AF1	UART	UART2_RX	DB9 (Reserved-2)	3	UART 2 Receive
AE1	UART	UART2_TX		2	UART 2 Transmit
AD1	UART	UART3_RX	DB9 (Reserved-1)	3	UART 3 Receive
AC1	UART	UART3_TX		2	UART 3 Transmit
AG2	UART	UART4_RX	DB9 (Xavier-A)	3	UART 4 Receive
AE2	UART	UART4_TX		2	UART 4 Transmit
AJ2	UART	UART5_RX	DB9 (MCU)	3	UART 5 Receive
AH2	UART	UART5_TX		2	UART 5 Transmit
AK2	HW Config	HWCFG3	SPST (PRG / RUN)	N/A	Hardware Configuration

### 3.1.2 Vehicle 32-pin Cable Harness Connector CMC-2

The 32-pin cable harness includes the following connections to different interfaces. The data signals are connected to a single DB9 female connector.

- ▶ 1x UART (DB9 female connector)
- ▶ KL30\_VBAT Vehicle Power/Ground (SBS50 connector)

Table 3-3 shows the developer system 32-pin cable harness connections.

**Table 3-3. Interfaces on the 32-pin Cable Harness Connector CMC-2**

CMC-2 Pin #	Wire Group	Signal Name	Connector (Label)	Connector Pin #	Signal Description	
BG4	Power	KL30_VBAT	Anderson SBS50	Pin noted “+”	KL30_VBAT (Vehicle Main Battery)	
BG3	Power					
BG2	Power			Pin noted “-”		
BG1	Power					
BH1	GND	GND		Ground	Reserved	
BH2	GND					
BH3	GND					
BH4	GND					
BA2					Reserved	
BA1						
BB2						
BB1						
BC2						
BC1						
BD2						
BD1						
BE2						
BE1						
BF2						
BF1						
BF3						
BE3						
BB4						
BA4						
BA3						
BB3						
BF4	UART	UART6_RX	DB9 (Xavier-B)	3	UART 6 Receive	
BE4	UART	UART6_TX		2	UART 6 Transmit	
BD3	GND	GND		5	GND	
BC3	GND	GND	N/A	N/A		
BD4	Harness Detection	HRNS_DET*	N/A	N/A	Harness Detection (connect to BC3 via 32-pin cable harness)	
BC4	RSVD	RSVD	N/A	N/A	Reserved	

### 3.1.3 Pinout of Connections to Vehicle

The developer system cable harness breaks out signals to individual connectors. This section details the pinout information for each connector type.

On the 48-pin cable harness, the DB9 female connector, commonly used for RS-232 serial connection in the PC industry, is used for CAN, FlexRay, UART and GPIO. On the 32-pin cable harness, the DB9 female connector is used for UART signals. Figure 3-4 shows the pinout of the DB9 connector.

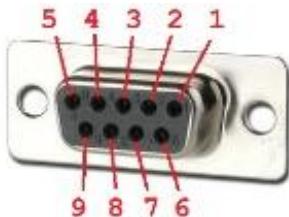


Figure 3-4. Cable Harness DB9 Connector Pinouts

#### 3.1.3.1 CAN Connectors

Table 3-4 shows the pinout for each DB9 connector used for two CAN buses. The developer system cable harness includes three DB9 connectors for a total of six CAN buses, which are numbered from **1** to **6**. Each CAN DB9 connector is labeled to identify the CAN bus numbers it is connected to. The CAN buses are paired in **x** and **y** in each DB9 connector with label of “CAN **x&y**”, where the (**x, y**) are the CAN bus numbers and paired in **(1, 2)**, **(5, 3)** and **(6, 4)**. Table 3-5 shows a more detailed CAN bus mapping to the MCU and the Xavier SoCs.



#### CAUTION:

On the cable harness, pin-9 of the CAN connector is connected to the VBAT. When connecting two developer systems together via the CAN connectors, this pin-9 **should not be connected**. When building CAN cable using 10-wire ribbon cable and DB9 connectors, **please cut pin 9 and pin 10** to avoid shorting the VBAT of the two systems together.

Table 3-4. CAN Connector Pinout

Pin Number (DB9)	Signal of the CAN Bus	Description
7	CAN_x_H	CAN high signal of Bus/Port x
2	CAN_x_L	CAN low signal of Bus/Port x
8	CAN_y_H	CAN high signal of Bus/Port y
1	CAN_y_L	CAN low signal of Bus/Port y
3 and 6	GND	GND
9	VBAT (connected to KL30_VBAT)	Power

Note:

- This DB9 connector contains two CAN buses with pin-9 connected to VBAT. Its pinout is not the standard CAN pinout, which has CAN signals at pin-7 and pin-2 for a single CAN bus.
- The CAN cable adapter, CANcable2Y, from Vector Informatik GmbH can be used for splitting the two CAN buses into two separate DB9 connectors with the standard pinout.

Table 3-5. CAN Bus/Port Mapping to MCU and Xavier SoCs

CAN Bus # on Cable Harness	DB9 Label	DB9 Pin # (High/Low)	SoC	CAN Port # on SoC	Wake System from Deep Sleep
CAN 1	CAN 1&2	Pin-7/Pin-2	MCU	A	Yes
CAN 2	CAN 1&2	Pin-8/Pin-1	MCU	B	Yes
			Xavier A	CAN0	No
			Xavier B	CAN0	No
			CVM	-	No
			MCU	F	No
CAN 3	CAN 5&3	Pin-8/Pin-1	MCU	C	No
CAN 4	CAN 6&4	Pin-8/Pin-1	MCU	D	No
CAN 5	CAN 5&3	Pin-7/Pin-2	MCU	E	No
CAN 6	CAN 6&4	Pin-7/Pin-2	Xavier A	CAN1	No
			Xavier B	CAN1	No
			CVM	-	No

### 3.1.3.2 FlexRay Connector

Table 3-6 shows the pinout for each DB9 connector used for the two MCU FlexRay ports. The connector is labeled with “**FLEXRAY 1&2**”.

Table 3-6. FlexRay Connector Pinout

Pin Number (DB9)	Signal
7	FR_1_BP
2	FR_1_BM
8	FR_2_BP
1	FR_2_BM
3 and 5	GND

### 3.1.3.3 GPIO Connector

Table 3-7 shows the pinout for each DB9 connectors used for GPIO ports. The connector is labeled with “**GPIO/PPS**”.

Table 3-7. GPIO Connector Pinout for the 48-pin Cable Harness

Pin Number (DB9)	Signal	Function	Connection
3	GPIO1/PPS	Input Only	Xavier A, Xavier B, CVM, MCU
8	GPIO2	Input Only	MCU
7	GPIO3	Input / Output	MCU
6	GPIO4	Input / Output	Xavier A
5	GND	Ground	Ground

Table 3-8. GPIO Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{IH}$	HIGH Level Input Voltage	2	-	$V_{BAT\_SYS}$	V
$V_{IL}$	LOW Level Input Voltage	0	-	0.7	V
$I_o$	Output Current	0	-	300	mA
$V_{OH}$	HIGH Level Output Voltage	-	$V_{BAT\_SYS}$	-	V
$V_{OL}$	LOW Level Output Voltage	-	0	-	V

### 3.1.3.4 UART Connectors

Table 3-9 shows the pinout for each DB9 connector used for UART port.

Table 3-9. UART Connector Pinout

Pin Number (DB9)	Signal
3	UART Rx
2	UART Tx
5	GND

As shown in Table 3-10 there are 6 UART connectors on the cable harness labeled with: “MCU”, “Xavier-A”, “Reserved-1”, “Reserved-2”, “IMU” (Inertial Measurement Unit) and “Xavier-B”.

Table 3-10. UART Connectors on Cable Harness

Developer System UART #	Label on DB9 Connector	Function	UART Connection
UART 1	IMU	External Peripheral (ex. IMU, GPS, GNSS)	Xavier A (UART2 of Xavier A)
UART 2	Reserved-2	Reserved	SoC on CVM
UART 3	Reserved-1	Reserved	SoC on CVM
UART 4	Xavier-A	Debug*	Xavier A (UART3 of Xavier A)
UART 5	MCU	Debug*	MCU
UART 6	Xavier-B	Debug*	Xavier B (UART3 of Xavier B)

**Note:**  
The UART ports of the DB9 connectors used for debugging can also be controlled using the on-board USB Hub device via the FTDI4232 USB-to-UART chips. Please see Table 3-19 for more information.

### 3.1.3.5 KL30\_VBAT Connector

Table 3-11 shows the pinout for the Anderson SB50 and SBS50 connectors used for KL30\_VBAT power, which should be connected to the main battery of the vehicle.

Table 3-11. KL30\_VBAT Connector Pinout

Pin Number	Signal
Pin noted “+”	KL30_VBAT
Pin noted “-”	GND

### 3.1.3.6 KL15 Connector

A banana plug is used for the KL15 functionality.

For lab use, the KL15 gets 12V power from the banana jack by connecting the plug and the jack together. On the developer system cable harness, if the source of KL15 is not coming from the cable harness KL30\_VBAT power input, NVIDIA recommends adding a **125mA fuse** between the banana jack/plug (see P1/P3 in Figure 3-3).

In the vehicle, the **KL15 source may be connected to the power-on switch for wake-up functionality**. Note that the wake-up feature needs software support before it is functional. Please refer to the latest NVIDIA documents: *DRIVE Software Release Notes* and *DRIVE OS with DriveWorks Release Notes* for more details.

## 3.2 FRONT PANEL CONNECTORS

Other than the connectors provided through the cable harnesses, the connectors on the front panel of the developer system are for either Ethernet or cameras. The NVIDIA DRIVE™ AGX Developer Kit ships with the following components for these interface connections:

- ▶ Dual GbE Dongles (E3579)
- ▶ HSD Cables
- ▶ Quad Camera Breakout Cables
- ▶ Sekonix AR0231 GMSL Cameras
- ▶ FAKRA Coax Cables

### 3.2.1 HSD Connectors for Ethernet

Figure 3-5 shows the Rosenberger HSD connectors for 10 GbE, 1 GbE and 100 MbE Ethernet, as well as the E3579 dongle, for converting 1 GbE and 100 MbE HSD to the standard RJ45 connectors. The E3579 dongle supports both 1000BASE-T1 and 100BASE-T1. Depending on which HSD connector the dongle is connected to, the RJ45 may carry 1000BASE-T1 or 100BASE-T1.

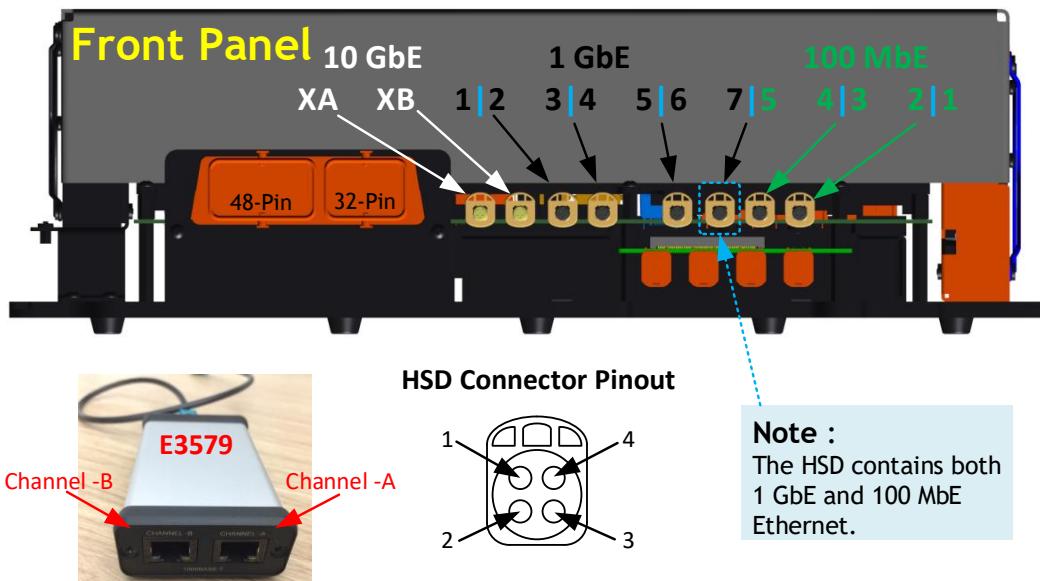


Figure 3-5. Ethernet Connectors

Table 3-12 shows the Ethernet connection mapping when connecting the E3579 dongles to the developer system using HSD cables. Each of the HSD connectors requires a dongle to convert the HSD to two RJ45 Ethernet channels. These Ethernet ports are networked together with the Ethernet switches on the mainboard and can be accessed by either of the NVIDIA® Xavier™ devices- Xavier A, Xavier B, or the SoC on CVM.

**Table 3-12. Dual GbE Dongle Ethernet Connection Mapping**

Silkscreen	HSD Color	HSD Pin #	Polarity	Ethernet Standard	Max Speed Supported	E3579 Channel #
2   1	Green	2	P	100BASE-T1	100 Mbps	Channel -A
		4	N			
		3	P	100BASE-T1	100 Mbps	Channel -B
		1	N			
4   3	Green	2	P	100BASE-T1	100 Mbps	Channel -A
		4	N			
		3	P	100BASE-T1	100 Mbps	Channel -B
		1	N			
7   5	Black	2	P	100BASE-T1	100 Mbps	Channel -A
		4	N			
		3	P	1000BASE-T1	1 Gbps	Channel -B
		1	N			
5   6	Black	2	P	1000BASE-T1	1 Gbps	Channel -A
		4	N			
		3	P	1000BASE-T1	1 Gbps	Channel -B
		1	N			
3   4	Black	2	P	1000BASE-T1	1 Gbps	Channel -A
		4	N			
		3	P	1000BASE-T1	1 Gbps	Channel -B
		1	N			
1   2	Black	2	P	1000BASE-T1	1 Gbps	Channel -A
		4	N			
		3	P	1000BASE-T1	1 Gbps	Channel -B
		1	N			

Each 10 GbE port is implemented with individual 10 GbE controller containing four differential pairs. These pairs are converted to single-ended by the transformers on the mainboard before connecting to the HSD connectors. Therefore, each of the 10 GbE HSD connector pins carries a single-ended signal. Multiple developer systems can be networked together with HSD cables. The pair mapping of the 10 GbE HSD are shown in Table 3-13. These 10 GbE ports are accessed by Xavier via its PCIe interface.

Table 3-13. Pair Mapping of 10 GbE Ethernet Connectors

Silkscreen	HSD Pin #	Controller Pair #	Ethernet Standard	Connected to NVIDIA SoC
XA	1	Single-ended of Pair A	10GBASE-T	Xavier A
	2	Single-ended of Pair D		
	3	Single-ended of Pair C		
	4	Single-ended of Pair B		
XB	1	Single-ended of Pair A	10GBASE-T	Xavier B
	2	Single-ended of Pair D		
	3	Single-ended of Pair C		
	4	Single-ended of Pair B		

### 3.2.2 FAKRA Connectors for Camera Inputs

With the Quad Camera Breakout Cables each of the four MATE-AX connectors can be connected to four cameras using the FAKRA Coax cables. So, a total of 16 cameras can be supported. The Sekonix AR0231 GMSL Cameras are POC (power-over-coax) cameras with their power coming from FAKRA Coax cables. With the GMSL2 Deserializer/Aggregator, both Xavier A and Xavier B can access these 16 cameras.

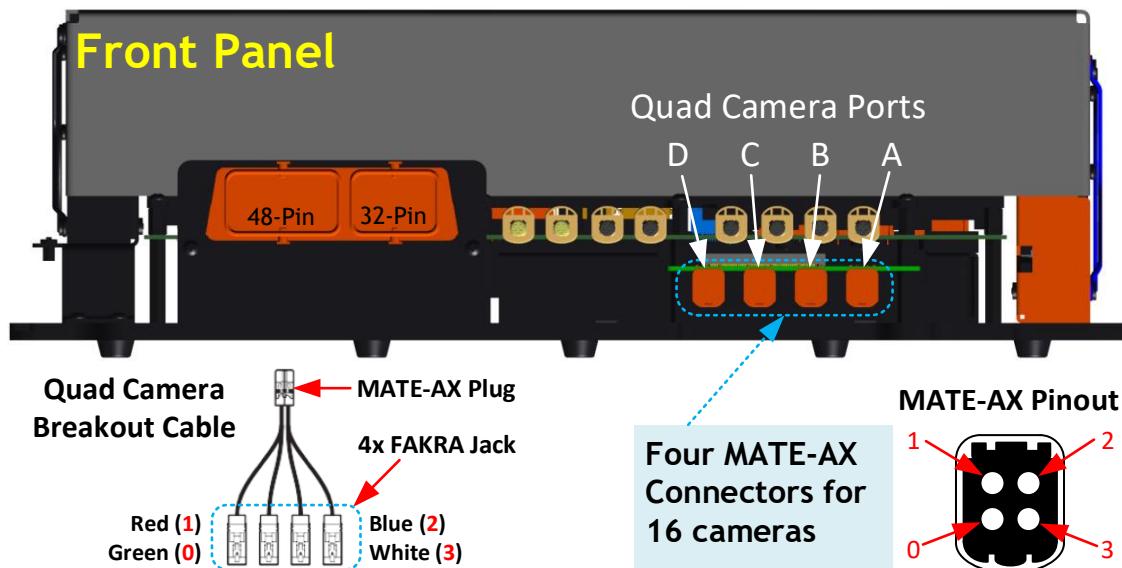


Figure 3-6. Camera Connectors

### 3.3 REAR PANEL CONNECTORS

The connectors on the rear panel are industry standard connectors for development purpose. Please refer to the specifications of these standards for their pinout. The mapping of these industrial standard connectors is described in the following sections.

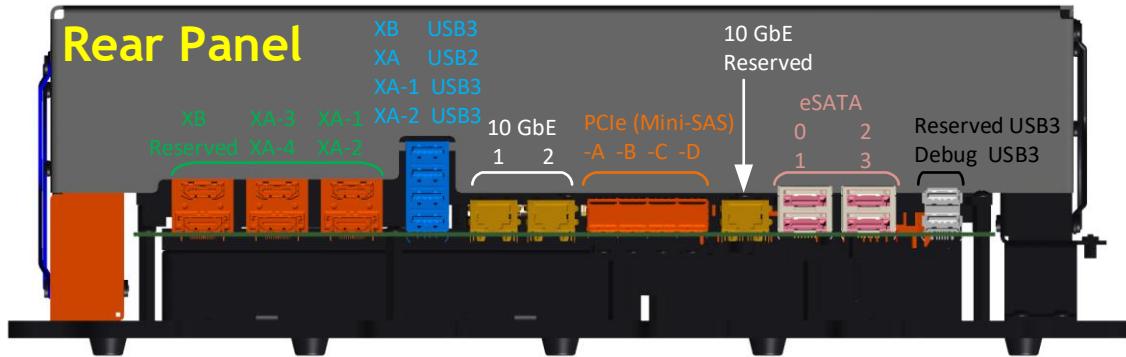


Figure 3-7. Rear Panel Connectors

#### 3.3.1 HDMI Connectors

There are six connectors on the rear panel for HDMI output during the drive application development process.

When using an HDMI monitor, please follow the required power sequencing below:

- Power on the NVIDIA DRIVE AGX System first, then power on the HDMI monitor
- Power off the HDMI monitor first, then power off the NVIDIA DRIVE AGX System

Table 3-14. HDMI Connector Mapping to the NVIDIA SoC

Silkscreen	Location	Connected to NVIDIA SoC
XA-1	Top-right	Xavier A
XA-2	Bottom-right	
XA-3	Top-middle	
XA-4	Bottom-middle	
XB	Top-left	Xavier B
Reserved	Bottom-left	Reserved

### 3.3.2 USB Connectors

There are four USB connectors stacked on the rear panel. These are USB 2.0 or USB 3.1 connectors to either Xavier A or Xavier B. Table 3-15 shows their connections to the Xavier SoC, the supported USB standards and modes.

Table 3-15. USB Connector Mapping to the NVIDIA SoC

Silkscreen	USB Standard	USB Mode Support	Connected to NVIDIA SoC
XB USB3	USB 3.1	Host Mode Only	Xavier B
XA USB2	USB 2.0	Host Mode Only	Xavier A
XA-1 USB3	USB 3.1	Host Mode Only	
XA-2 USB3	USB 3.1	Host/Device	

### 3.3.3 10 GbE RJ45 Connectors

The 10 GbE RJ45 connectors on the rear panel are for development purpose. They are connected to different 10 GbE controllers. The 10 GbE controllers have PCIe interface connected to a PCIe switch for accessing by Xavier A and/or Xavier B.

Table 3-16. 10GbE RJ45 Connector Mapping to the NVIDIA SoC

Silkscreen	Connected to NVIDIA SoC
10 GbE 1	Xavier A, Xavier B
10 GbE 2	
10 GbE Reserved	Reserved

### 3.3.4 PCIe (Mini-SAS) Connector

The Mini-SAS connector on the rear panel includes 4 ports. These ports are connected to the PCIe switch via PCIe repeaters. Each port has 4 PCIe lanes, which follow the pinout defined in the *PCI Express External Cabling Specification* published by PCISIG. With Mini-SAS cables (SFF-8644 cable assembly), this connector provides external PCIe access for the Xavier SoCs and the SoC on CVM.

Table 3-17. Mini-SAS Connector Mapping to the NVIDIA SoC

Silkscreen	Connected to NVIDIA SoC
PCIe A	Xavier A, Xavier B, SoC on CVM
PCIe B	
PCIe C	
PCIe D	

### 3.3.5 eSATA Connectors

The eSATA connectors on the rear panel can be used to connect to eSATA drives for storing data during the development.

Note that since these are eSATA connectors, not eSATAp connectors, the eSATA drives will have to be powered externally.

Table 3-18. eSATA Connector Mapping to the NVIDIA SoC

Silkscreen	Location	Connected to NVIDIA SoC
eSATA 0	Top-left	Xavier A, Xavier B, SoC on CVM
eSATA 1	Bottom-left	
eSATA 2	Top-right	
eSATA 3	Bottom-right	

### 3.3.6 Debug USB Connector

The bottom USB connector of the dual USB connector on the right is used for debugging. This debug USB port is connected to a 7-port USB Hub chip. Three of the seven USB ports are connected to the NVIDIA SoCs for flashing the software. The other four USB ports are connected to FTDI4232 chips for implementing debug consoles and JTAG ports.

Table 3-19. Debug USB Connector Mapping

Silkscreen	Port# of USB Hub	FTDI4232	Port# of FTDI4232	Connected to NVIDIA SoC
USB Debug	1	n/a	n/a	Xavier A (for flashing SW)
	2	n/a	n/a	Xavier B (for flashing SW)
	3	n/a	n/a	SoC on CVM (for flashing SW)
	4	Chip #1	A	Reserved
			B	Xavier A JTAG
			C	Xavier A Debug Console (UART)
			D	Aurix Debug Console (UART)
	5	Chip #2	A	Reserved
			B	Xavier B JTAG
			C	Xavier B Debug Console (UART)
			D	Reserved
	6	Chip #3	A	Reserved
			B	SoC on CVM JTAG
			C	SoC on CVM (UART#1 on CVM)
			D	SoC on CVM (UART#2 on CVM)
	7	Chip #4	A	Reserved
			B	Reserved
			C	Reserved
			D	PCIe switch UART

# Chapter 4. ENVIRONMENTAL REQUIREMENTS

When installing the developer system in a vehicle, NVIDIA requires the following:  
Mount the system horizontally with the baseplate facing downwards and providing the necessary keep-out as shown in Figure 2-1.

- ▶ Use M6 screws through the 13 mounting holes of the baseplate to secure to the vehicle. If needed, the rubber feet on the bottom of the baseplate can be removed prior to installing in the vehicle as they are for desktop use only.
- ▶ Ensure a dust free environment; *do not mount on carpet*.
- ▶ Ensure a good GND connection to the chassis of the car.
- ▶ Ensure sufficient air flow; refer to Chapter 2 for mounting considerations.

## 4.1 OPERATING ENVIRONMENT REQUIREMENTS

The system should be operating under the temperature constraints described in Table 4-1.

Table 4-1. Ambient Temperature

Temperature	Module Configuration
0°C to 45°C	Without any SXM2 dGPU modules
0°C to 45°C	With Turing SXM2 dGPU modules
0°C to 40°C	With Tesla V100 SXM2 dGPU modules or COM Express module

The system operation should not exceed the shock and the vibration constraints summarized below.

- ▶ Mechanical Shock Constraints:
  - Half Sine Wave at  $500 \text{ m/s}^2$ , 6 ms duration
  - 10 shocks in Z-direction, with system mounted horizontally and the baseplate facing downwards.
- ▶ Mechanical Vibration Constraints:
  - Excitation with wide-band random vibration
  - RMS value of acceleration:  $19.7 \text{ m/s}^2$
  - Frequency range is 10-1000 Hz following ISO16750

The system should operate in the humidity of 5% to 95% RH.

## 4.2 STORAGE ENVIRONMENT REQUIREMENTS

Storage ambient temperature:  $-40^\circ\text{C}$  to  $65^\circ\text{C}$

Storage humidity: 5% to 95% RH

# Chapter 5. ELECTRICAL INSTALLATION

## 5.1 OPERATING VOLTAGE

Table 5-1 lists the operating voltage range at the harness connector.

Table 5-1. Operating Voltage

Power Input	Minimum	Nominal	Maximum
KL30_VBAT	7V	12V	28V

**Notes:**

- 1.The developer system is designed to be powered by a 12V vehicle battery. The 28V specification is meant for momentary voltage spike like load dump. It DOES NOT support a 24V battery.
- 2.Includes DC level and any noise or other transients; ensure the input rail remains within the specified range.
- 3.If the developer system to be installed in vehicle comes with GV100 dGPU or COM Express modules, we recommend the following for the cold crank case:
  - Use an inverter and the power supply included in the NVIDIA DRIVE™ AGX Developer Kit
  - Use a second battery to maintain (12V-5%) or higher voltage.
  - Contact vehicle electronic companies such as CALEX for a solution.

## 5.2 OPERATING CURRENT

The KL30\_VBAT maximum operating peak current, System Electrical Design Power (System EDP), is specified as the peak current consumed by the developer system at 200ms moving average.

System EDP is defined using the developer system with the CIM installed. Additional current sourcing capability is required if the developer system is installed with CVM and/or COM EX.

Different from the system EDP current, the inrush current is a surge current required when the developer system power is switched on. The magnitude and the duration of the inrush current is shown in Table 5-2.

Table 5-2. System EDP and Inrush Current

ID	Configuration		System EDP Current (200ms moving average) @ 12V	Inrush Current (Magnitude / Duration) @ 12V
	Xavier SoC(s)	dGPU module(s)		
1	2	2	95A	130A / 200us
2	2	0	38A	130A / 200us
3	1	0	29A	130A / 200us

Note:

1. CIM is included in all above configurations, but CVM and COMEX are not included.
2. The current consumption of the debug interfaces on the rear panel of the developer system, as shown in Figure 1-6, are not included.
3. The **System EDP Current** and the **Inrush Current** in this table are specified at the nominal KL30\_VBAT voltage of 12V. Please calculate the worst-case current based on the lowest possible KL30\_VBAT voltage using the following equation:

$$\text{Current} @ V_{min} = \text{Current} @ 12V \times \frac{12V}{V_{min}(v)}$$

The vehicle's main power system should be capable of delivering the **System EDP Current** and the **Inrush Current**. These numbers are also used to select an appropriate inline fuse.

## 5.3 INSTALLATION

The power for the developer system is supplied via the Power Input connector of the cable harness as shown in Figure 3-3. The power source can be either the power adapter that comes with the NVIDIA DRIVE™ AGX Developer Kit or the main battery of a vehicle. There are “+” and “–” signs on the Power Input connector to indicate which terminal to connect to -- VBAT (+) and GND (-).

**When installing the developer system into a vehicle, it is important to ensure that the following requirements are met for the electrical installation:**

1. Battery connection:
  - a) Connect KL30\_VBAT of the developer system to the positive terminal of the vehicle’s main battery. This is the VBAT (+) terminal on the Power Input connector.
  - b) Connect GND of the developer system to the negative terminal of the vehicle main battery. This is the GND (-) terminal on the Power Input connector.
  - c) Connect the KL15 banana plug to the power-on switch of the car for wake-up function. Or, optionally the KL15 banana plug can be connected to the banana jack of the harness so that it pulls power from the main battery.
2. **Fuse and Power Protection:**
  - a) See Table 5-2 for the EDP current numbers for selecting the proper fuse value that meets the developer system configuration.
  - b) The fuse, as shown in Figure 5-1, should factor in fluctuations in the battery voltage due to warm crank conditions.



Figure 5-1. Power Protection Diagram



**Note:**

After powering off the NVIDIA DRIVE AGX System, NVIDIA recommends waiting for more than 20 seconds before powering on the system again. This is to allow the residual power to be properly drained.

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