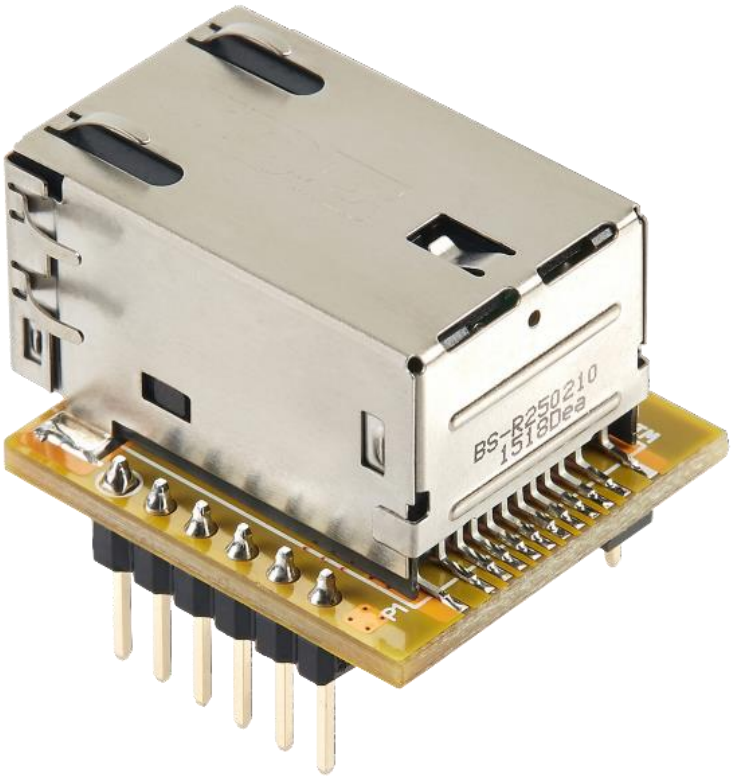
WIZ850io Datasheet

(Version V1.0)



©2016 WIZnet Co., Ltd. All Rights Reserved.

☞ For more information, visit our website at http://www.wiznet.co.kr

Document Revision History

Date	Revision	Changes
2016-04-28	V1.0	Official Release

내용

1. Overview

WIZ850io is a compact size network module that includes a W5500 (TCP/IP hardwired chip and PHY embedded), a transformer and RJ45. It can be used as a component and no effort is required to interface W5500 and Transformer.

The WIZ850io is an ideal option for users who want to develop their Internet enabling systems rapidly. WIZ850io is hardware pin compatible with WIZ820io.

WIZ820io users, to migrate to WIZ850io, need to modify the Firmware.

For the detailed information on implementation of Hardware TCP/IP, refer to the W5500 Datasheet.

1.1. Feature

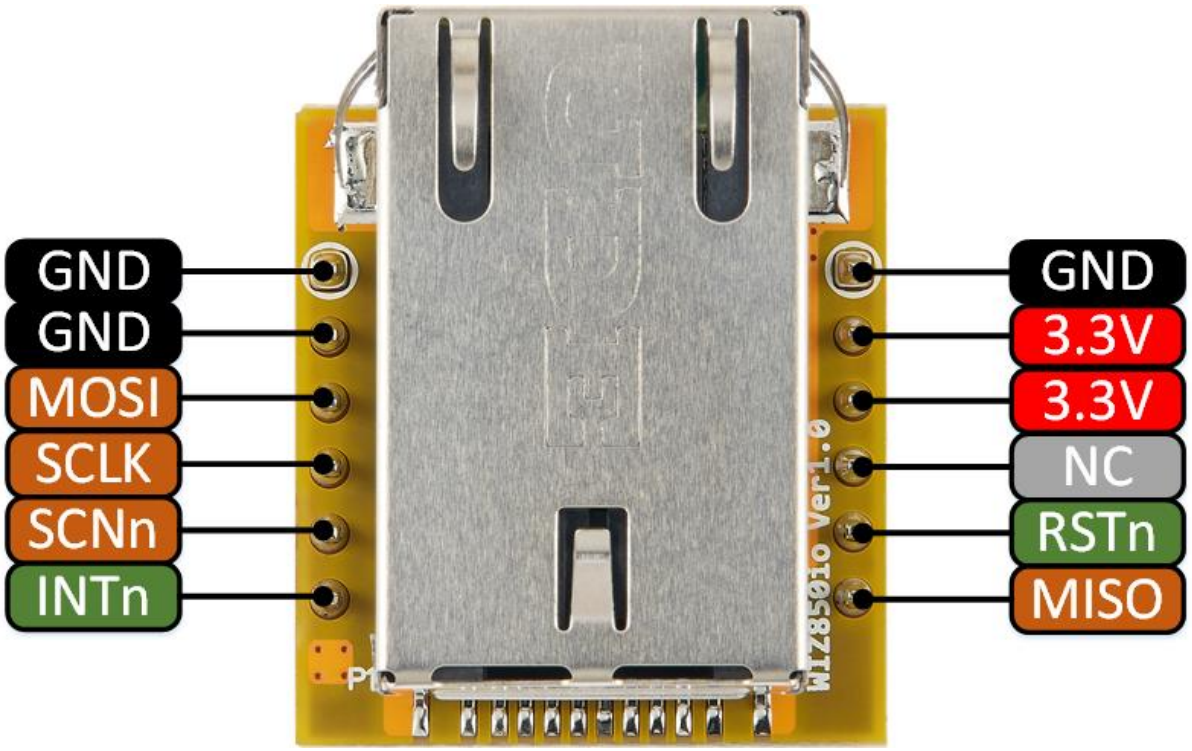
- Supports following Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Supports High Speed Serial Peripheral Interface(SPI MODE 0, 3)
- Internal 32Kbytes Memory for Tx/Rx Buffers
- 10BaseT/100BaseTX Ethernet PHY embedded
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Not support IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- Not support auto MDIX

2. Hardware Specification

2.1. WIZ850io Hardware Summary

- Plugin Network Module.
- Hardware pin compatible with WIZ820io.
- Usable without H/W design for W5500, Transformer & RJ45.
- Fast evaluation for W5500 & MCU in the target board.
- Support high speed SPI interface.
- Support power down mode and Wake-on-LAN function
- Operating Temperature : -40℃ ~ 85℃
- Very small form factor : 23mm x 25.75mm x 18mm
- 1 x 6, 2.54mm Pin Header x 2

2.2. Pinout



2.3. Pin Description

	Pin No.	Pin Type	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	GND	**Ground**
	3	I	MOSI	**SPI Master Out Slave In** This pin is used for SPI MOSI signal pin
	4	I	SCLK	**SPI Clock** This pin is used for SPI Clock Signal pin
	5	I	SCNn	**SPI Slave Select** This pin is used for SPI Slave Select Signal Pin when using SPI interface
	6	I	INTn	**W5500 Interrupt** : Low activity This pin is used for indicating event like socket TCP connection, disconnection, data receiving timeout, WOL(Wake on Lan) and so on occurred in W5500 inside WIZ550io. The interrupt is cleared by writing IR register or Sn_IR. All interrupts are maskable.

	Pin No.	Pin Type	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	3.3V	**Power** : 3.3V power supply
	3	P	3.3V	**Power** : 3.3V power supply
	4	-	NC	**Not Connect**
	5	I	RSTn	**Reset** : Low activity This pin is to initialize WIZ850io. Hold at least 500us after asserted to LOW and keep HIGH until next Reset needed. User need to wait for 50ms after this pin is changed to HIGH to communicate with WIZ850io. (Refer to 5. Timing Diagram)
	6	O	MISO	**SPI Master In Slave Out** This pin is used for SPI MISO signal pin

※ **P : Power , I : Input , O : Output**

3. Characteristic

3.1. DC Characteristic

Symbol	Parameter	Pins	Min	Typ	Max	Unit
V_{DD}	Supply voltage	3.3V	2.97	3.3	3.63	V
V_{IL}	High level input voltage	ALL	2.0	-	5.5	V
V_{IH}	Low level input voltage	ALL	-0.3	-	0.8	V
V_{OL}	Low level output voltage	ALL	-	-	0.4	V
V_{OH}	High level output voltage	ALL	2.4	-	-	V
L_{OL}	Low level output Current	ALL	8.6	13.9	18.9	mA
L_{OH}	High level output Current	ALL	12.5	26.9	47.1	mA
I_{DD}	Supply Current (Normal operation mode)	3.3V	-	132	-	mA
L_{DD}	Supply Current (Power Down mode)	3.3V	-	13	-	mA

3.2. Power Dissipation

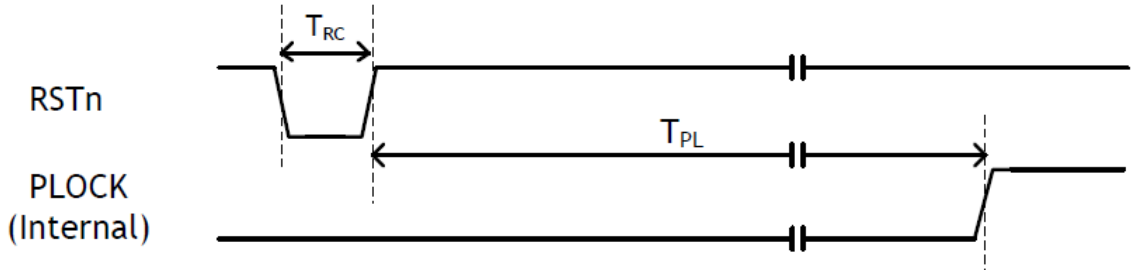
Condition	Min	Typ	Max	Unit
100M Link	-	128	-	mA
10M Link	-	75	-	mA
Un-Link (Auto- negotiation mode)	-	65	-	mA
100M Transmitting	-	132	-	mA
10M Transmitting	-	79	-	mA
Power Down mode	-	13	-	mA

4. SPI Operations

As WIZ850io consists of W5500 and others, SPI operation of WIZ850io follows W5500 SPI specification. For more information about SPI operation of WIZ850io, please refer to W5500 Datasheet.

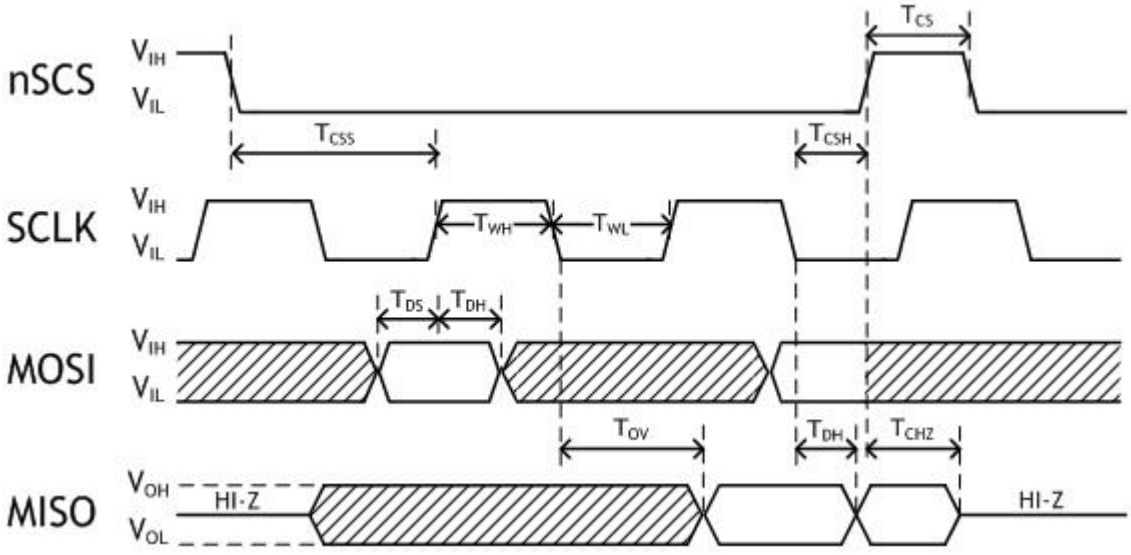
5. Timing Diagram

5.1. Reset Timing



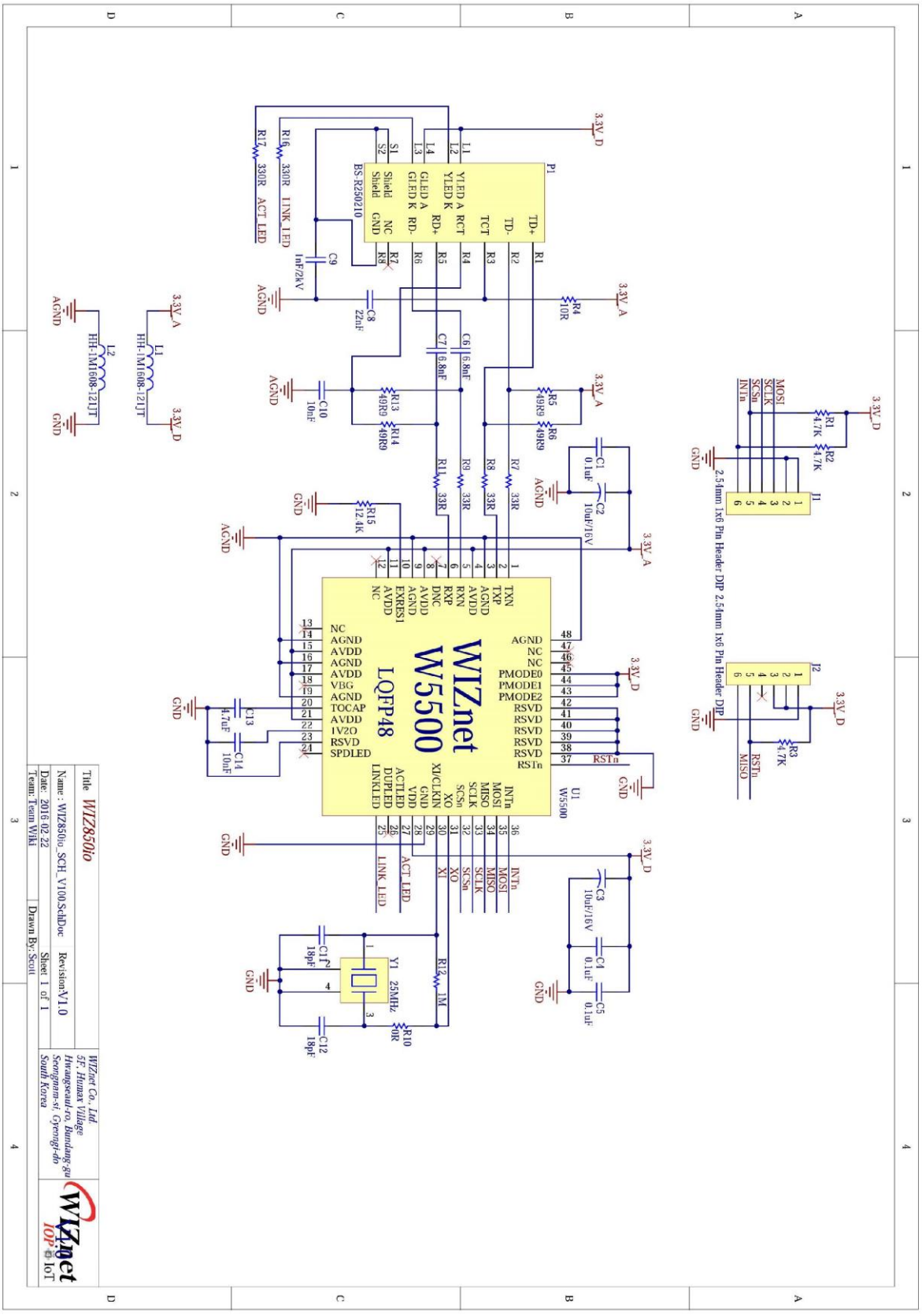
Symbol	Description	Min	Max
T_{RC}	Reset Cycle Time	500us	-
TPL	Internal Auto Configuration	-	50ms

5.2. SPI Timing



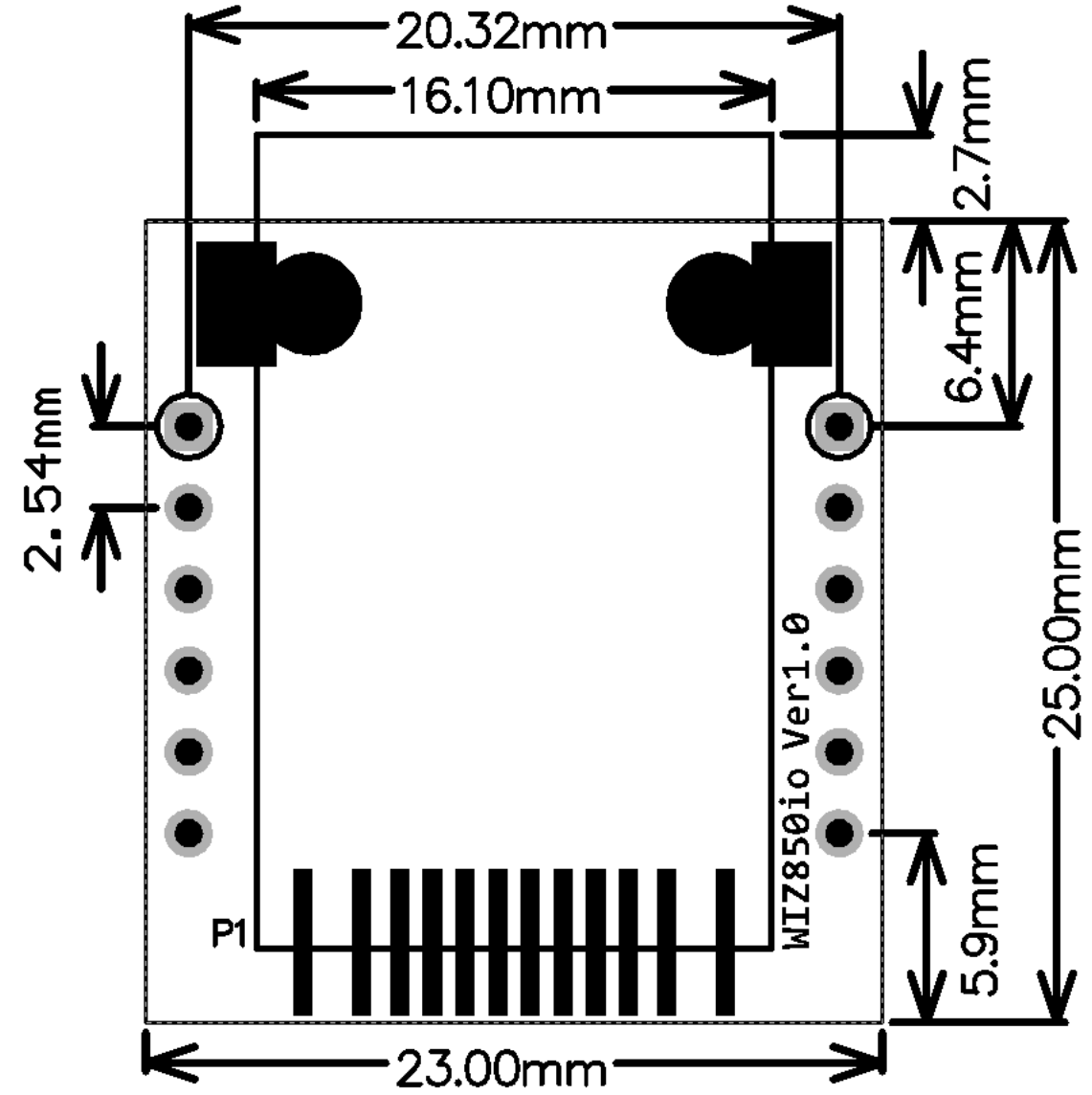
Symbol	Description	Min	Max	Units
F_{SCK}	SCLK Clock Frequency	-	80	MHz
T_{WH}	SCLK High duration	6	-	ns
T_{WL}	SCLK Low duration	6	-	ns
T_{CS}	nSCS High duration	5	-	ns

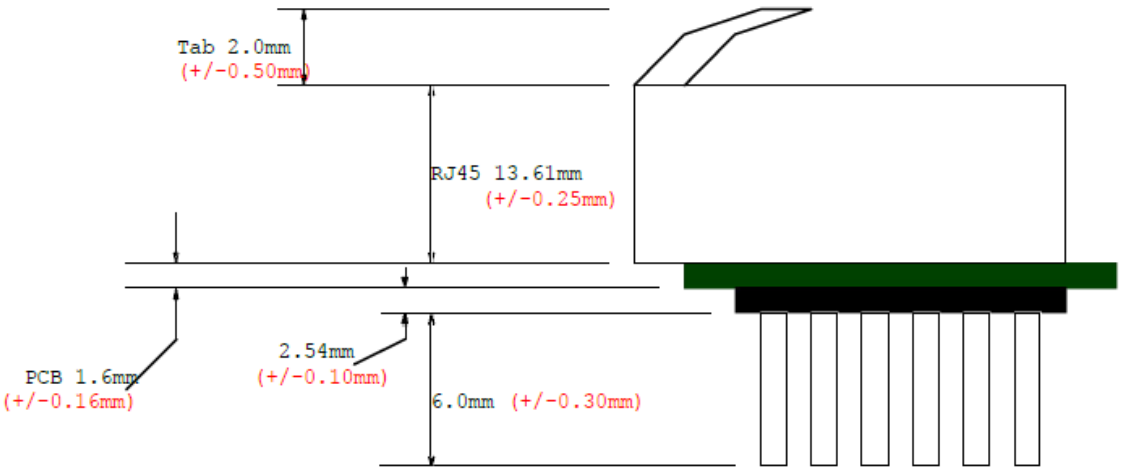
6. Schemetic


WIZnet
W5500
LQFP48
U1
W5500
P1
BS-R250210
J1
2.54mm 1x6 Pin Header DIP
J2
2.54mm 1x6 Pin Header DIP
Y1 25MHz
L1
HH-1M1608-121JT
L2
HH-1M1608-121JT
Title WIZ850io
Name : WIZ850io_SCH_V100.SchDoc
RevisionV1.0
Date: 2016-02-22
Sheet 1 of 1
Team: Team Wiki
Drawn By: Scott
WIZnet Co., Ltd.
5F, Hunan Village
Hwangsaeul-ro, Bundang-gu
Seongnam-si, Gyeonggi-do
South Korea

7. Dimension

3D PDF Link : http://wizwiki.net/wiki/doku.php?id=products:wiz850io:start&#dimension





Total Height: 2mm(Tap) +13.61mm(RJ45) + 1.6mm(PCB) + 8.54mm(Pin Header) = 25.75mm