

1 Introduction

Documentation goes here.

| IP Facts Table | |
|------------------|--|
| Name | Example IP |
| Identifier | org.wqzhao.example_ip |
| Version | 1.0 |
| Author | Wuqiong Zhao (me@wqzhao.org) |
| Device | AMD UltraScale+ |
| Platform | Vivado |
| Design Files | Verilog |
| Simulation Model | Verilog |
| Constraints File | N/A |