Example IP Module v1.0

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1 Introduction

The "Example IP" is just an example. You will need to create your own IP module to use this class to document it elegantly. This `ip-doc` class is designed to help you write beautiful documentation for your IP modules, so you can concentrate on contents only. Basic LaTeX knowledge is required to use this class. Yet, you may further customize this class to suit your needs.

IP Facts Table

Name	Example IP
Identifier	`org.wqzhao.example_ip`
Version	1.0
Author	Wuqiong Zhao (me@wqzhao.org)
Device	AMD UltraScale+
Platform	Vivado
Design Files	Verilog
Simulation Model	Verilog
Constraints File	N/A

I have been working with RFSoC for a while, and I found that the documentation for IP modules is often not as good as it should be. Therefore, I created this class to make it easier for me to document my custom IP modules. I hope you find it useful too.

This LaTeX class is maintained by Teddy van Jerry (Wuqiong Zhao).

2 Features

This module is only an example with minimal features. The features of this IP module are:

- Support AXI4 interface.
- Some features related to LaTeX which is unfortunately not hardware.
  - Beautiful documentation for you to concentrate on writing good contents.
  - Easy to use and customize thanks to the LaTeX3 technology.
  - Fully open source and free at `https://github.com/Teddy-van-Jerry/ip-doc`.
- Other features that you want to impress your users.

3 Usage

3.1 Fundamentals

This class can be used with any LaTeX engine, including `pdflatex`, `lualatex`, and `xelatex`.

3.2 Text

The text is in sans-serif font "TeX Gyre Heros," a "Helvetica" clone. Section numbers are in the left margin.

3.2.1 Subsubsection

Here is a subsubsection, the smallest sectioning command that comes with numbering.

Paragraph. Here is a paragraph, which has a run-in header.

3.3 Math

Math fonts are still the serif ones. For example $a^2 + b^2 = c^2$. Display equations can also be used:

$$\int_0^1 x^2 \, \mathrm{d}x = \frac{1}{3}. \tag{1}$$

3.4 Figures and Tables

Figures and tables are useful to illustrate your IP module. Figure 1 shows a waveform plot of integrated logic analyzer (ILA) captured QPSK packet.

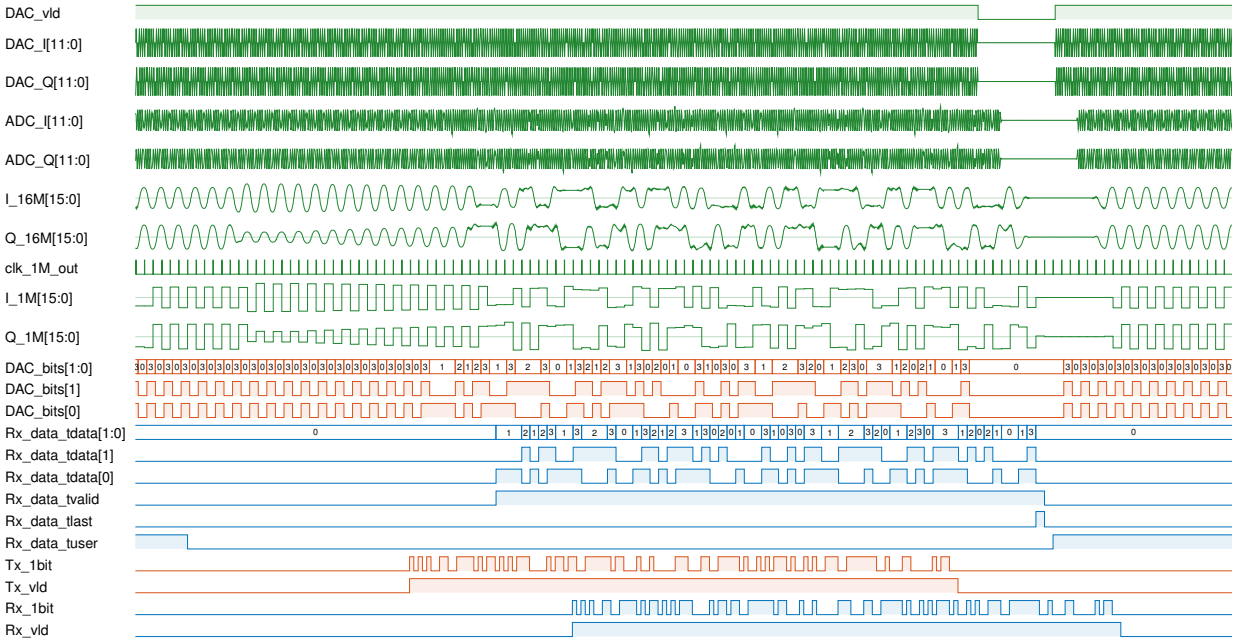

Figure 1: A QPSK packet captured by ILA. [1]

4 Know Issues

1. The `factstable` environment internally uses the `wrapstuff` package, which may cause some issues. Its position may not be as expected, so you may add parameters to the `wrapstuff` environment via the first optional argument of the `factstable` environment. Another known issue is in some places the `itemize` and `enumerate` environment has to be separated by a blank line (or `\par`) from the text.

2. The documentation of this class is not complete.

5 Further Readings

Ti*k*Z is useful to create beautiful diagrams in LaTeX. These can be useful to illustrate the architecture of your IP module. An example paper about high-level-synthesis (HLS) using Ti*k*Z is [2], with open access PDF at https://wqzhao.org/assets/zhao2024flexible.pdf.

References

[1] Wuqiong Zhao. Dual-mode PSK transceiver on SDR with FPGA. https://wqzhao.org/assets/sdr-psk-fpga.pdf, 2024.

[2] Wuqiong Zhao, Changhan Li, Zhenhao Ji, Zhichen Guo, Xuanbo Chen, You You, Yongming Huang, Xiaohu You, and Chuan Zhang. Flexible high-level synthesis library for linear transformations. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 71(7):3348–3352, July 2024.