

Dual-Mode PSK Transceiver on SDR With FPGA

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(This is a draft version and has not been completed yet.)

Abstract—In this experiment, we implement a dual-mode PSK transceiver on SDR with FPGA, supporting both BPSK and QPSK. Moreover, the transceiver is designed to be able to switch between the two modes by introducing packet-based communication, where modulation information can be extracted from the packet header.

Index Terms—Phase-shift keying (PSK), software-defined radio (SDR), transceiver design, modulation, demodulation, field programmable gate array (FPGA).

I. INTRODUCTION

SOFTWARE-DEFINED radio (SDR) is interesting, like application in millimeter wave [1]. FPGA is also interesting! Instead of employing high-level synthesis (HLS) [2], we directly implement the transceiver on FPGA using hardware description language (HDL) Verilog, for a better control of the underlying hardware.

The design source (Vivado project) and this paper (in \LaTeX) are open source [3].

II. SYSTEM OVERVIEW

A. Software-Defined Radio

eNodeX

B. Transceiver Design

The current transmitter and receiver are implemented on the same FPGA, but can be readily extended to different FPGAs with small frequency offsets. The system overview is shown in Fig. 1.

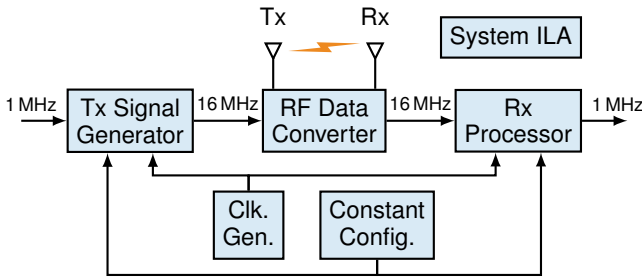


Fig. 1. Transceiver system overview.

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Online URL: <https://go.wqzhao.org/sdr-psk-fpga>

Clock Generator. All reset signals are generated using Processor System Reset Modules [4], which can provide synchronized power-up reset signals.

RF Data Converter. This block contains analog-to-digital converter (ADC) and digital-to-analog converter (DAC), enabled by a vendored AD9361 module.

Tx Signal Generator.

Rx Processor. This block is responsible to process the received signal, including demodulation and data extraction from a packet. It is the most complicated block in the system.

System ILA. The system integrated logic analyzer (system ILA) [5] is used to observe the internal signals.

Constant Configurations. Several parameters can be configured in this block. Most importantly, the mode control constants (MODE_CTRL) are shown in Table I.

TABLE I
MODE CONTROL CONSTANTS

Mode	Localparam	Value	is_bpsk	Packet
BPSK	MODE_BPSK	4'b0001 (1)	1'b1	No
QPSK	MODE_QPSK	4'b0010 (2)	1'b0	No
Mixed	MODE_MIX	4'b0100 (4)	variable	Yes

C. BPSK/QPSK Modulation

The BPSK and QPSK modulation constellation graphs used in our system are shown in Fig. 2. Different from the traditional setting, our adopted BPSK constellation in Fig. 2(a) is a combination of I and Q components. This is to make sure the phases used in BPSK are among those in QPSK, to ensure a smooth transition between the two modes, especially because the header field is always modulated in BPSK.

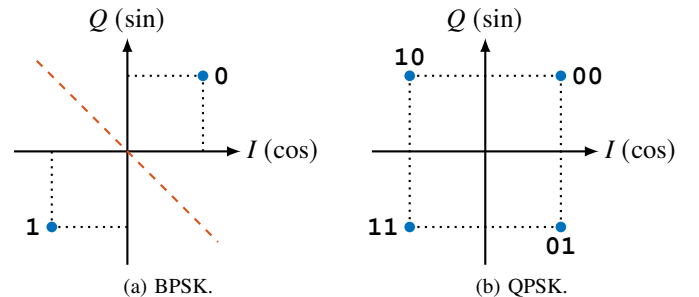


Fig. 2. BPSK/QPSK modulation constellation used in our system.

$$u_I(r) = y_I(r - \frac{1}{2}) [\text{sgn}(y_I(r)) - \text{sgn}(y_I(r-1))] + y_O(r - \frac{1}{2}) [\text{sgn}(y_O(r)) - \text{sgn}(y_O(r-1))], \quad (4)$$

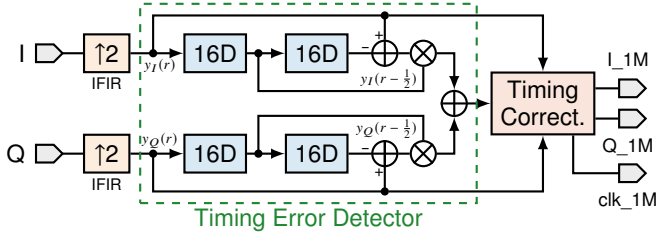


Fig. 4. Structure of a Gardner loop for symbol timing synchronization.

where r has a symbol frequency of 1.024 MHz. For better timing performance, we linearly interpolate the 16.385 MHz input I/Q data to 32.768 MHz. Therefore, $y_I(r-1)$ and $y_Q(r-1)$ are delayed by 32 clocks. In FPGA implementation, for each I/Q stream, two shift registers of depth 16 are used. Notably, since we adopt the BPSK constellation in Fig. 2(a), the symbol timing error depends on both I and Q components, the same as QPSK.

V. PACKET-BASED COMMUNICATION

A. Frame Structure

The frame structure is shown in Fig. 5.

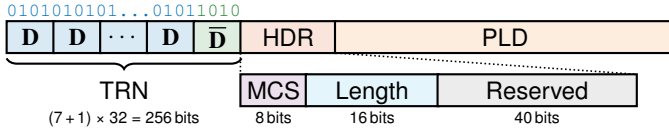


Fig. 5. Frame structure of the packet-based communication.

Training (TRN). The training field is used to provide packet timing information (coarse synchronization), as well as synchronize the carrier and symbol timing. It consists of 7 repetitions of **D** and one **D̄**, where **D** and **D̄** are of length 32. **D** and **D̄** are repetitive sequences of ‘01’ and ‘10’, respectively. The training field from bit 0 to $(7+1) \times 32 - 1 = 255$ is defined as

$$\text{TRN}[i] = \begin{cases} \text{mod}(i, 2), & i = 0, 1, \dots, 223, \\ \text{mod}(i + 1, 2), & i = 224, 225, \dots, 255. \end{cases} \quad (5)$$

Notably, the phase transition from bit 223 to 224 is used to indicate the boundary of the packet.

Header (HDR). The header field is used to provide packet information, including the modulation and coding scheme (MCS) and the packet length (Length) in bits. The remaining bits are reserved for future use. The MCS field currently only determines the use of BPSK or QPSK. The MCSs for BPSK and QPSK are defined as ‘01010101’ and ‘10101010’ respectively.

Payload (PLD). The payload field is used to carry the actual data. Its length in bits (1 bit for each BPSK symbol, 2 bits for each QPSK symbol) should match the Length field in the header.

B. Packetizer Design

The packetizer FSM has 5 states: IDLE, HDR, PLD, LAST and WAIT. The IDLE state is used to wait for the packet start.

It transits to the HDR state when the valid and ready signals are both high, i.e., the packet starts transmitting. The HDR state is used to transmit the header (including TRN and HDR)¹, as discussed in Section V-A. It then transmits to the PLD state to transmit the payload stored in the FIFO. Notably, the FIFO depth should not be smaller than the header length (i.e. 32).

C. Depacketizer Design

D. SPB Detection

SPD detection consists of strength detection (SD), packet detection (PD) and boundary detection (BD). They jointly provide information for the coarse packet timing.

1) **Strength Detection (SD):** The strength detection checks the baseband I/Q amplitude from the Costas loop. It is useful because the PSK detector will always output a value, and it can confuse the packet parsing when the noise coincides with the packet sequence. For stability, the **SD_flag** is asserted when either the I or Q signal amplitude is larger than **RX_SD_THRESHOLD** at one clock within the window of **RX_SD_WINDOW** clocks.

2) **Packet Detection (PD):** The presence of a packet can be identified by detecting repetitive ‘010101...’ sequence (modulated using BPSK). This can be performed by checking the continuous 1s for the differential results. The **PD_flag** is asserted when the differential results remain 1 for **RX_PD_WINDOW** clocks. Interestingly, the packet detection itself does not require a synchronized carrier, as a carrier phase shift does not significantly affect the ‘01’ sequence detection.

3) **Boundary Detection (BD):** Exploiting the phase transition from bit 223 to 224 in the training field (see Section V-A and Fig. 5), the boundary detection can be performed by checking the differential value being 0 after the **PD_flag** being asserted. To ensure stability, the **BD_flag** is asserted after **RX_BD_WINDOW** clocks of continuous 1s in differential values.

VI. SIMULATION RESULTS

In all Verilog simulation, random is added to the Rx ADC, to better simulate the real-world scenario.

A. Transmitter

The transmitter DAC simulation results are shown in Fig. 6.

B. Carrier Synchronization Convergence

The simulation results of the Costas loop are shown in Fig. 7. In the BPSK mode, the Costas loop can successfully handle the CFO smaller than 7.81 kHz. It can be verified by the fact that the feedback saturates around a constant (corresponding to the CFO value), which . In the QPSK mode, the value is 1.96 kHz. The convergence is relatively fast.

Notably, the convergence performance of QPSK is poorer than BPSK in the current parameter set, which is by design.

¹For the packetizer and the depacketizer, we do not distinguish TRN and HDR for simplicity, and they are called the header in contrast to the payload.

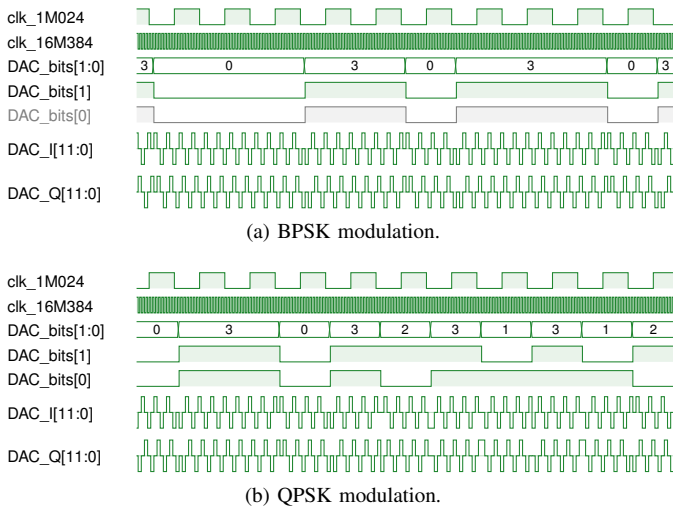


Fig. 6. DAC simulation results of the transmitter.

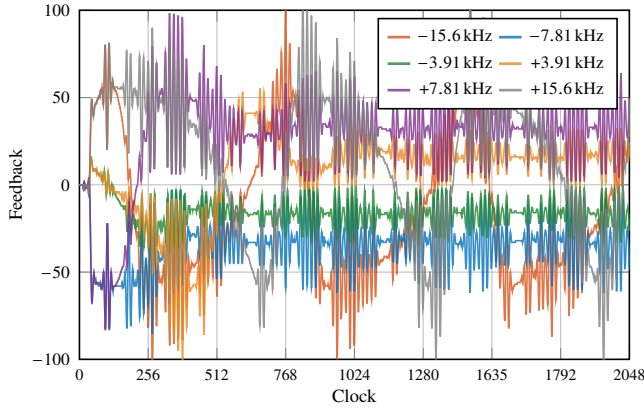


Fig. 7. Carrier synchronization for BPSK. The feedback value after the loop filter v.s. time, with different CFO.

For a dual-mode system which transmits payload in both BPSK and QPSK with a BPSK header, so the carrier synchronization is achieved at the BPSK header, therefore, QPSK does not need a strong feedback. Furthermore, the smaller feedback makes the BPSK and QPSK transmission smoother, avoiding a sudden phase jump of 90° .

C. Mixed-Mode Receiver

In this simulation, we show the successful transmission of packets in both BPSK and QPSK modulations. The simulation results are shown in Fig. 8.

VII. FPGA IMPLEMENTATION

The design is implemented in Vivado 2022.2.

The hardware resources consumption on Zynq-7020 with the default synthesis and implementation strategy is shown in Table II. Therefore, the design itself is area-efficient, and can be readily incorporated into a larger system.

VIII. EXPERIMENT RESULTS ON SDR

The experiment results are observed via a system ILA in Vivado, and 4 general-purpose input/output (GPIO) pins are

TABLE II
HARDWARE RESOURCES CONSUMPTION ON ZYNQ-7020

Resource	Utilization	Available	Util. Rate
LUT	7,248	53,200	8.04%
LUTRAM	1,121	17,400	6.44%
FF	8,144	106,400	7.65%
BRAM	27	140	19.29%
DSP	51	220	23.18%
IO	33	200	16.50%
BUFG	10	32	31.25%
MMCM	2	4	50.00%

used to output some 1-bit signals, including the 1-bit Tx and Rx data stream and their corresponding clock.

In our design, 4 GPIO pins are connected, as listed in Table III. Fig. 9 shows the oscilloscope results of the GPIO outputs.

TABLE III
GPIO PIN CONNECTIONS

Pin	Signal
GPIO_TH1	Tx 1-bit sequence (clock: 1.024 MHz or 2.048 MHz)
GPIO_TH2	Rx 1-bit sequence (sync. w/ Rx timing clock when BPSK)
GPIO_TH3	2.048 MHz global clock from the clock divider
GPIO_TH4	Rx timing clock (~ 1.024 MHz)

Fig. 9(a) and Fig. 9(b) connects the GPIO_TH1 and GPIO_TH2 pins, showing the transmitted 1-bit sequence (Tx) and the respective received 1-bit sequence (Rx). Clearly, the sequence is successfully recovered in both cases, with a certain time delay. The structure of pn_5 sequence in BPSK is clearly seen in Fig. 9(a), which has a bit frequency of 1.024 MHz. By contrast, the bit frequency of QPSK packets in Fig. 9(b) is 2.048 MHz.

IX. DISCUSSIONS

A. Possible Enhancement

Frame structure design. CRC and/or checksums can be added to the frame structure.

Changing parameters on the fly. AXI peripheral [8] can be used to change the parameters in the Constant_Config on the fly, if the board allows.

B. Possible Extensions Beyond the Experiment

The training (TRN) field can be better utilized for additional experiments. For example, signal-to-noise (SNR) can be estimated at the TRN field.

Channel estimation algorithm [9], [10].

Auto generation [11].

X. CONCLUSION

In this paper,



Fig. 8. Mixed-mode simulation results.

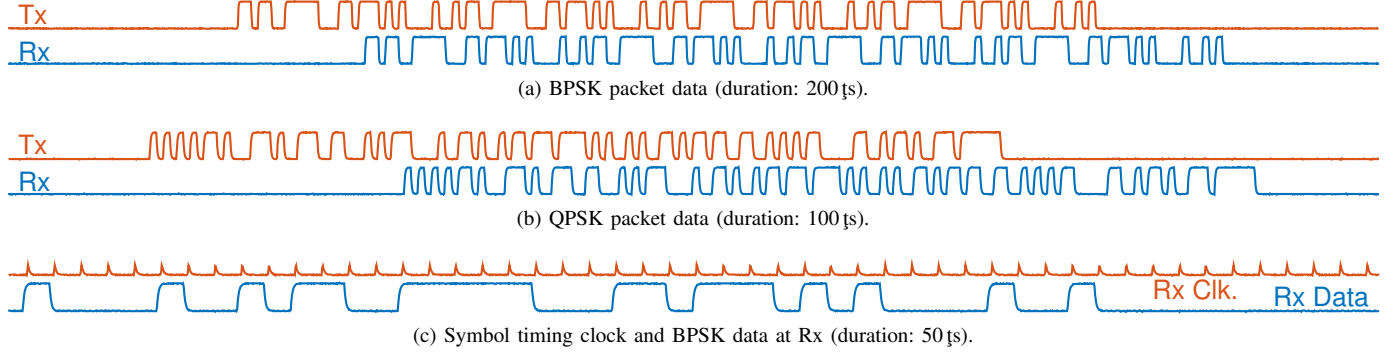


Fig. 9. Two-channel oscilloscope results of GPIO outputs.

APPENDIX A BLOCK DIAGRAMS

A. Block Diagrams Design

B. Debugging With Block Diagrams

AXI connections. 1. connection one out of the bus. 2. `FREQ_HZ` property.

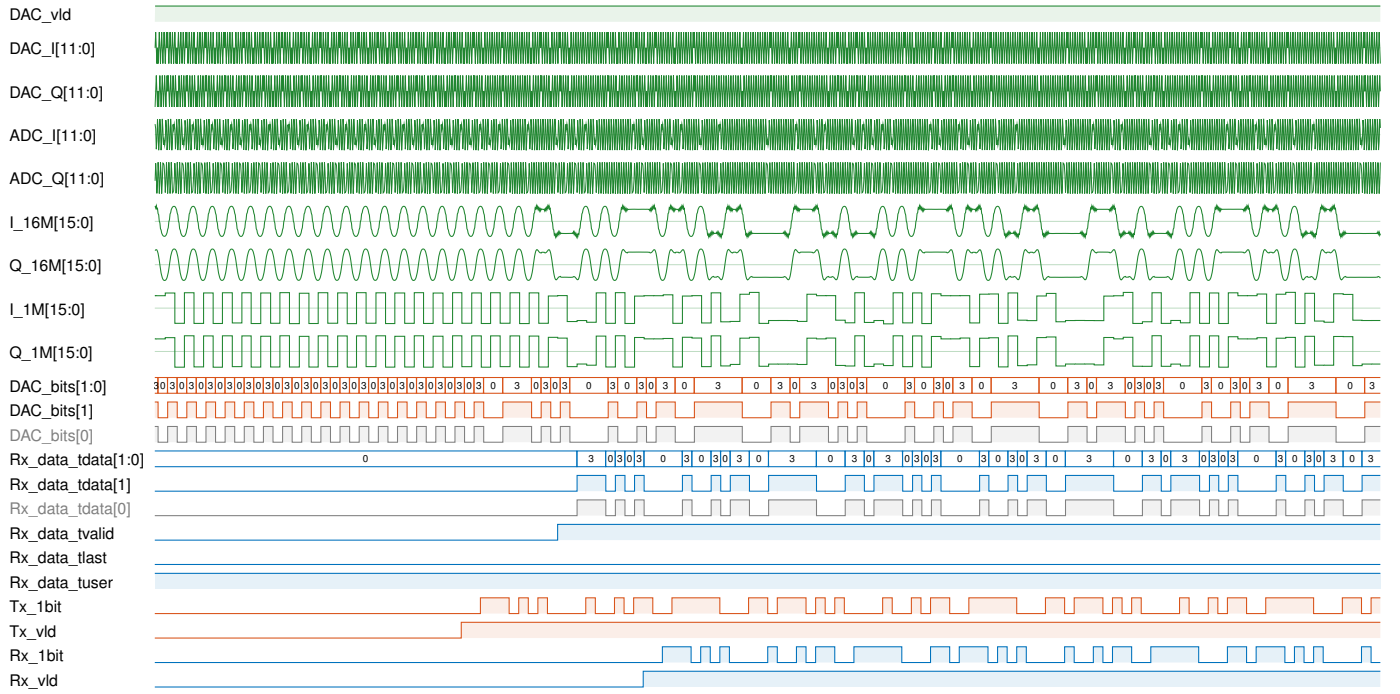
Testbenches for block diagrams.

APPENDIX B FIGURES IN THIS PAPER

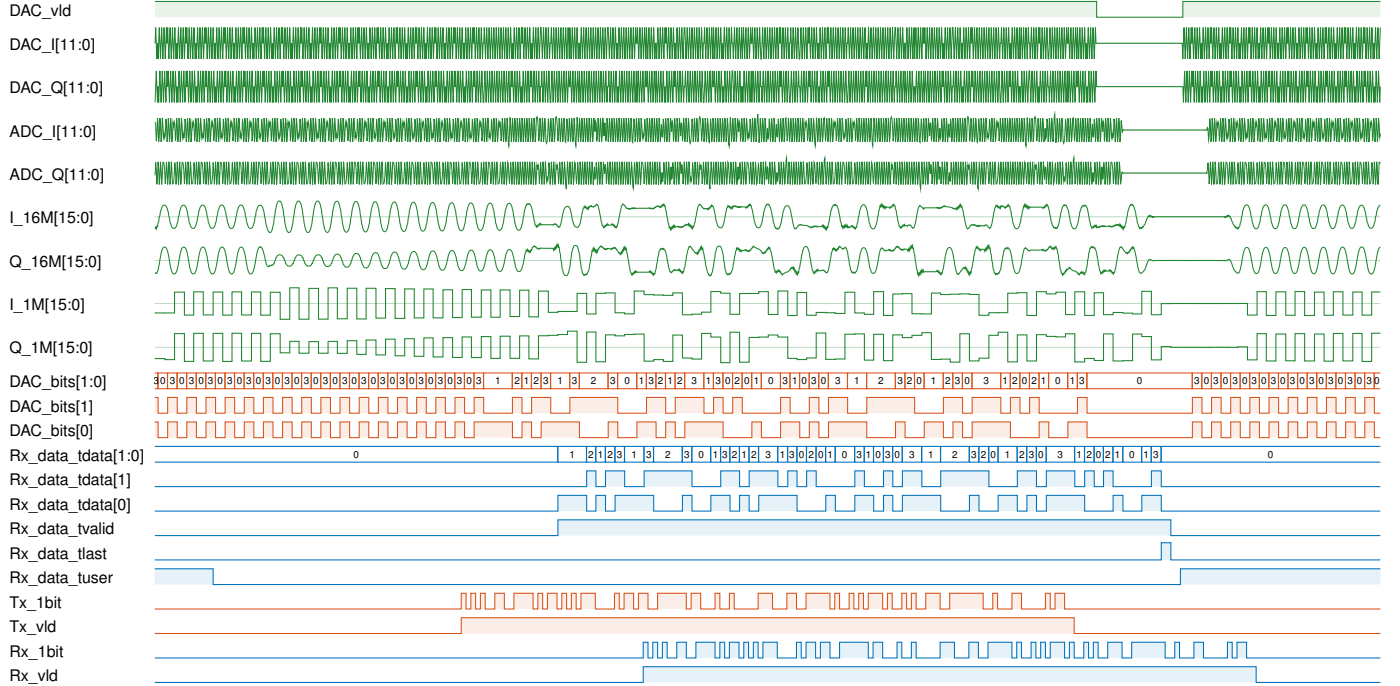
All figures except for block diagrams in this paper are created using TikZ, part of L^AT_EX. The way I create them is quite interesting, and you can find the source code in the GitHub repository [3].

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(a) A BPSK packet.



(b) A QPSK packet.

Fig. 10. System ILA results.

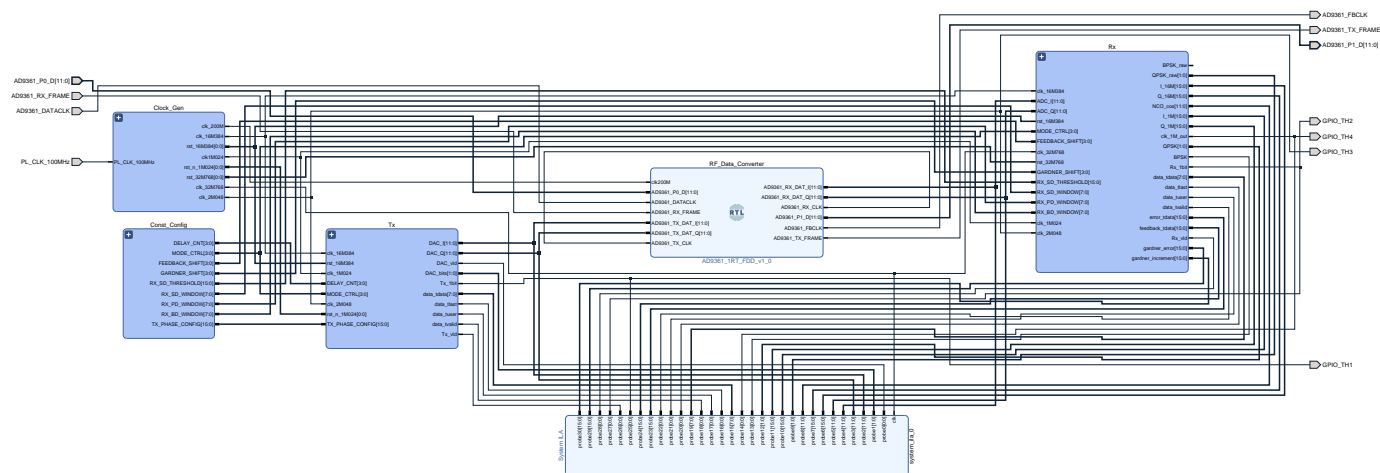


Fig. 11. Top block diagram.