Dual-Mode PSK Transceiver on SDR With FPGA

Wuqiong Zhao, *Student Member, IEEE*

***Abstract*—In this experiment, we implement a dual-mode PSK transceiver on SDR with FPGA, supporting both BPSK and QPSK. Moreover, the transceiver is designed to be able to switch between the two modes by introducing packet-based communication, where modulation information can be extracted from the packet header.**

***Index Terms*—Phase-shift keying (PSK), software-defined radio (SDR), transceiver design, modulation, demodulation, field programmable gate array (FPGA).**

I. Introduction

SOFTWARE-DEFINED radio (SDR) is interesting, like application in millimeter wave [1]. FPGA is also interesting!

Instead of employing high-level synthesis (HLS) [2], we directly implement the transceiver on FPGA using hardware description language (HDL) Verilog, for a better control of the underlying hardware.

The design source (Vivado project) and this paper (in LaTeX) are open source [3].

II. System Overview

A. Software-Defined Radio

B. Transceiver Design

The current transmitter and receiver are implemented on the same FPGA, but can be readily extended to different FPGAs with small frequency offsets. The system overview is shown in Fig. 1.

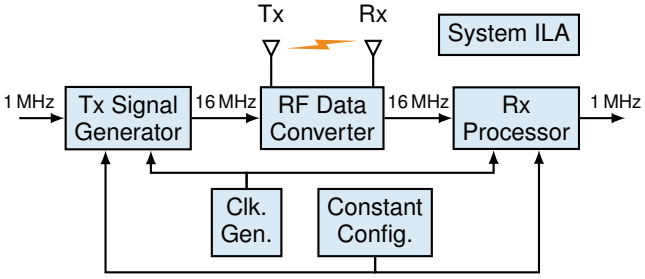


Fig. 1. Transceiver system overview.

Clock Generator. All reset signals are generated using Processor System Reset Modules [4], which can provide synchronized power-up reset signals.

RF Data Converter. This block is contains analog-to-digital converter (ADC) and digital-to-analog converter (DAC), enabled by a vendored AD9361 module.

Tx Signal Generator.

Rx Processor.

System ILA. The system integrated logic analyzer (system ILA) [5] is used to observe the internal signals.

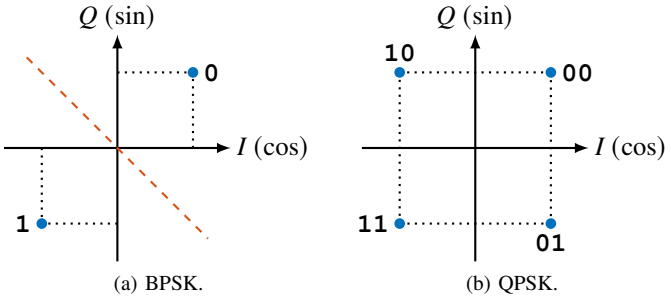
Constant Configurations. Several parameters can be configured in this block. Most importantly, the mode control constants (`MODE_CTRL`) are shown in Table I.

TABLE I
Mode Control Constants

Mode	Localparam	Value	`is_bpsk`	Packet
BPSK	`MODE_BPSK`	`4'b0001` (1)	`1'b1`	No
QPSK	`MODE_QPSK`	`4'b0010` (2)	`1'b0`	No
Mixed	`MODE_MIX`	`4'b0100` (4)	variable	Yes

C. BPSK/QPSK Modulation

The BPSK and QPSK modulation constellation graphs used in our system are shown in Fig. 2. Different from the traditional setting, out adopted BPSK constellation in Fig. 2(a) is a combination of I and Q components.



(a) BPSK. (b) QPSK.

Fig. 2. BPSK/QPSK modulation constellation used in our system.

III. Transmitter

A. Carrier NCO

The carrier frequency is generated by a numerically controlled oscillator (NCO). In Vivado, we use the Direct Digital Synthesis (DDS) Compiler IP core to generate the NCO.

B. PSK Modulation

C. Pseudo-random Noise (PN) Generator

In this experiment, the transmitted signal are pseudo-random noise (PN) sequences. Typically, we implement the PN generator with $N = 4$ and $N = 5$.

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Wuqiong Zhao is with Southeast University, Nanjing 211189, China. (e-mail: wqzhao@seu.edu.cn, website: https://wqzhao.org).

Online URL: https://go.wqzhao.org/sdr-psk-fpga

The Verilog code for the module `PN_Gen` is shown below.

```
module PN_Gen # (parameter N = 5) (
  input      clk,
  output reg pn
);
  reg [N-1:0] PN_buf = 1; wire rst;
  generate
  if (N == 5)
    always @ (posedge clk)
      if (rst) begin PN_buf <= 5'd1; pn <= 0; end
      else begin
        PN_buf <= { PN_buf[3:0], PN_buf[4] ^ PN_buf[2] };
        pn <= PN_buf[4];
      end
  else if (N == 4)
    always @ (posedge clk)
      if (rst) begin PN_buf <= 4'd1; pn <= 0; end
      else begin
        PN_buf <= { PN_buf[2:0], PN_buf[3] + PN_buf[2] };
        pn <= PN_buf[3];
      end
  else ; // NOT implemented yet!
  endgenerate
  assign rst = !(|PN_buf);  // reset when PN_buf is all 0
endmodule
```

IV. Receiver

A. Overview

B. Carrier Synchronization Using Costas Loop

Costas loop [6].

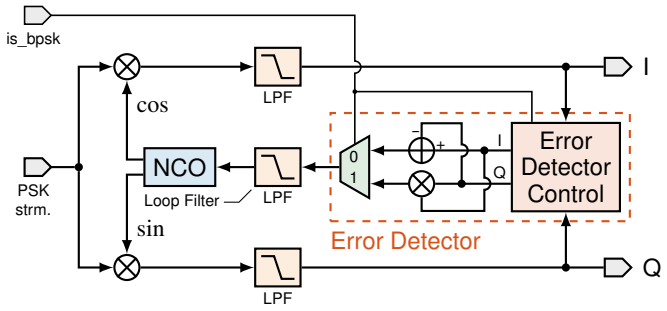


Fig. 3. Costas loop for carrier synchronization with BPSK/QPSK support.

```
if (is_bpsk) begin // BPSK
  out_I_tdata <= in_I_tvalid ? in_I_tdata + in_Q_tdata : 0;
  out_Q_tdata <= in_Q_tvalid ? in_I_tdata - in_Q_tdata : 0;
end
else begin // QPSK
  out_I_tdata <= in_I_tvalid ? (in_Q_tdata[WIDTH-1] ?
    -in_I_tdata : in_I_tdata) >> 6 : 0;
  out_Q_tdata <= in_Q_tvalid ? (in_I_tdata[WIDTH-1] ?
    -in_Q_tdata : in_Q_tdata) >> 6 : 0;
end
```

C. Symbol Synchronization Using Gardner Loop

A Gardner loop [7] is used to achieve symbol (timing) synchronization. The structure of a Gardner loop is shown in Fig. 4.

To reduce implementation complexity, we use the sign of strobe values as mentioned in [7]. The total symbol timing error considering I and Q components is

$$u_t(r) = y_I(r-\tfrac{1}{2})\left[\operatorname{sgn}\left(y_I(r)\right) - \operatorname{sgn}\left(y_I(r-1)\right)\right] + y_Q(r-\tfrac{1}{2})\left[\operatorname{sgn}\left(y_Q(r)\right) - \operatorname{sgn}\left(y_Q(r-1)\right)\right], \quad (1)$$

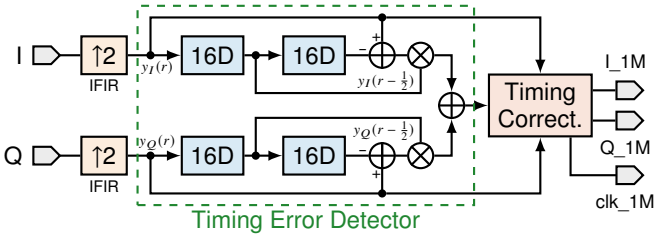


Fig. 4. Structure of a Gardner loop for symbol timing synchronization.

where r has a symbol frequency of 1.024 MHz. For better timing performance, we linearly interpolate the 16.385 MHz input I/Q data to 32.768 MHz. Therefore, $y_I(r-1)$ and $y_Q(r-1)$ are delayed by 32 clocks. In FPGA implementation, for each I/Q stream, two shift registers of depth 16 are used. Notably, since we adopt the BPSK constellation in Fig. 2(a), the symbol timing error depends on both I and Q components, the same as QPSK.

V. Packet-Based Communication

A. Frame Structure

The frame structure is shown in Fig. 5.

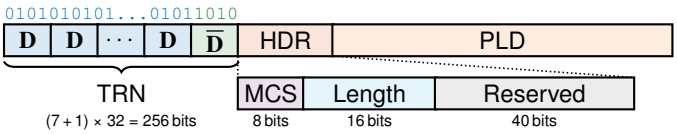


Fig. 5. Frame structure of the packet-based communication.

Training (TRN). The training field is used to provide packet timing information (coarse synchronization), as well as synchronize the carrier and symbol timing. It consists of 7 repetitions of **D** and one $\overline{\mathbf{D}}$, where **D** and $\overline{\mathbf{D}}$ are of length 32. **D** and $\overline{\mathbf{D}}$ are repetitive sequences of '01' and '10', respectively. The training field from bit 0 to $(7+1)\times 32-1 = 255$ is defined as

$$\mathrm{TRN}[i] = \begin{cases} \mathrm{mod}(i,2), & i = 0,1,\ldots,223, \\ \mathrm{mod}(i+1,2), & i = 224,225,\ldots,255. \end{cases} \quad (2)$$

Notably, the phase transition from bit 223 to 224 is used to indicate the boundary of the packet.

Header (HDR). The header field is used to provide packet information, including the modulation and coding scheme (MCS) and the packet length (Length) in bits. The remaining bits are reserved for future use. The MCS field currently only determines the use of BPSK or QPSK. The MCSs for BPSK and QPSK are defined as '01010101' and '10101010' respectively.

Payload (PLD). The payload field is used to carry the actual data. Its length in bits (1 bit for each BPSK symbol, 2 bits for each QPSK symbol) should match the Length field in the header.

B. Packetizer Design

C. Depacketizer Design

D. SPB Detection

1) Strength Detection (SD):

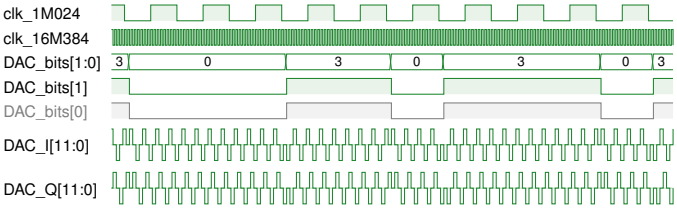
2) Packet Detection (SD):

3) Boundary Detection (BD):

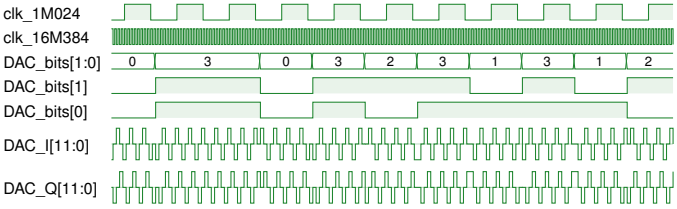
VI. Simulation Results

A. Transmitter

The transmitter DAC simulaiton results are shown in Fig. 6.



(a) BPSK modulation.



(b) QPSK modulation.

Fig. 6. DAC simulation results of the transmitter.

B. Carrier Synchronization Convergence

C. Mixed-Mode Receiver

VII. Experiment Results on SDR

The design is implemented in Vivado 2022.2. The experiment results are observed via a system ILA in Vivado, and 4 general-purpose input/output (GPIO) pins are used to output some 1-bit signals, including the 1-bit Tx and Rx data stream and their corresponding clock.

In our design, 4 GPIO pins are connected, as listed in Table II. Fig. 7 shows the oscilloscope results of the GPIO outputs.

TABLE II
GPIO Pin Connections

Pin	Signal
`GPIO_TH1`	Tx 1-bit sequence (clock: 1.024 MHz or 2.048 MHz)
`GPIO_TH2`	Rx 1-bit sequence (sync. w/ Rx timing clock when BPSK)
`GPIO_TH3`	2.048 MHz global clock from the clock divider
`GPIO_TH4`	Rx timing clock (~1.024 MHz)

Fig. 7(a) and Fig. 7(b) connects the `GPIO_TH1` and `GPIO_TH2` pins, showing the transmitted 1-bit sequence (Tx) and the respective received 1-bit sequence (Rx). Clearly, the sequence is successfully recovered in both cases, with a certain time delay. The structure of `pn_5` sequence in BPSK is clearly seen in Fig. 7(a), which has a bit frequency of 1.024 MHz. By contrast, the bit frequency of QPSK packets in Fig. 7(b) is 2.048 MHz.

VIII. Discussions

A. Possible Enhancement

Frame structure design. CRC and/or checksums can be added to the frame structure.

Changing parameters on the fly. AXI peripheral [8] can be used to change the parameters in the `Constant_Config` on the fly, if the board allows.

B. Possible Extensions Beyond the Experiment

The training (TRN) field can be better utilized for additional experiments. For example, signal-to-noise (SNR) can be estimated at the TRN field.

Channel estimation algorithm [9], [10].

Auto generation [11].

IX. Conclusion

In this paper,

Appendix A
Block Diagrams

Appendix B
Figures in This Paper

References

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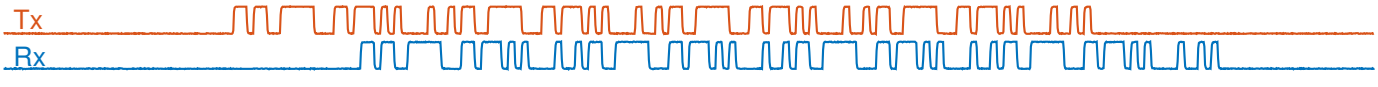
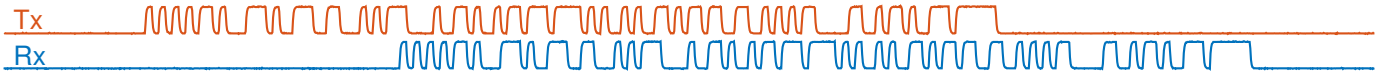
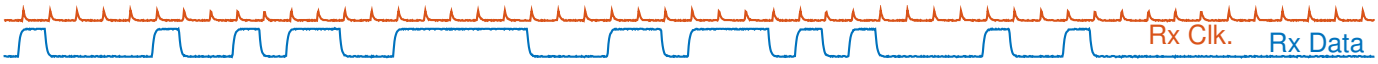


(a) BPSK packet data (duration: 200 μs).

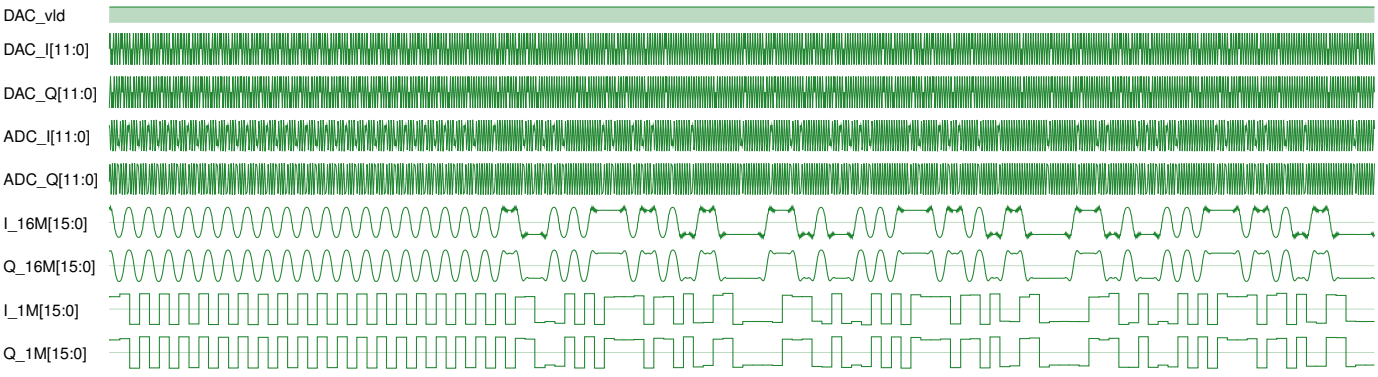


(b) QPSK packet data (duration: 100 μs).

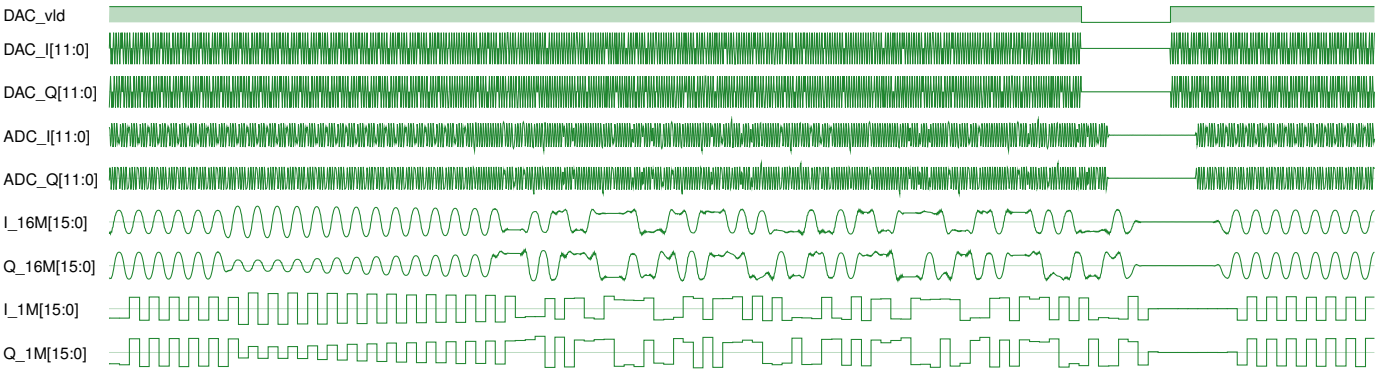


(c) Symbol timing clock and BPSK data at Rx (duration: 50 μs).

Fig. 7. Two-channel oscilloscope results of GPIO outputs.



(a) A BPSK packet.



(b) A QPSK packet.

Fig. 8. System ILA results.

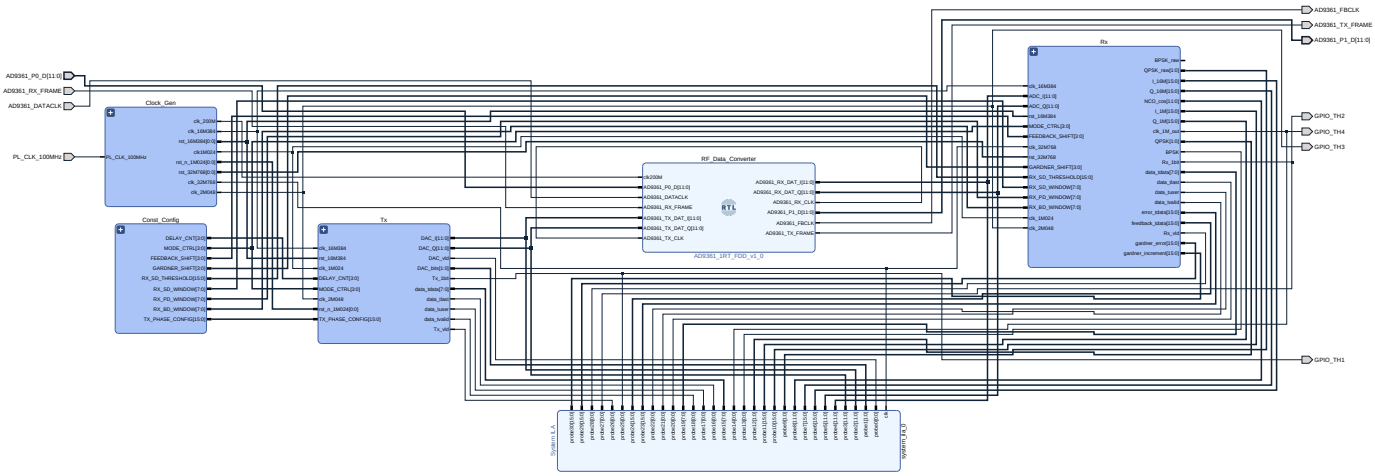


Fig. 9. Top block diagram.