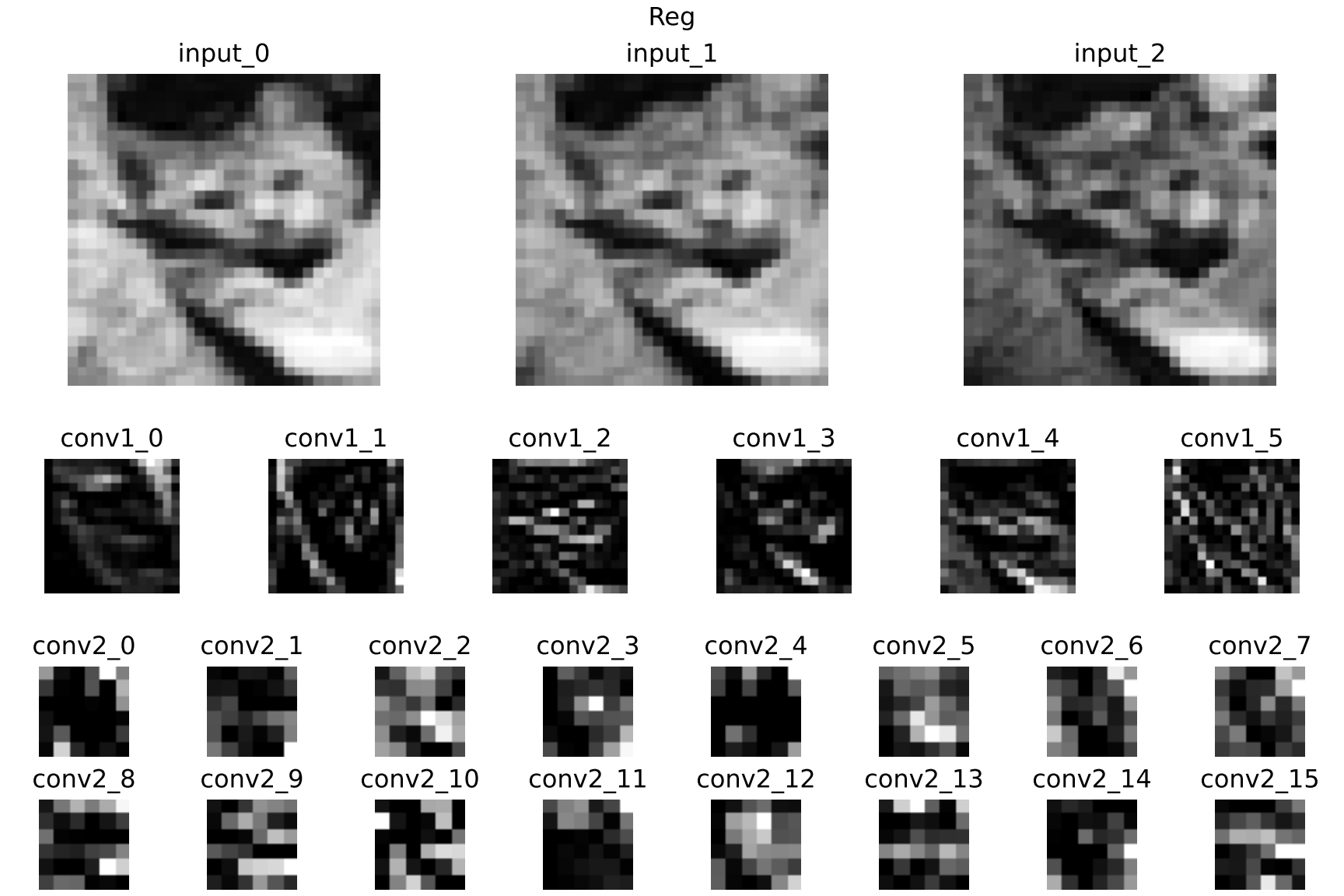
Reg
input_0
input_1
input_2
conv1_0
conv1_1
conv1_2
conv1_3
conv1_4
conv1_5
conv2_0
conv2_1
conv2_2
conv2_3
conv2_4
conv2_5
conv2_6
conv2_7
conv2_8
conv2_9
conv2_10
conv2_11
conv2_12
conv2_13
conv2_14
conv2_15