
STM32
CubeMX

1. Description

1.1. Project

Project Name	stm_W6100_bus
Board Name	NUCLEO-H723ZG
Generated with:	STM32CubeMX 6.2.1
Date	04/22/2021

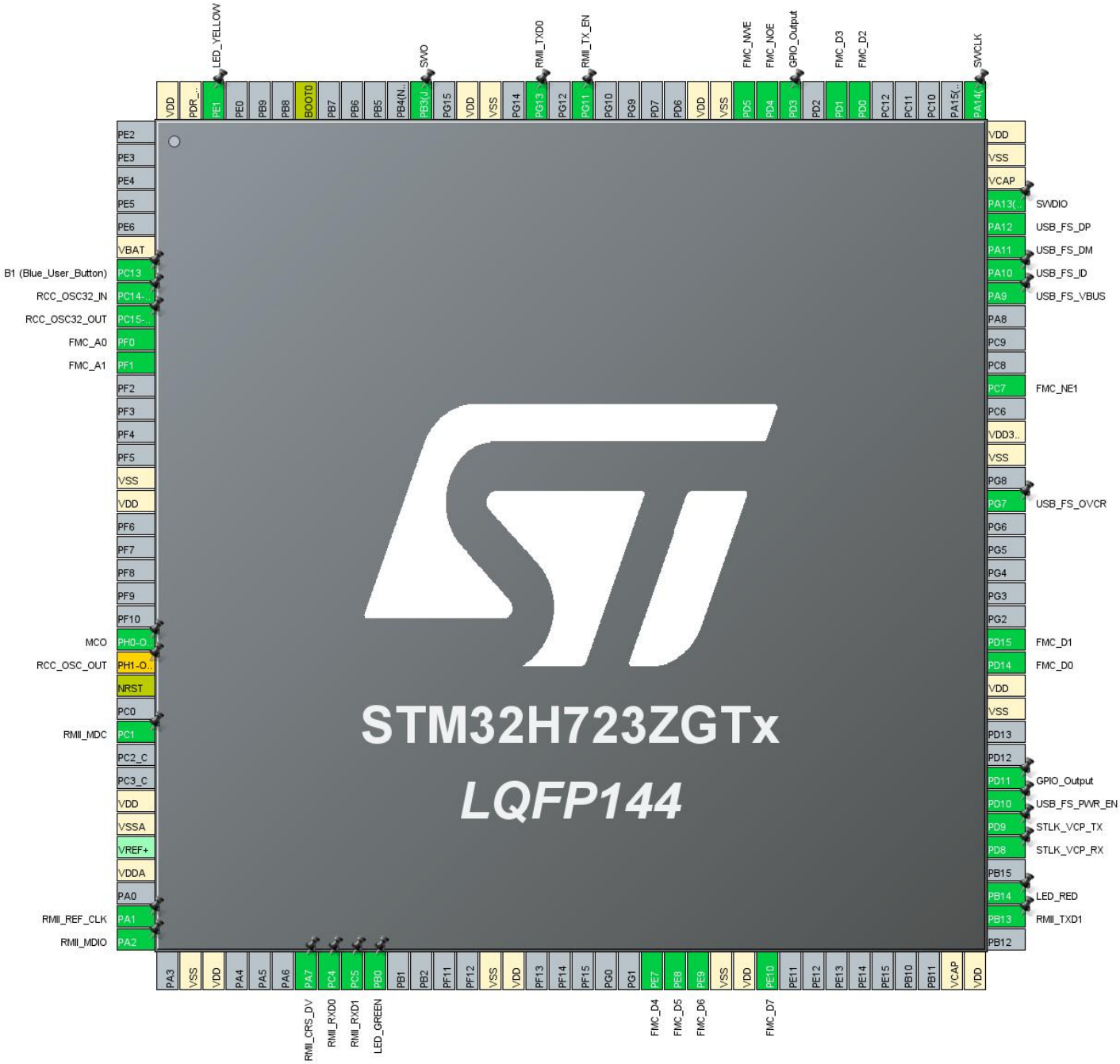
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H723/733
MCU name	STM32H723ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



3. Pins Configuration

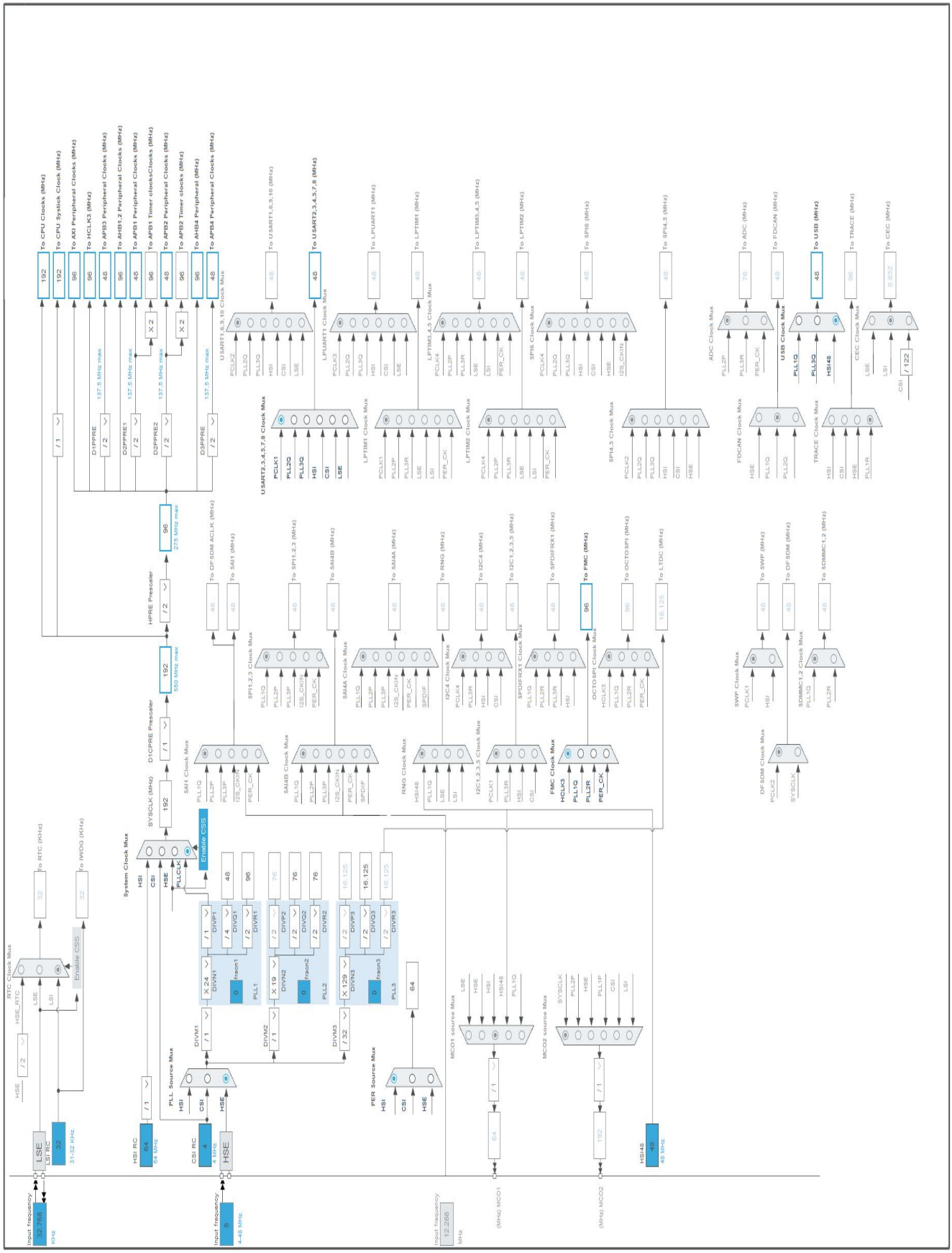
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 (Blue_User_Button)
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
16	VSS	Power		
17	VDD	Power		
23	PH0-OSC_IN	I/O	RCC_OSC_IN	MCO
24	PH1-OSC_OUT **	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	RMII_MDC
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	RMII_REF_CLK
36	PA2	I/O	ETH_MDIO	RMII_MDIO
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	RMII_CRS_DV
44	PC4	I/O	ETH_RXD0	RMII_RXD0
45	PC5	I/O	ETH_RXD1	RMII_RXD1
46	PB0 *	I/O	GPIO_Output	LED_GREEN
51	VSS	Power		
52	VDD	Power		
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
71	VCAP	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	RMII_TXD1
75	PB14 *	I/O	GPIO_Output	LED_RED
77	PD8	I/O	USART3_TX	STLK_VCP_RX

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
78	PD9	I/O	USART3_RX	STLK_VCP_TX
79	PD10 *	I/O	GPIO_Output	USB_FS_PWR_EN
80	PD11 *	I/O	GPIO_Output	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
92	PG7	I/O	GPIO_EXTI7	USB_FS_OVCR
94	VSS	Power		
95	VDD33USB	Power		
97	PC7	I/O	FMC_NE1	
101	PA9	I/O	USB_OTG_HS_VBUS	USB_FS_VBUS
102	PA10	I/O	USB_OTG_HS_ID	USB_FS_ID
103	PA11	I/O	USB_OTG_HS_DM	USB_FS_DM
104	PA12	I/O	USB_OTG_HS_DP	USB_FS_DP
105	PA13(JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	SWDIO
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14(JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	SWCLK
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
117	PD3 *	I/O	GPIO_Output	
118	PD4	I/O	FMC_NOE	
119	PD5	I/O	FMC_NWE	
120	VSS	Power		
121	VDD	Power		
126	PG11	I/O	ETH_TX_EN	RMII_TX_EN
128	PG13	I/O	ETH_TXD0	RMII_TXD0
130	VSS	Power		
131	VDD	Power		
133	PB3(JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	SWO
138	BOOT0	Boot		
142	PE1 *	I/O	GPIO_Output	LED_YELLOW
143	PDR_ON	Power		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm_W6100_bus
Project Folder	D:\wiznet\Teddy\Workspace\2021\06_TestAutomation\02_CODE\01_BusTest\ST
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ETH_Init	ETH
4	MX_USART3_UART_Init	USART3
5	MX_USB_OTG_HS_USB_Init	USB_OTG_HS
6	MX_FMC_Init	FMC
7	MX_DMA2D_Init	DMA2D

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H723/733
MCU	STM32H723ZGTx
Datasheet	DS13313_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

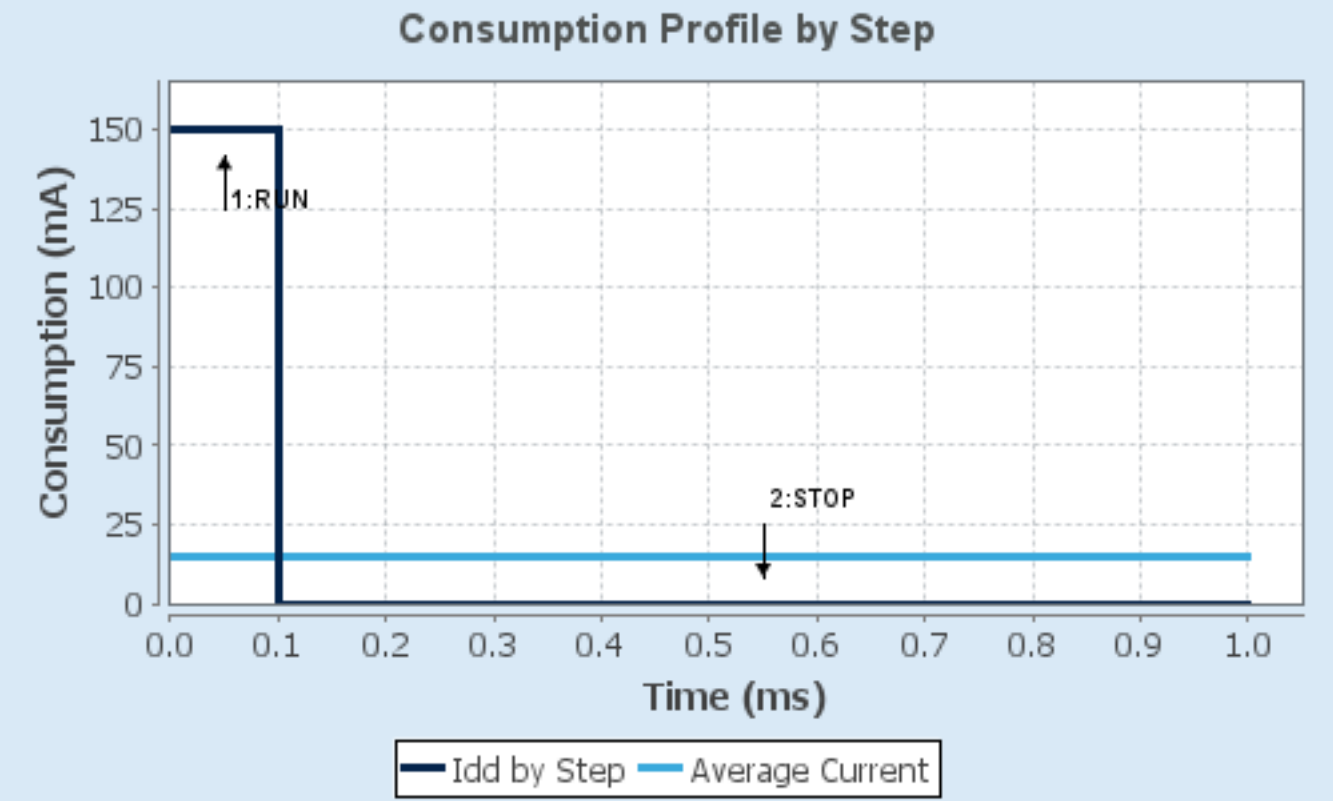
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0/Boost	SVOS5: System-Scale5
D1 Mode	DRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	SRAM1/FlashMode-ON/Cache	NA
CPU Frequency	550 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL_CLOCKS_OFF
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	150 mA	94.5 µA
Duration	0.1 ms	0.9 ms
DMIPS	1177.0	0.0
Ta Max	105.2	124.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	15.09 mA
Battery Life	1 day, 17 hours	Average DMIPS	1177.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. DEBUG

Debug: Trace Asynchronous Sw

7.2. DMA2D

mode: Activated

7.2.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)
DMA2D Chroma Sub-Sampling Mode	No chroma sub-sampling 4:4:4

7.3. ETH

Mode: RMII

7.3.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.4. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: NOR Flash

Address: 2 bits

Data: 8 bits

7.4.1. NOR/PSRAM 1:

NOR/PSRAM control:

Memory type	NOR Flash
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Write FIFO	Enabled
Extended mode	Disabled

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**10 ***
Data setup time in HCLK clock cycles	**26 ***
Bus turn around time in HCLK clock cycles	**0 ***

7.4.2. Bank Mapping:

Mapping parameters:

FMC bank mapping	Default mapping

7.5. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 2

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16

HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	1 WS (2 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range

7.6. SYS

Timebase Source: SysTick

7.7. USART3

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.8. USB_OTG_HS

Internal FS Phy: OTG/Dual_Role_Device

Activate_VBUS: Activate-VBUS

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DEBUG	PA13(JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14(JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PB3(JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	SWO
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_MDC
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_REF_CLK
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_MDIO
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_CRS_DV
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_RXD0
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_RXD1
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TXD1
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TX_EN
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	RMII_TXD0
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLK_VCP_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLK_VCP_TX
USB_OTG_	PA9	USB_OTG_HS_	Input mode	No pull-up and no pull-down	n/a	USB_FS_VBUS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
HS		VBUS				
	PA10	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_FS_ID
	PA11	USB_OTG_HS_DM	n/a	n/a	n/a	USB_FS_DM
	PA12	USB_OTG_HS_DP	n/a	n/a	n/a	USB_FS_DP
Single Mapped Signals	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 (Blue_User_Button)
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_FS_PWR_EN
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_FS_OVCR
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_YELLOW

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART3 global interrupt	true	0	0
PVD/AVD through EXTI Line detection Interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line[9:5] interrupts	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FPU global interrupt	unused		
DMA2D global interrupt	unused		
HSEM1 global interrupt	unused		

8.5.2. NVIC Code generation

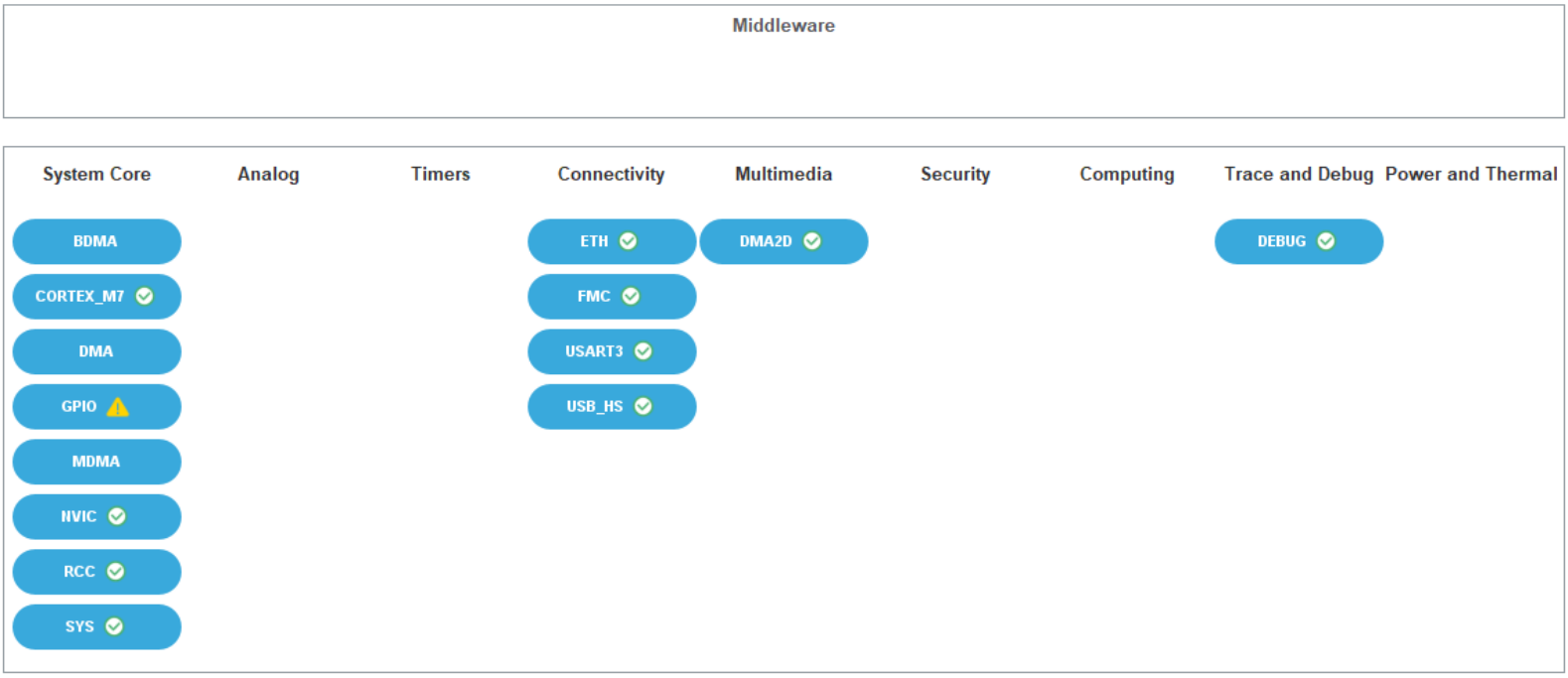
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USART3 global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00701028.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00603761.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00625312.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00663674.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf