

Start of File

LVDS Lane 1	RX0 (I) Sample 1
	RX0 (I) Sample 2
LVDS Lane 2	RX0 (Q) Sample 1
	RX0 (Q) Sample 2
.	.
.	.
LVDS Lane 1	RX0 (I) Sample N-1
	RX0 (I) Sample N
LVDS Lane 2	RX0 (Q) Sample N-1
	RX0 (Q) Sample N
.	.
.	.
.	.
LVDS Lane 1	RX3 (I) Sample 1
	RX3 (I) Sample 2
LVDS Lane 2	RX3 (Q) Sample 1
	RX3 (Q) Sample 2
.	.
.	.
.	.
LVDS Lane 1	RX3 (I) Sample N-1
	RX3 (I) Sample N
LVDS Lane 2	RX3 (Q) Sample N-1
	RX3 (Q) Sample N

1st Chip

N ADC Samples Per Chirp



LVDS Lane 1	RX0 (I) Sample 1
	RX0 (I) Sample 2
LVDS Lane 2	RX0 (Q) Sample 1
	RX0 (Q) Sample 2
.	.
.	.
.	.
LVDS Lane 1	RX0 (I) Sample N-1
	RX0 (I) Sample N
LVDS Lane 2	RX0 (Q) Sample N-1
	RX0 (Q) Sample N
.	.
.	.
.	.
LVDS Lane 1	RX3 (I) Sample 1
	RX3 (I) Sample 2
LVDS Lane 2	RX3 (Q) Sample 1
	RX3 (Q) Sample 2
.	.
.	.
.	.
LVDS Lane 1	RX3 (I) Sample N-1
	RX3 (I) Sample N
LVDS Lane 2	RX3 (Q) Sample N-1
	RX3 (Q) Sample N

End of File

Mth Chip

N ADC Samples Per Chirp