

# STM32 CubeMX

## 1. Description

### 1.1. Project

Project Name	GLASSALT_SRAM
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	01/21/2026

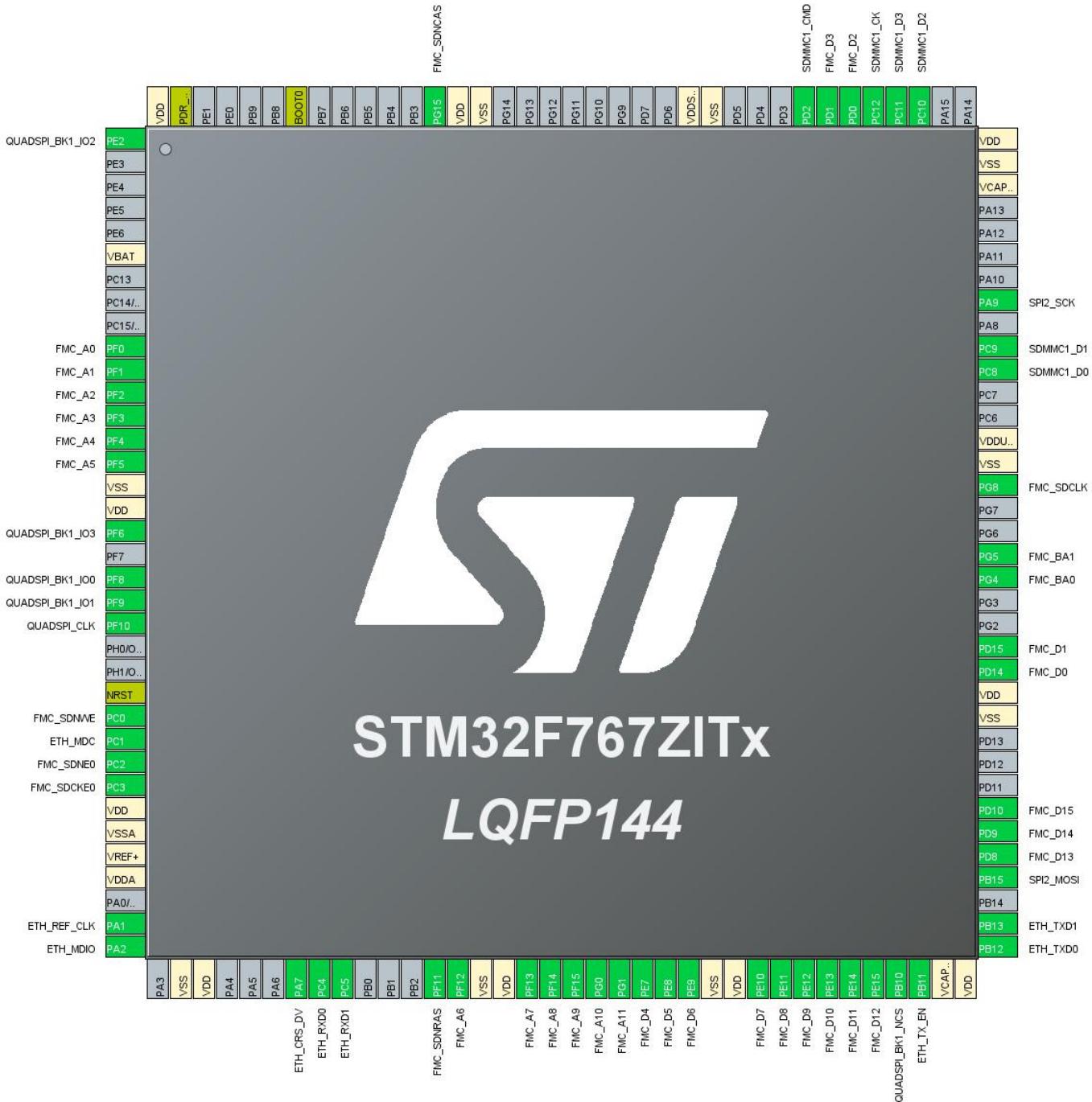
### 1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	Arm Cortex-M7
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## **2. Pinout Configuration**



### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
6	VBAT	Power		
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
20	PF8	I/O	QUADSPI_BK1_IO0	
21	PF9	I/O	QUADSPI_BK1_IO1	
22	PF10	I/O	QUADSPI_CLK	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1	I/O	ETH_MDC	
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	

GLASSALT\_SRAM Project  
Configuration Report

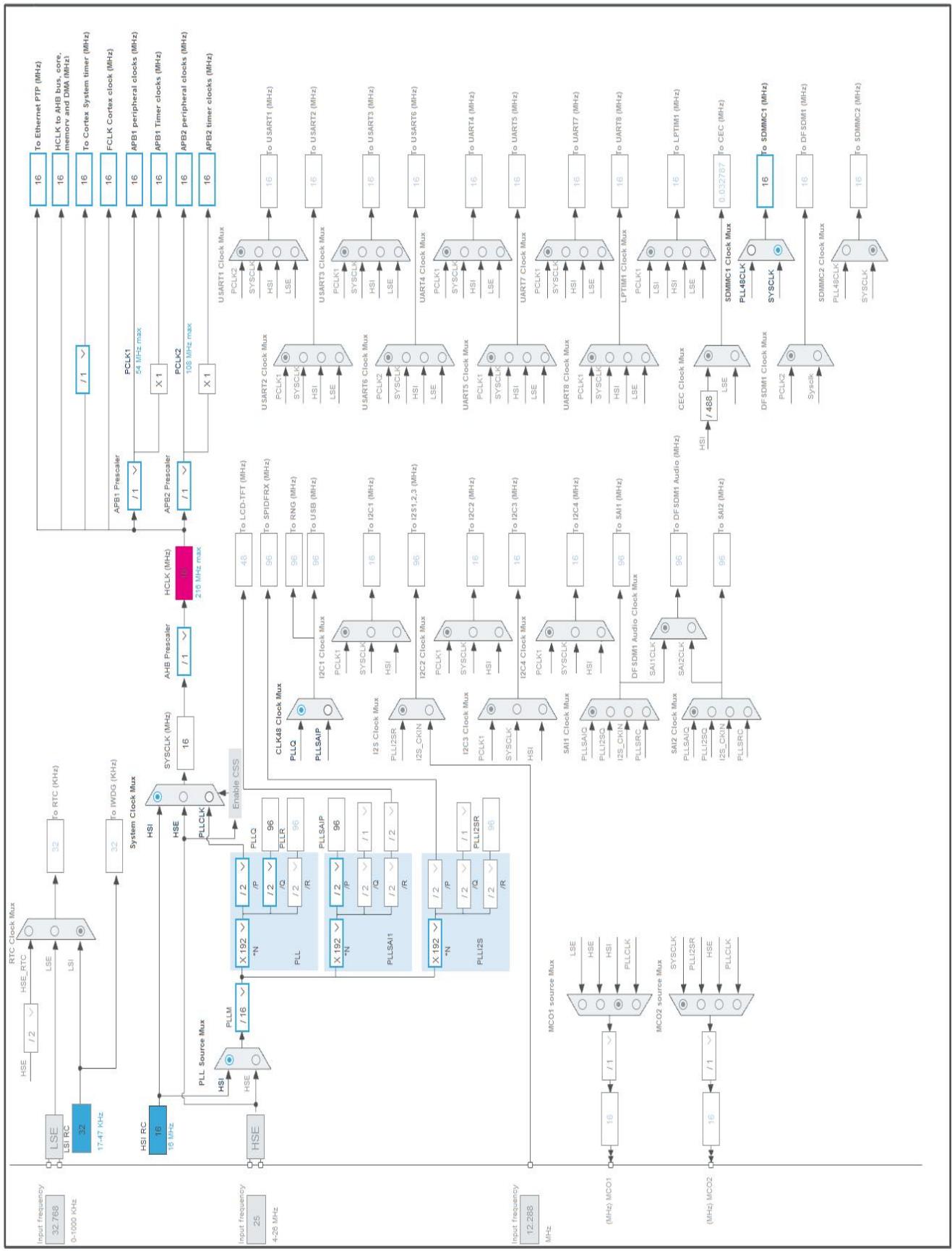
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Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	QUADSPI_BK1_NCS	
70	PB11	I/O	ETH_TX_EN	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	ETH_TXD1	
76	PB15	I/O	SPI2_MOSI	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDDUSB	Power		
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
101	PA9	I/O	SPI2_SCK	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		

GLASSALT\_SRAM Project  
Configuration Report

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2	I/O	SDMMC1_CMD	
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

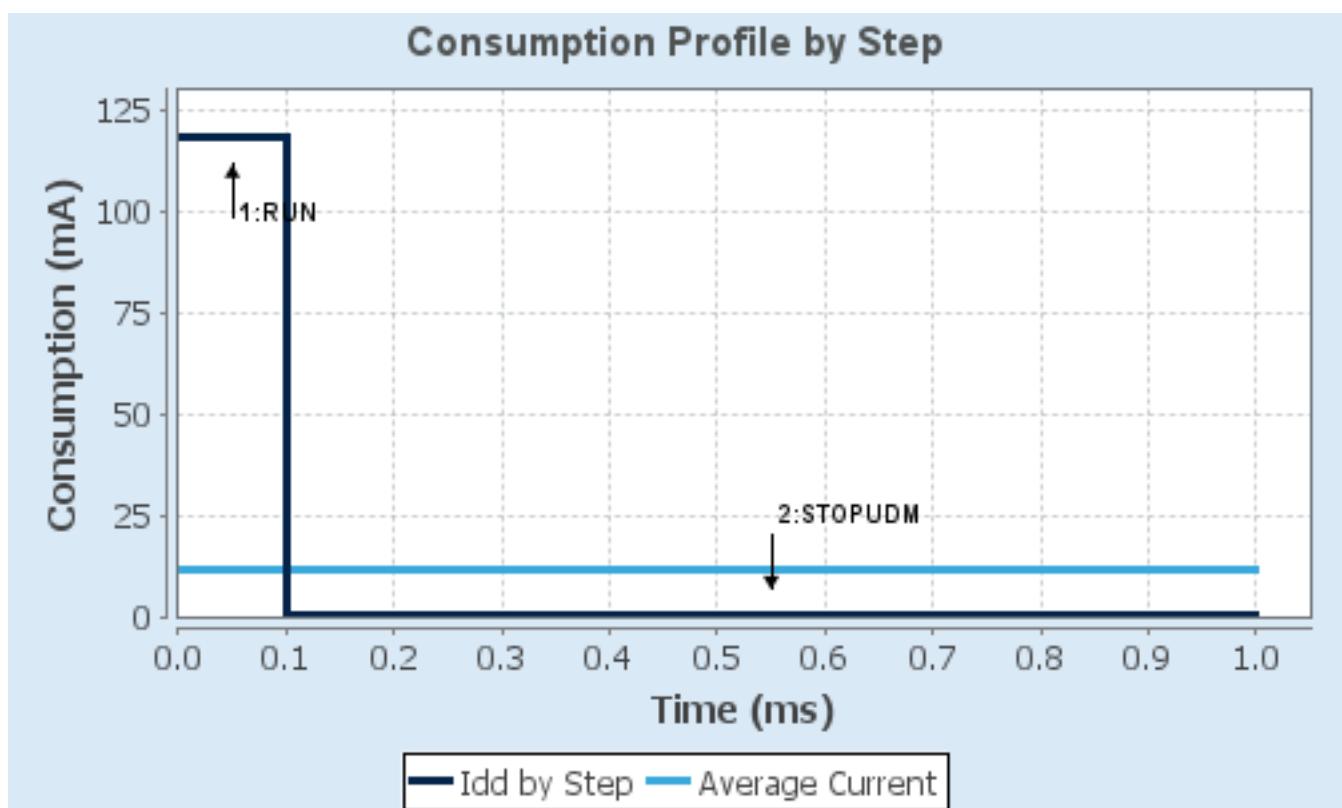
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP UDM (Under Drive)
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	ICTM FLASH-SingleBank REGON	n/a
<b>CPU Frequency</b>	216 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	118 mA	130 µA
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	462.0	0.0
<b>T<sub>a</sub> Max</b>	89.42	104.98
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

#### 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	GLASSALT_SRAM
Project Folder	C:\Users\dteichman.LOCAL\STM32CubeIDE\workspace_2.0.0\GLASSALT_SRA
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c./h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_FMC_Init	FMC
5	MX_ETH_Init	ETH
6	MX_SDMMC1_SD_Init	SDMMC1
7	MX_DMA2D_Init	DMA2D
8	MX_QUADSPI_Init	QUADSPI
9	MX_SPI2_Init	SPI2



### **3. Peripherals and Middlewares Configuration**

#### **3.1. CORTEX\_M7**

##### 3.1.1. Parameter Settings:

###### **Speculation default mode Settings:**

Speculation default mode **Enabled \***

###### **Cortex Interface Settings:**

Flash Interface	AXI Interface
ART ACCELERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

###### **Cortex Memory Protection Unit Control Settings:**

MPU Control Mode **Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers**

###### **Cortex Memory Protection Unit Region 0 Settings:**

MPU Region	Enabled
MPU Region Base Address	<b>0x0 *</b>
MPU Region Size	4GB
MPU SubRegion Disable	<b>0x87 *</b>
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	DISABLE
MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

###### **Cortex Memory Protection Unit Region 1 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 2 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 3 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 4 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 5 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 6 Settings:**

MPU Region **Disabled**

###### **Cortex Memory Protection Unit Region 7 Settings:**

MPU Region                          Disabled

### 3.2. DMA2D

**mode: Activated**

#### 3.2.1. Parameter Settings:

##### **Basic Parameters:**

Transfer Mode                          Memory to Memory

Color Mode                              **ARGB4444 \***

Output Offset                        0

##### **Foreground layer Configuration:**

DMA2D Input Color Mode            ARGB4444

DMA2D ALPHA MODE                 No modification of the alpha channel value

Input Alpha                            0

Input Offset                        0

DMA2D ALPHA Inversion            Regular Alpha

DMA2D Red and Blue swap        Regular mode (RGB or ARGB)

### 3.3. ETH

**Mode: RMII**

#### 3.3.1. Parameter Settings:

##### **General : Ethernet Configuration:**

Ethernet MAC Address               00:80:E1:00:00:00

Tx Descriptor Length                4

First Tx Descriptor Address       **0x2007c0a0 \***

Rx Descriptor Length                4

First Rx Descriptor Address       **0x2007c000 \***

Rx Buffers Length                   1524

Rx Mode                              Polling Mode

### 3.4. FMC

#### SDRAM 1

**Clock and chip enable: SDCKE0+SDNE0**

**Internal bank number: 4 banks**

**Address: 12 bits**

**Data: 16 bits**

#### 3.4.1. SDRAM 1:

##### **SDRAM control:**

Bank	SDRAM bank 1
Number of column address bits	<b>9 bits *</b>
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	<b>2 HCLK clock cycles *</b>
SDRAM common burst read	<b>Enabled *</b>
SDRAM common read pipe delay	<b>1 HCLK clock cycle *</b>

##### **SDRAM timing in memory clock cycles:**

Load mode register to active delay	<b>2 *</b>
Exit self-refresh delay	<b>8 *</b>
Self-refresh time	<b>5 *</b>
SDRAM common row cycle delay	<b>7 *</b>
Write recovery time	<b>2 *</b>
SDRAM common row precharge delay	<b>2 *</b>
Row to column delay	16

## **3.5. QUADSPI**

### **QuadSPI Mode: Bank1 with Quad SPI Lines**

#### 3.5.1. Parameter Settings:

##### **General Parameters:**

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

## 3.6. RCC

### 3.6.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

#### **RCC Parameters:**

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

#### **Power Parameters:**

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

## 3.7. SDMMC1

### **Mode: SD 4 bits Wide bus**

### 3.7.1. Parameter Settings:

#### **SDMMC parameters:**

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCCLK clock divide factor	0

## 3.8. SPI2

### **Mode: Transmit Only Master**

### 3.8.1. Parameter Settings:

#### **Basic Parameters:**

Frame Format	Motorola
Data Size	<b>16 Bits *</b>
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	<b>8 *</b>
Baud Rate	<b>2.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

### 3.9. SYS

**Timebase Source: SysTick**

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

GLASSALT\_SRAM Project  
Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
QUADSPI	PE2	QUADSPI_BK1_I_O2	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF6	QUADSPI_BK1_I_O3	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF8	QUADSPI_BK1_I_O0	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF9	QUADSPI_BK1_I_O1	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PB10	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PA9	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	

## 4.2. DMA configuration

DMA request	Stream	Direction	Priority
SDMMC1_RX	DMA2_Stream3	Peripheral To Memory	Low
SDMMC1_TX	DMA2_Stream6	Memory To Peripheral	Low

### SDMMC1\_RX: DMA2\_Stream3 DMA request Settings:

Mode: **Peripheral Flow Control \***

Use fifo: **Enable \***

FIFO Threshold: Full

Peripheral Increment: Disable

Memory Increment: **Enable \***

Peripheral Data Width: **Word \***

Memory Data Width: Word

Peripheral Burst Size: **4 Increment \***

Memory Burst Size: 4 Increment

### SDMMC1\_TX: DMA2\_Stream6 DMA request Settings:

Mode: **Peripheral Flow Control \***

Use fifo: **Enable \***

FIFO Threshold: Full

Peripheral Increment: Disable

Memory Increment: **Enable \***

Peripheral Data Width: **Word \***

Memory Data Width: Word

Peripheral Burst Size: **4 Increment \***

Memory Burst Size: 4 Increment

## 4.3. NVIC configuration

### 4.3.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream6 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
SPI2 global interrupt		unused	
FMC global interrupt		unused	
SDMMC1 global interrupt		unused	
Ethernet global interrupt		unused	
Ethernet wake-up interrupt through EXTI line 19		unused	
FPU global interrupt		unused	
DMA2D global interrupt		unused	
QUADSPI global interrupt		unused	

### 4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

##### Middleware

###### System Core

###### Analog

###### Timers

###### Connectivity

###### Multimedia

###### Security

###### Computing

CORTEX\_M7 ✓

DMA ✓

GPIO ✓

NVIC ✓

RCC ✓

SYS ✓

ETH ✓

DMA2D ✓

FMC ✓

QUADSPI ✓

SDMMC1 ✓

SPI2 ✓

## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip</a>
System View	<a href="https://www.st.com/resource/en/svd/stm32f7-svd.zip">https://www.st.com/resource/en/svd/stm32f7-svd.zip</a>
Description	
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf">https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/expansion-boards-for-intelligent-power-switches.pdf">https://www.st.com/resource/en/brochure/expansion-boards-for-intelligent-power-switches.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
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