

STM32 CubeMX

1. Description

1.1. Project

Project Name	GLASSALT_SRAM
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	01/26/2026

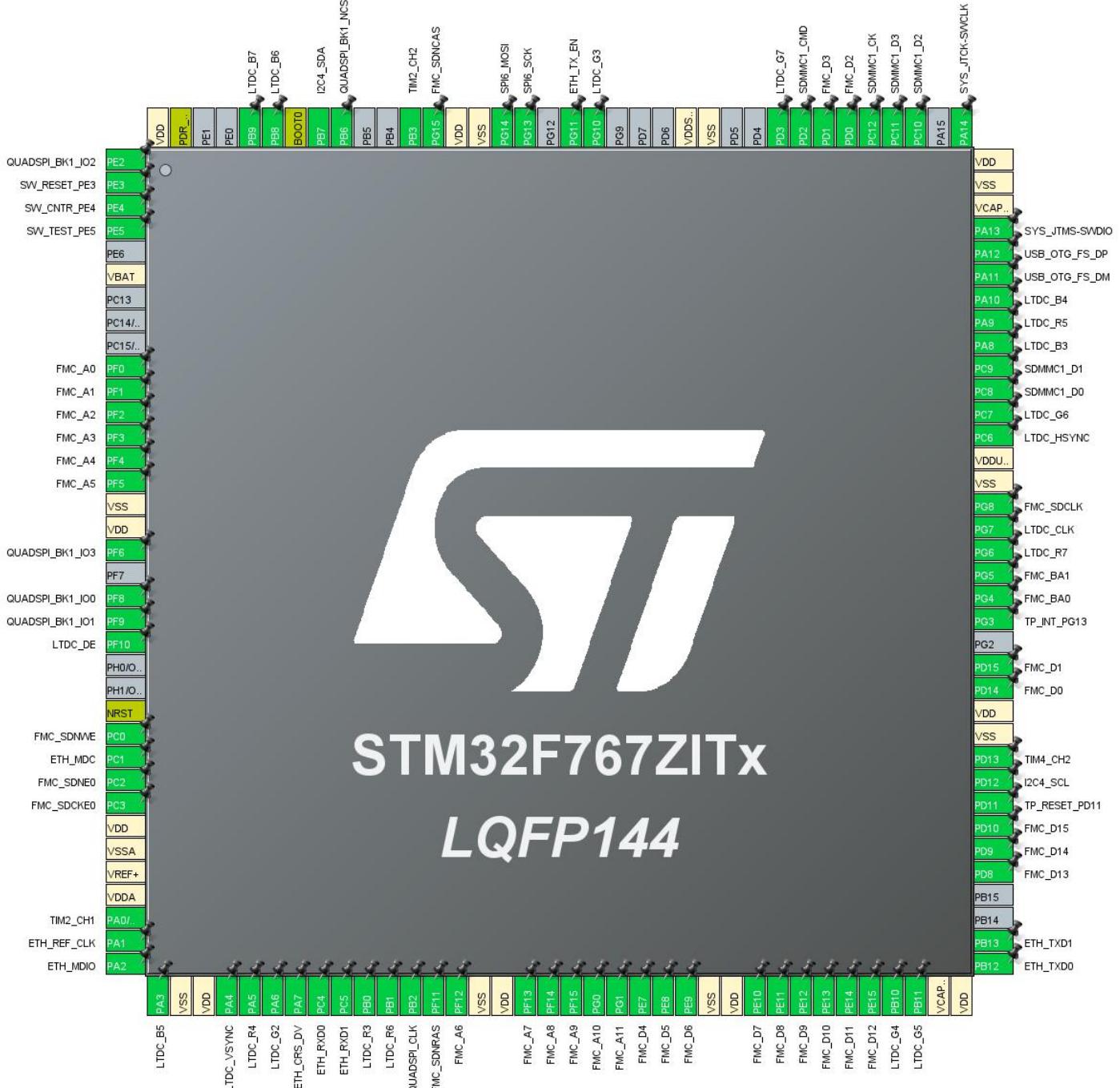
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
2	PE3 *	I/O	GPIO_Input	SW_RESET_PE3
3	PE4 *	I/O	GPIO_Input	SW_CNTR_PE4
4	PE5 *	I/O	GPIO_Input	SW_TEST_PE5
6	VBAT	Power		
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
20	PF8	I/O	QUADSPI_BK1_IO0	
21	PF9	I/O	QUADSPI_BK1_IO1	
22	PF10	I/O	LTDC_DE	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1	I/O	ETH_MDC	
28	PC2	I/O	FMC_SDNE0	
29	PC3	I/O	FMC_SDCKE0	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM2_CH1	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
37	PA3	I/O	LTDC_B5	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	
41	PA5	I/O	LTDC_R4	
42	PA6	I/O	LTDC_G2	
43	PA7	I/O	ETH_CRS_DV	

GLASSALT_SRAM Project
Configuration Report

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
46	PB0	I/O	LTDC_R3	
47	PB1	I/O	LTDC_R6	
48	PB2	I/O	QUADSPI_CLK	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	LTDC_G4	
70	PB11	I/O	LTDC_G5	
71	VCAP_1	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	ETH_TXD1	
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
80	PD11 *	I/O	GPIO_Output	TP_RESET_PD11
81	PD12	I/O	I2C4_SCL	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		

GLASSALT_SRAM Project
Configuration Report

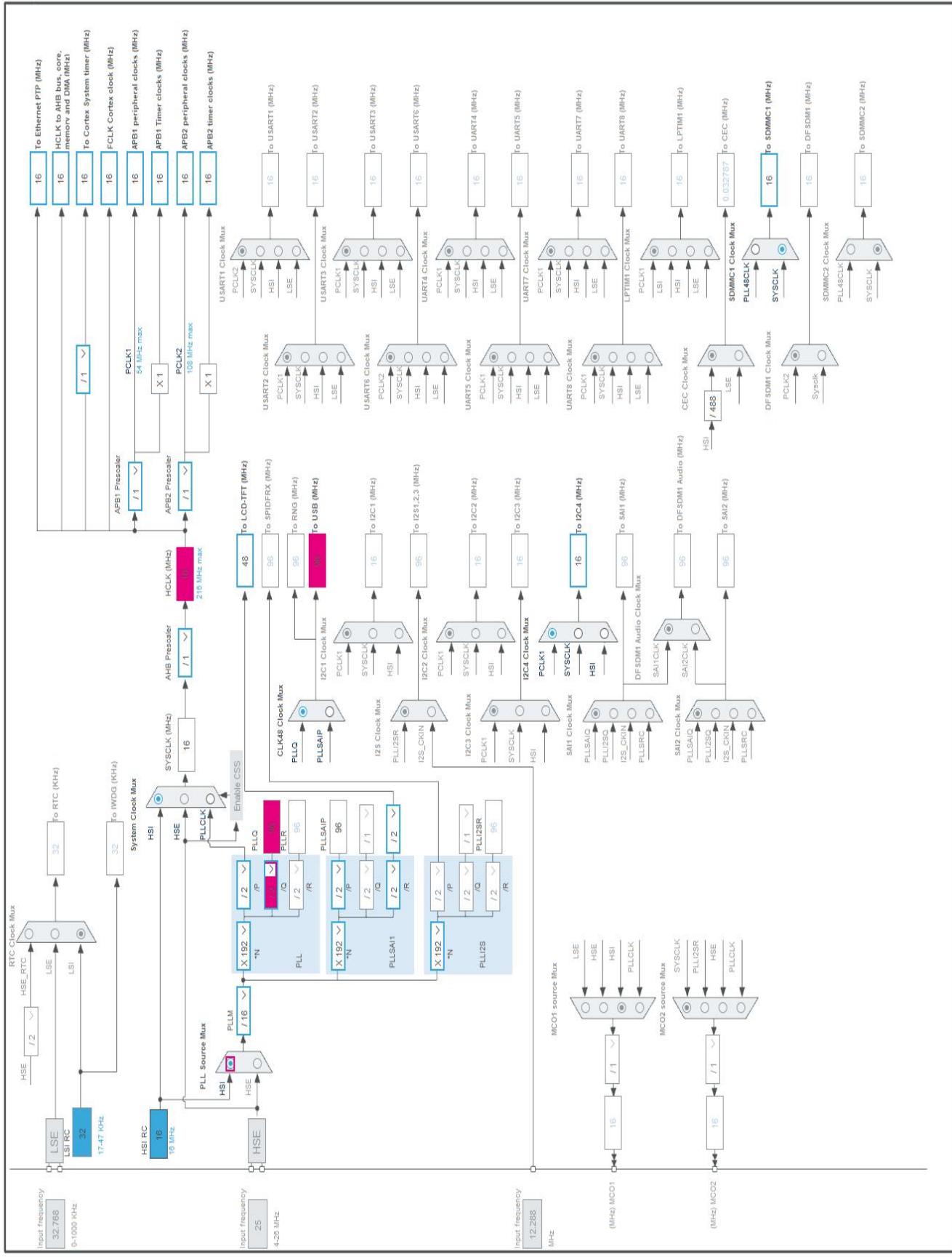
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
88	PG3	I/O	GPIO_EXTI3	TP_INT_PG13
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6	I/O	LTDC_R7	
92	PG7	I/O	LTDC_CLK	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	LTDC_HSYNC	
97	PC7	I/O	LTDC_G6	
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
100	PA8	I/O	LTDC_B3	
101	PA9	I/O	LTDC_R5	
102	PA10	I/O	LTDC_B4	
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
116	PD2	I/O	SDMMC1_CMD	
117	PD3	I/O	LTDC_G7	
120	VSS	Power		
121	VDDSDMMC	Power		
125	PG10	I/O	LTDC_G3	
126	PG11	I/O	ETH_TX_EN	
128	PG13	I/O	SPI6_SCK	
129	PG14	I/O	SPI6_MOSI	
130	VSS	Power		
131	VDD	Power		

GLASSALT_SRAM Project
Configuration Report

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
132	PG15	I/O	FMC_SDNCAS	
133	PB3	I/O	TIM2_CH2	
136	PB6	I/O	QUADSPI_BK1_NCS	
137	PB7	I/O	I2C4_SDA	
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	
140	PB9	I/O	LTDC_B7	
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

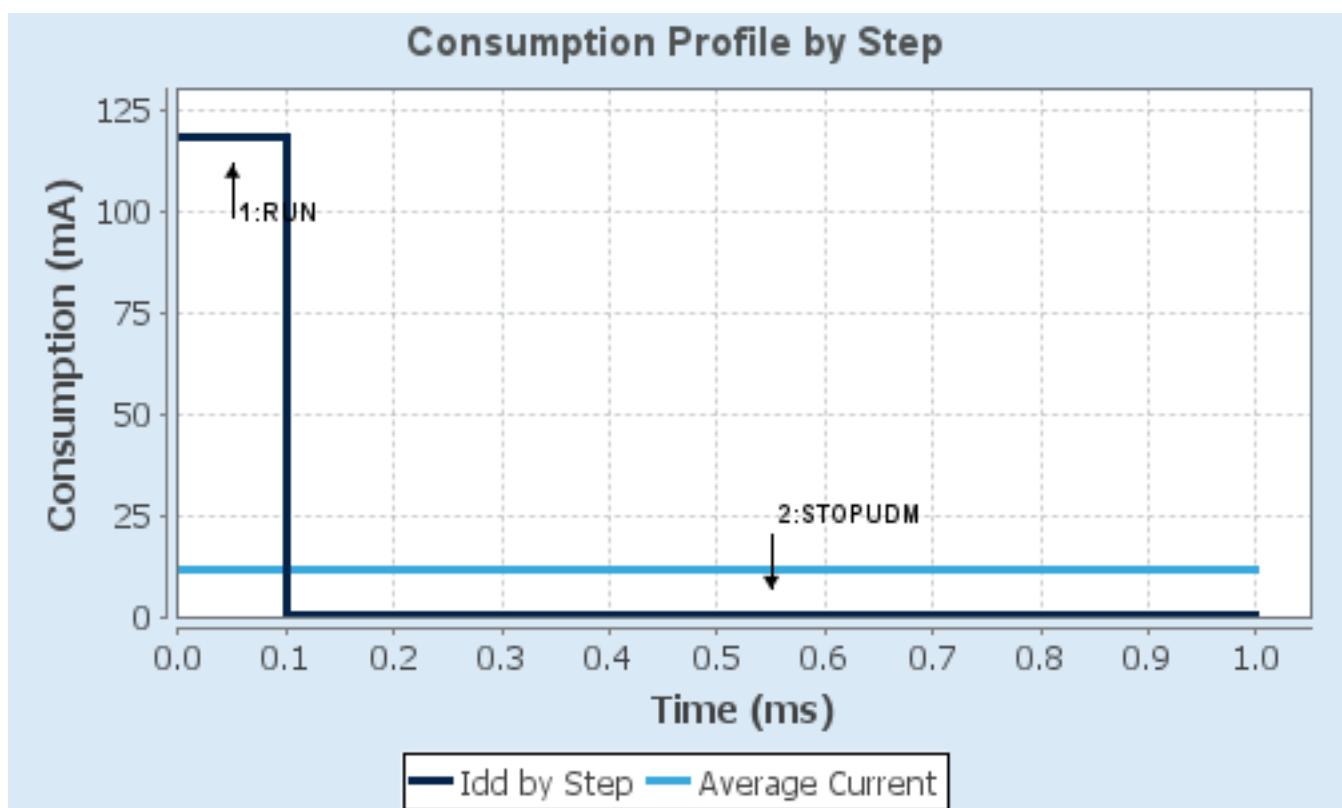
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
T_a Max	89.42	104.98
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	GLASSALT_SRAM
Project Folder	C:\Users\dteichman.LOCAL\STM32CubeIDE\workspace_2.0.0\GLASSALT_SRA
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.4
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c./h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_FMC_Init	FMC
5	MX_ETH_Init	ETH
6	MX_SDMMC1_SD_Init	SDMMC1
7	MX_DMA2D_Init	DMA2D
8	MX_QUADSPI_Init	QUADSPI
9	MX_LTDC_Init	LTDC
10	MX_TIM2_Init	TIM2
11	MX_TIM4_Init	TIM4

GLASSALT_SRAM Project

Configuration Report

Rank	Function Name	Peripheral Instance Name
12	MX_I2C4_Init	I2C4
13	MX_SPI6_Init	SPI6
14	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS

3. Peripherals and Middlewares Configuration

3.1. CORTEX_M7

3.1.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode **Enabled ***

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCELERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode **Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers**

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled
MPU Region Base Address	0x0 *
MPU Region Size	4GB
MPU SubRegion Disable	0x87 *
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	DISABLE
MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 2 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 3 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 4 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 5 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 6 Settings:

MPU Region **Disabled**

Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

3.2. DMA2D

mode: Activated

3.2.1. Parameter Settings:

Basic Parameters:

Transfer Mode Memory to Memory

Color Mode **ARGB4444 ***

Output Offset 0

Foreground layer Configuration:

DMA2D Input Color Mode ARGB4444

DMA2D ALPHA MODE No modification of the alpha channel value

Input Alpha 0

Input Offset 0

DMA2D ALPHA Inversion Regular Alpha

DMA2D Red and Blue swap Regular mode (RGB or ARGB)

3.3. ETH

Mode: RMII

3.3.1. Parameter Settings:

General : Ethernet Configuration:

Ethernet MAC Address 00:80:E1:00:00:00

Tx Descriptor Length 4

First Tx Descriptor Address **0x2007c0a0 ***

Rx Descriptor Length 4

First Rx Descriptor Address **0x2007c000 ***

Rx Buffers Length 1524

Rx Mode Polling Mode

3.4. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

3.4.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	9 bits *
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	2 HCLK clock cycles *
SDRAM common burst read	Enabled *
SDRAM common read pipe delay	1 HCLK clock cycle *

SDRAM timing in memory clock cycles:

Load mode register to active delay	2 *
Exit self-refresh delay	8 *
Self-refresh time	5 *
SDRAM common row cycle delay	7 *
Write recovery time	2 *
SDRAM common row precharge delay	2 *
Row to column delay	16

3.5. I2C4

I2C: I2C

3.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x00303D5B

Slave Features:

Clock No Stretch Mode	Disabled
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General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

3.6. LTDC

Display Type: RGB565 (16 bits)

3.6.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

Layer Default Color:

Red	0
Green	0
Blue	0

3.6.2. Layer Settings:

Layer Default Color:

Layer 0 - Alpha	0
Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Alpha	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

Number of Layers:

Number of Layers	2 layers
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3.7. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

3.7.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

3.8. RCC

3.8.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

3.9. SDMMC1

Mode: SD 4 bits Wide bus

3.9.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
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SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

3.10. SPI6

Mode: Transmit Only Master

3.10.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	8.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

3.11. SYS

Debug: Serial Wire

Timebase Source: SysTick

3.12. TIM2

Combined Channels: Encoder Mode

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
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_____ Parameters for Channel 1 _____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

_____ Parameters for Channel 2 _____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.13. TIM4

Channel2: PWM Generation CH2

3.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.14. USB_OTG_FS

Mode: Device_Only

3.14.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC2	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_I_O2	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF6	QUADSPI_BK1_I_O3	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PF8	QUADSPI_BK1_I_O0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

GLASSALT_SRAM Project
Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF9	QUADSPI_BK1_I_O1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI6	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PE3	GPIO_Input	Input mode	Pull-up *	n/a	SW_RESET_PE3
	PE4	GPIO_Input	Input mode	Pull-up *	n/a	SW_CNTR_PE4
	PE5	GPIO_Input	Input mode	Pull-up *	n/a	SW_TEST_PE5
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TP_RESET_PD11
	PG3	GPIO_EXTI3	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	TP_INT_PG13

4.2. DMA configuration

DMA request	Stream	Direction	Priority
SDMMC1_RX	DMA2_Stream3	Peripheral To Memory	Low
SDMMC1_TX	DMA2_Stream6	Memory To Peripheral	Low

SDMMC1_RX: DMA2_Stream3 DMA request Settings:

Mode: **Peripheral Flow Control ***

Use fifo: **Enable ***

FIFO Threshold: Full

Peripheral Increment: Disable

Memory Increment: **Enable ***

Peripheral Data Width: **Word ***

Memory Data Width: Word

Peripheral Burst Size: **4 Increment ***

Memory Burst Size: 4 Increment

SDMMC1_TX: DMA2_Stream6 DMA request Settings:

Mode: **Peripheral Flow Control ***

Use fifo: **Enable ***

FIFO Threshold: Full

Peripheral Increment: Disable

Memory Increment: **Enable ***

Peripheral Data Width: **Word ***

Memory Data Width: Word

Peripheral Burst Size: **4 Increment ***

Memory Burst Size: 4 Increment

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenemption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA2 stream3 global interrupt	true	0	0
DMA2 stream6 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
EXTI line3 interrupt		unused	
TIM2 global interrupt		unused	
TIM4 global interrupt		unused	
FMC global interrupt		unused	
SDMMC1 global interrupt		unused	
Ethernet global interrupt		unused	
Ethernet wake-up interrupt through EXTI line 19		unused	
USB On The Go FS global interrupt		unused	
FPU global interrupt		unused	
SPI6 global interrupt		unused	
LTDC global interrupt		unused	
LTDC global error interrupt		unused	
DMA2D global interrupt		unused	
QUADSPI global interrupt		unused	
I2C4 event interrupt		unused	
I2C4 error interrupt		unused	

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

GLASSALT_SRAM Project
Configuration Report

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA2 stream3 global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Security

Computing

CORTEX_M7 ✓

DMA ✓

GPIO ✓

NVIC ✓

RCC ✓

SYS ✓

TIM2 ✓

TIM4 ✓

ETH ✓

FMC ✓

I2C4 ✓

QUADSPI ✓

SDMMC1 ✓

SPI4 ✓

DMA2D ✓

LTDC ✓

USB_FS ✓

6. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip
System View	https://www.st.com/resource/en/svd/stm32f7-svd.zip
Description	
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Brochures	https://www.st.com/resource/en/brochure/expansion-boards-for-intelligent-power-switches.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Security Bulletin	https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
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for related Tools

& Software

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Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1206-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-qfp-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1207-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-so-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1208-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-tssop-and-ssop-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um2318-stm32f7-series-safety-manual-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um3251-stm32f7-series-ulcsaiec-607301603351-selftest-library-user-guide-stmicroelectronics.pdf