STUDY ORIENTED PROJECT

Final Report

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Acknowledgement:

I sincerely thank Dr Satyendra Kumar Mourya for giving me the opportunity to explore the field of Electronic Devices through this project. He guided me throughout the course of the project and helped me understand how to practically apply the knowledge I learnt from the Electronic Devices (ED) course.

This project, although small, has helped me understand the vastness of the field and its various applications. I hope to continue exploring the field through further projects and courses.

Motivation:

I've always been interested in the field of semiconductors. I wish to investigate the effect of different materials on the working of devices like MOSFETS and thus, improve their efficiency. I feel that semiconductors are one of the more fundamental components of electronics and nothing can function without them. The belief that I would be making an impact on the field of electric devices by working on its fundamental unit motivated me to take up this project.

Introduction:

Semiconductors are essential components in electric devices. They have enabled advances in communications, computing, healthcare, military systems, transportation, clean energy, and have countless other applications. Since it has such varied uses, research in the field of semiconductors is of utmost importance and can have far-reaching implications.

Before we talk about the project, it is important to understand the present state of the field and its potential:

1. Current state of art:

At present, Silicon transistors are primarily being used. The two basic types of silicon transistors are MOSFETs and BJTs. However, Silicon devices have certain disadvantages: Electrons aren't as mobile in it as compared to other materials. This reduces the rate of information travel. Modern ICs use CMOS technology to get around this. However, Silicon's electron-hole mobility is so low that manufacturers have to boost it by including Germanium with the Silicon. Another problem Silicon suffers from is that its performance degrades at higher temperature. Modern ICs with billions of transistors generate considerable heat, which is why a lot of time and money goes into cooling them. This severely reduces the efficiency of a device in non-ideal conditions. While Germanium offers some advantages, it will be difficult to realign the market around Germanium given that Silicon has been used for decades now. Instead, the way forward is to improve Silicon by integrating it with other materials.

2. <u>Ongoing research in the field:</u>

Present research centres around determining the viability of certain compound semiconductors like SiC and GaN. They offer certain advantages over Si semiconductors.

<u>SiC:</u>

It is a wide band-gap semiconductor that contains equal parts of Si and C atoms in a hexagonal crystal structure. There are two principal kinds of prototypes: 6H-SiC and 4H-SiC. The 4H-SiC model is more commonly used as it displays equal properties along all directions while 6H-SiC is anisotropic.

Benefits of SiC MOSFETs:

- Can operate at much higher temperature. (Greater than 150 degree Celsius—the maximum temperature at which Si can operate)
- Critical breakdown strength ten times that of Silicon.
- Provide higher current density and switching frequencies.
- High electro-thermal conductivity

<u>GaN-on-Silicon</u>:

Gallium nitride (GaN) is a very hard, mechanically stable wide bandgap semiconductor. With higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance, power devices based on GaN significantly outperform silicon-based devices.

Benefits of GaN MOSFETs:

- Devices made in GaN are hetero devices and base their operation on the two-dimensional electron gas (2DEG) that is formed in the quantum well between the heterojunction interfaces.
- This quantum well provides electrons with a highly conductive channel, allowing high electron mobility.
- The use of GaN transistors supports key RF demands such as high gain, low power consumption, high throughput, and extremely fast switching speeds.
- As an amplifier, it provides a much higher bandwidth.

<u>My contribution:</u>

I focussed on learning ATLAS by designing a Schottky diode and plotting its forward characteristics. I then interpreted the graphs (log and linear) and used it to analyse the device's parameters. I also added an interfacial (SiO_2) layer at the Schottky contact, thus improving its characteristics and dissipating any stray charges.

Software used:

The IDE Silvaco TCAD was used to simulate and analyse the parameters of the Schottky Diode. The ATLAS programming language was used to design the diode. TonyPlot was used to plot all graphs.

Algorithm:

1. Define the x and y coordinates of the meshes to be constructed. Meshes are the basic unit of construction in Atlas and are defined first. The first statement must always be **MESH SPACE.MULT=<value>**
2. Now, we must assign each mesh a material type. We do this using the **region** statement:
   REGION number=<integer> <material type> <position parameters>. Here, I have created four regions, three have the material Silicon and one has the material Silicon Oxide.
3. Next, we specify the electrodes. We do this using the **electr** statement:
   electr NAME=<electrode name> <Position parameters>
4. Now, we need to dope each of these regions:
   a. We dope specific regions using the doping statement:
      DOPING <type> <concentration> <position parameters> <distribution>
   b. Epitaxial doping: In this program, N-type Epitaxial doping has been performed
   c. Guard ring doping: I this program, P-type Guard Ring doping has been carried out
   d. Substrate doping: N+ doping has been carried out

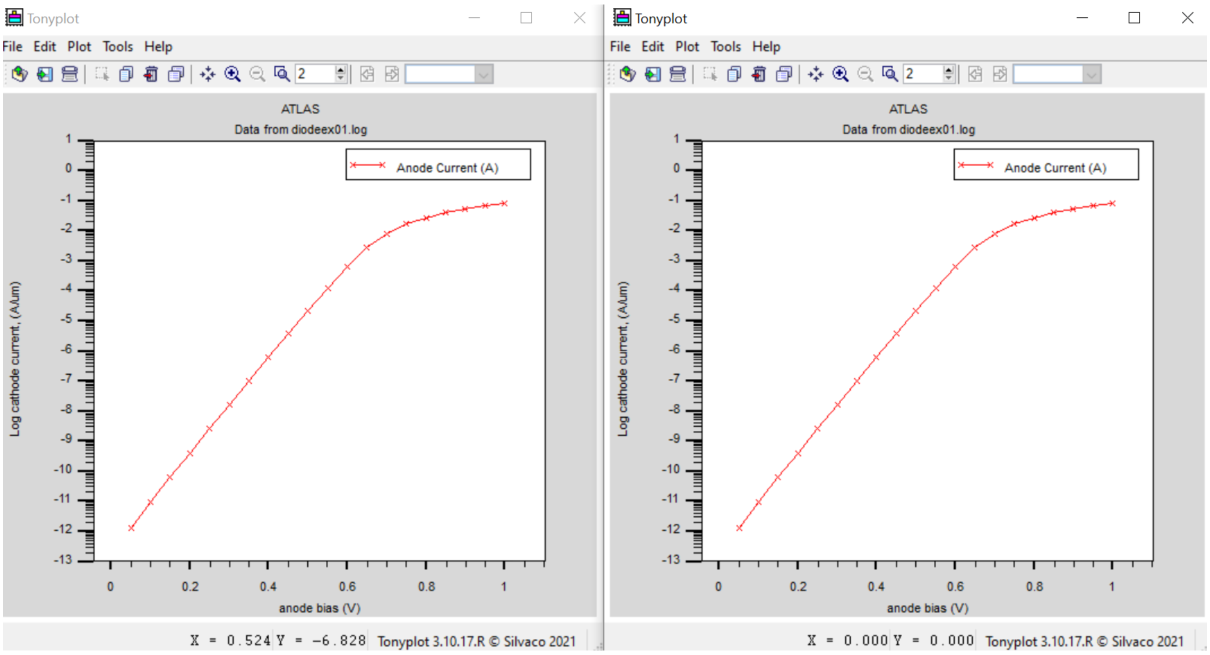
5. Now that the device has been fully realised, we need to set its models. the model statement is used to specify the following set of models: carrier concentration dependent mobility **(**ccsmob**)**, field dependent mobility, band-gap narrowing, SRH and Auger recombination.
6. To set a Schottky contact, we use **contact name=<char> work=<val>**. The work variable is used to set the work function of a Schottky electrode. Here, since the substrate is n-type silicon with an affinity of 4.17 V, the specified work function of 4.97 V provides a Schottky-barrier height of 0.8V. The default barrier height is zero (a perfect ohmic contact). This condition is assumed for the cathode.
7. Next, we simulate the I-V characteristics of the device. The simulation applies a voltage ranging from the anode voltage to 1.0V in 0.05V steps using the solve statement.
8. The results of the simulation are then displayed using TonyPlot.
9. The TonyPlot interface can be used to select the type of graph and variables to plot:
   a. In the graph interface that appears, select the "**Display**" tab
   b. Select the variables you want to plot.
   c. Click on "**OK**".

Code:

```
# (c) Silvaco Inc., 2018
go atlas

mesh  space.mult=1.0
#
x.mesh loc=0.00 spac=0.5
x.mesh loc=3.00 spac=0.2
x.mesh loc=5.00 spac=0.25
x.mesh loc=7.00 spac=0.25
x.mesh loc=9.00 spac=0.2
x.mesh loc=12.00 spac=0.5
#
y.mesh loc=0.00 spac=0.1
y.mesh loc=1.00 spac=0.1
y.mesh loc=2.00 spac=0.2
y.mesh loc=5.00 spac=0.4


region  num=1  material=silicon x.min=0 x.max=12 y.min=0 y.max=1
region num=2 material=SiO2 x.min=0 x.max=12 y.min=1 y.max=1.002
region  num=3  material=silicon x.min=0 x.max=12 y.min=1.002 y.max=5
region  num=4  silicon x.min=0 x.max=8 y.min=1 y.max=1.002

electr  name=anode  x.min=5  length=3
electr  name=cathode  bot

#....   N-epi doping
doping  n.type conc=5.e20 uniform

#....   Guardring doping
doping   p.type conc=1e19 x.min=0  x.max=3  junc=1 rat=0.6 gauss
doping   p.type conc=1e19 x.min=9 x.max=12 junc=1 rat=0.6 gauss

#....   N+ doping
doping  n.type conc=1e20 region=3 uniform

save outf=diodeex01_0.str


model    conmob  fldmob  srh  auger  bgn
contact     name=anode workf=4.97

solve      init

method newton

log   outfile=diodeex01.log
solve      vanode=0.05  vstep=0.05  vfinal=1  name=anode
tonyplot diodeex01.log -set diodeex01_log.set
quit
```

Results

The impact of the Interstitial layer on Ideality Factor:



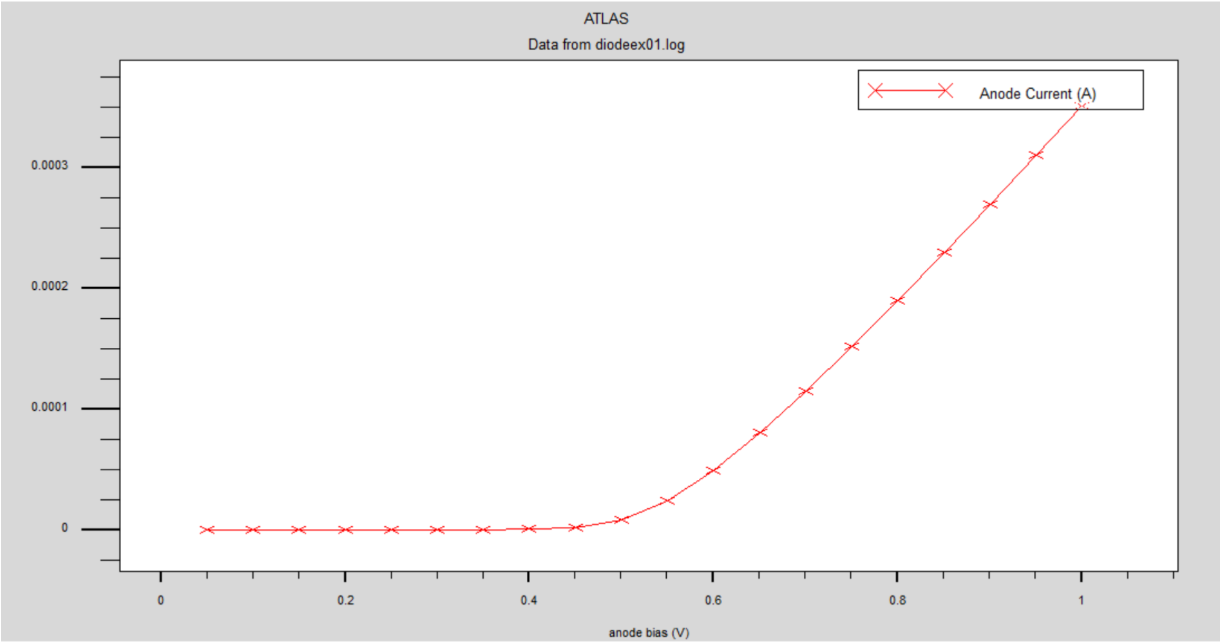
An interfacial layer between the metal and semiconductor of a Schottky diode affects the measured barrier height and built-in potential. The total potential within the device is now divided between the interfacial layer and the semiconductor. This causes the potential across the semiconductor to be lower so that carriers can more easily flow from the semiconductor into the metal, yielding a larger current. The interfacial layer acts as an insulator and thus, reduces the ideality factor. As shown in graphs above, the ideality factor reduces from 2.207 at 10 Å to 2.163 at 20 Å.

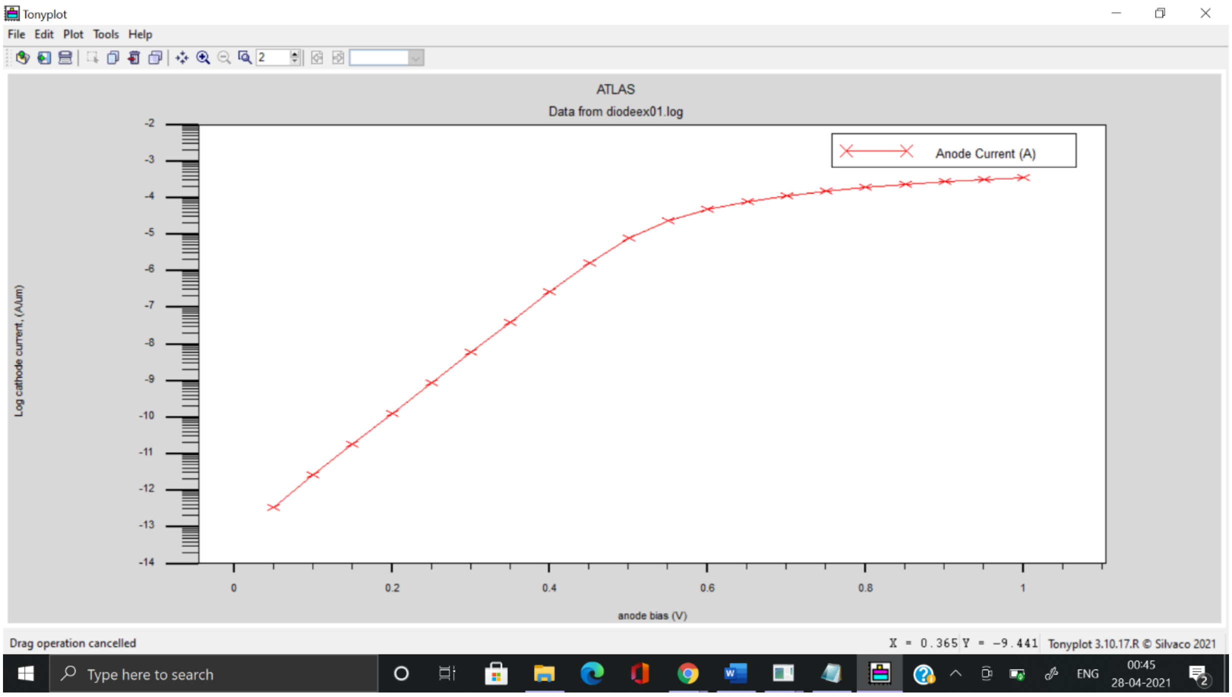
Variation of cut-in voltage and ideality factor with N+ doping:

N+ doping(cm^{-3})	Cut-in voltage(V)	Ideality factor
10^{16}	0.472	1.748
10^{17}	0.498	1.884
10^{18}	0.524	1.944
10^{19}	0.547	1.995
10^{20}	0.6	2.163
10^{21}	0.621	2.337
10^{22}	0.630	2.392

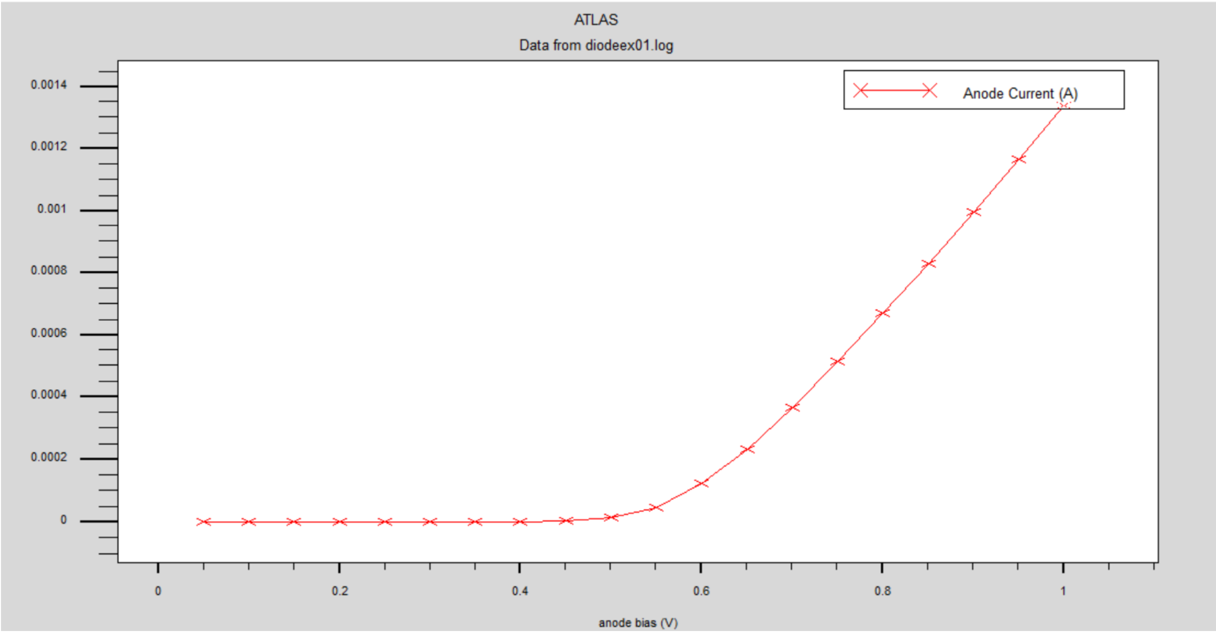
Graphs

$10^{16}(cm^{-3})$:

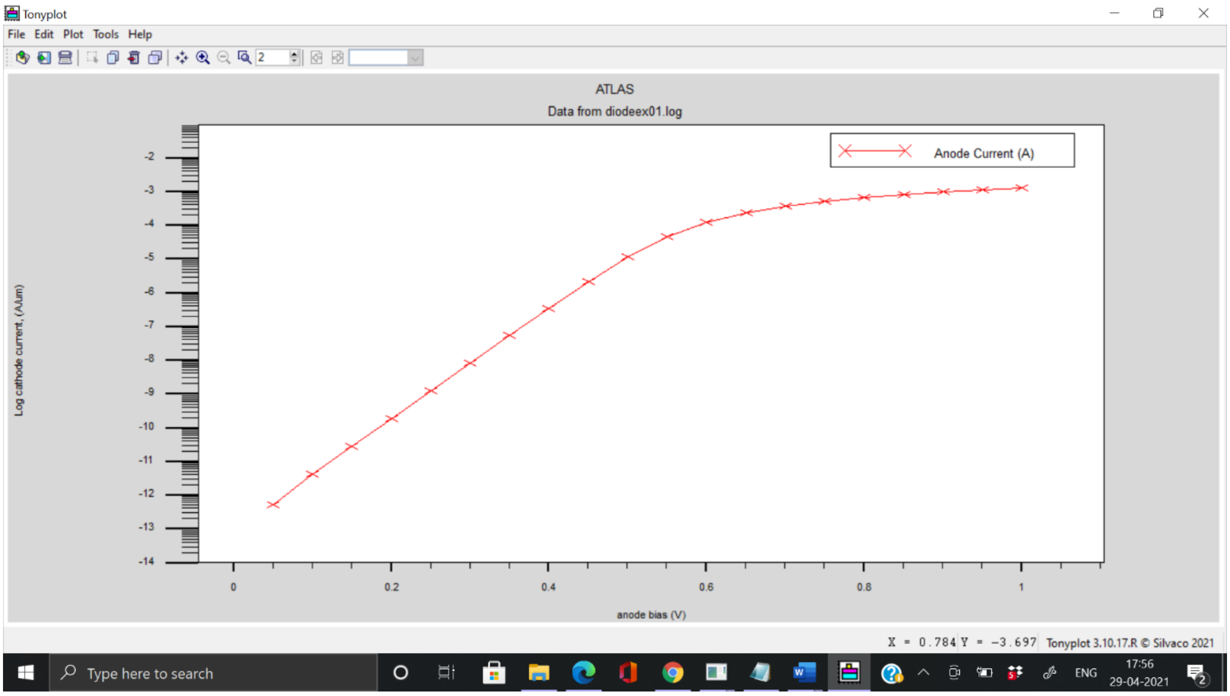




$10^{17}(cm^{-3})$:

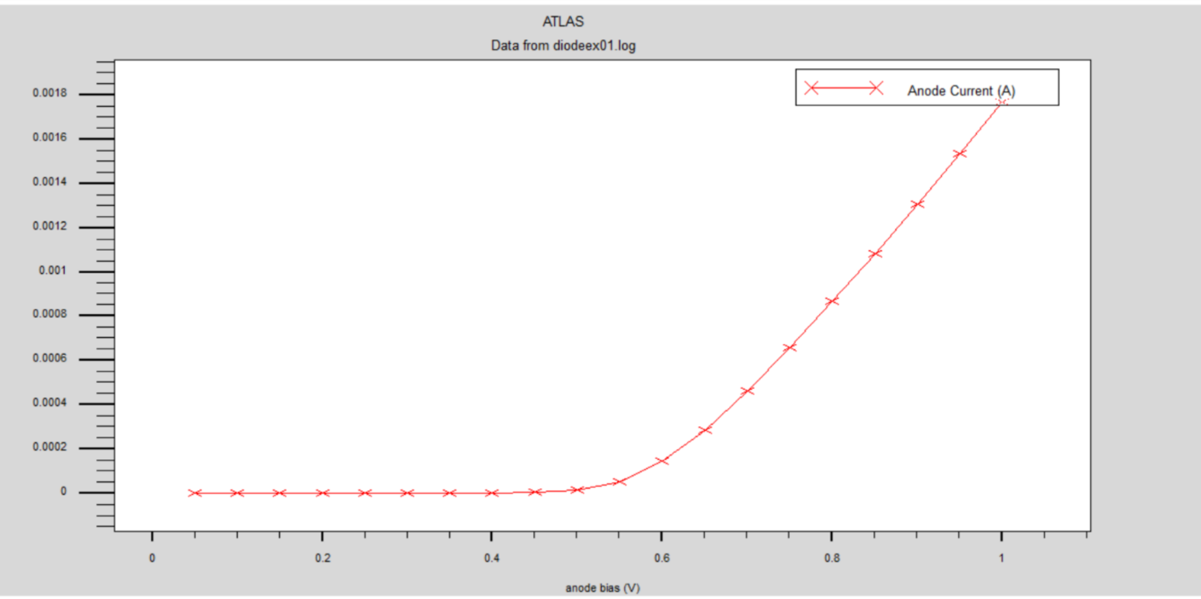


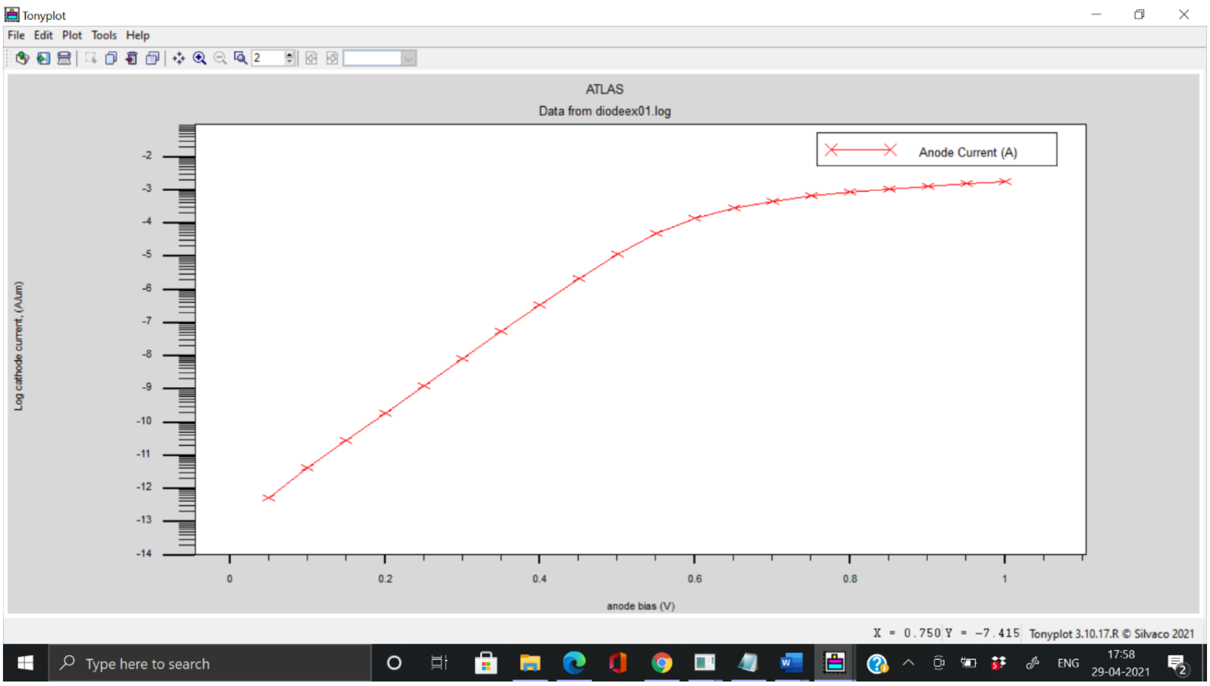
ATLAS
Data from diodeex01.log
Anode Current (A)
0.0014
0.0012
0.001
0.0008
0.0006
0.0004
0.0002
0
0
0.2
0.4
0.6
0.8
1
anode bias (V)



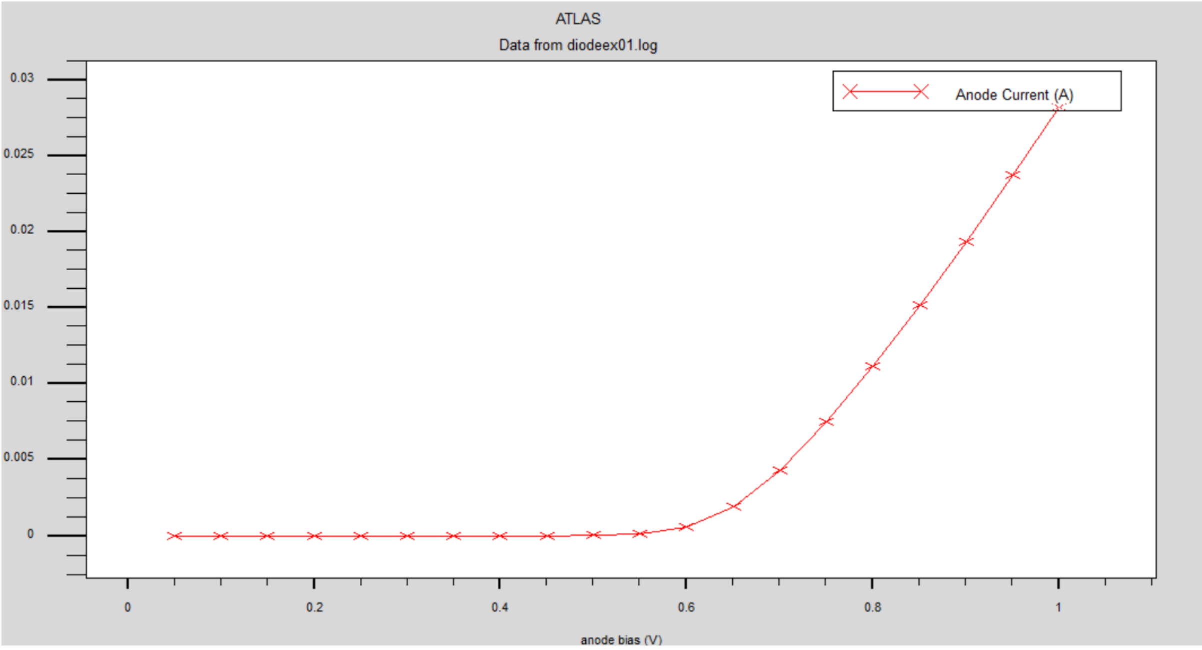
Tonyplot
File Edit Plot Tools Help
ATLAS
Data from diodeex01.log
Anode Current (A)
Log cathode current, (A/um)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
0
0.2
0.4
0.6
0.8
1
anode bias (V)
X = 0.784 Y = -3.697 Tonyplot 3.10.17.R © Silvaco 2021
Type here to search
ENG
17:56
29-04-2021

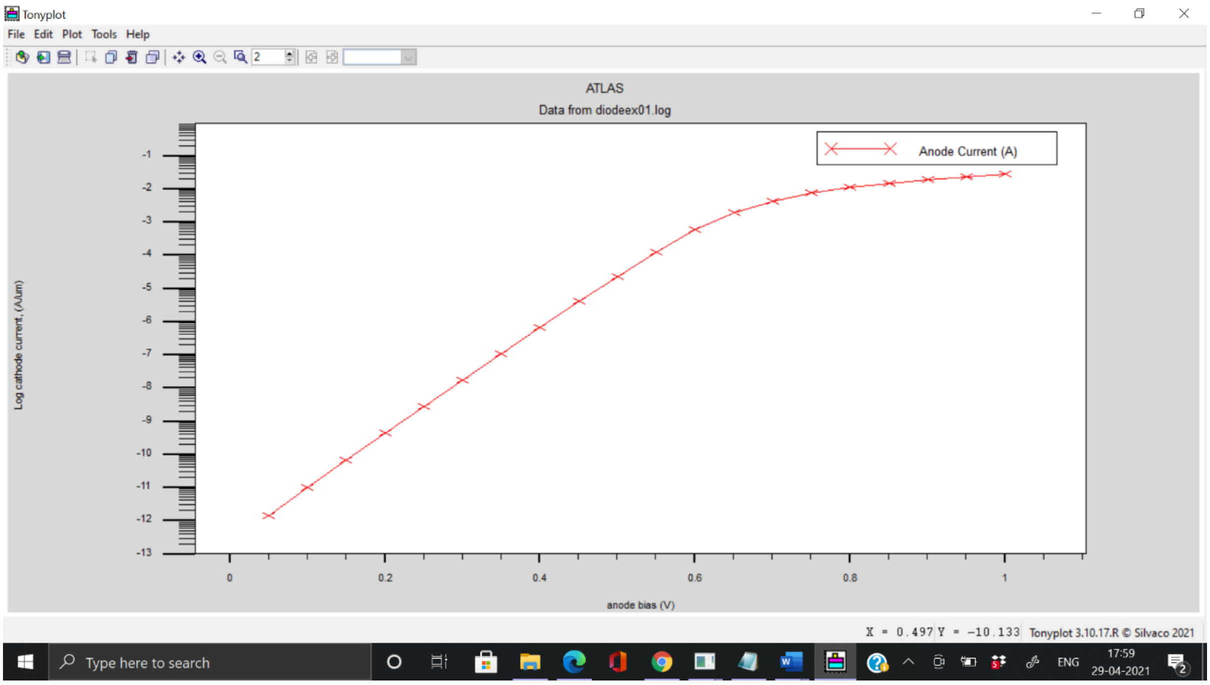
$10^{18}(cm^{-3})$:


ATLAS
Data from diodeex01.log
Anode Current (A)
0.0018
0.0016
0.0014
0.0012
0.001
0.0008
0.0006
0.0004
0.0002
0
0
0.2
0.4
0.6
0.8
1
anode bias (V)

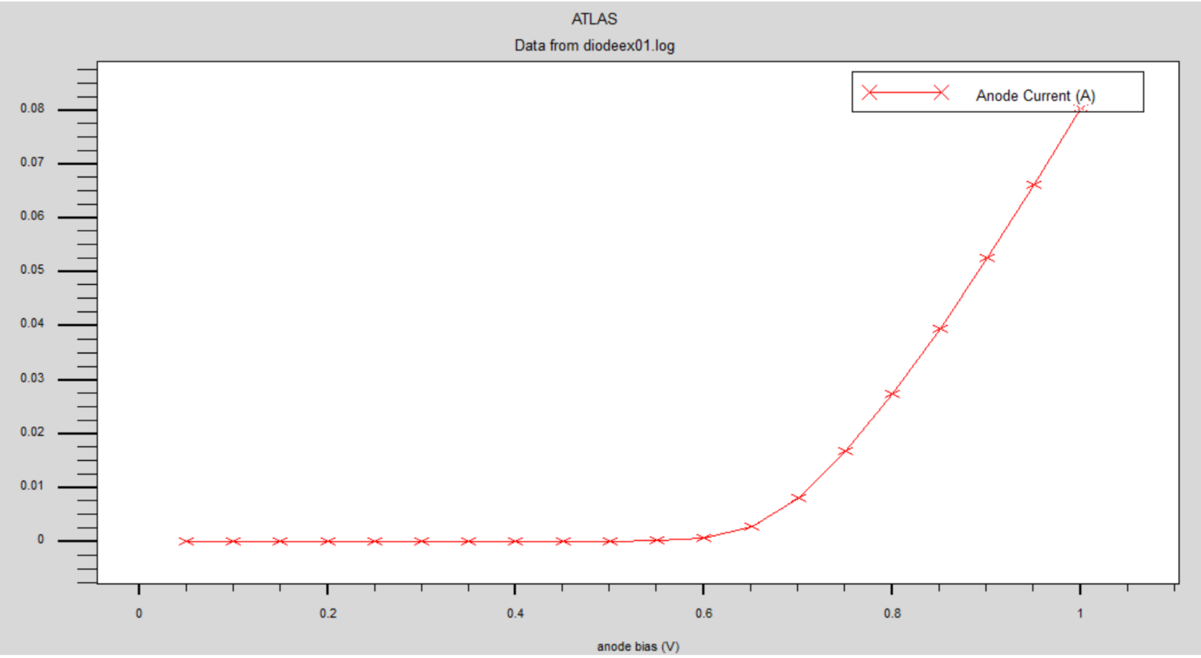

Tonyplot
File Edit Plot Tools Help
ATLAS
Data from diodeex01.log
Anode Current (A)
Log cathode current, (A/um)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
0
0.2
0.4
0.6
0.8
1
anode bias (V)
X = 0.750 Y = -7.415 Tonyplot 3.10.17.R © Silvaco 2021
Type here to search
ENG
17:58
29-04-2021

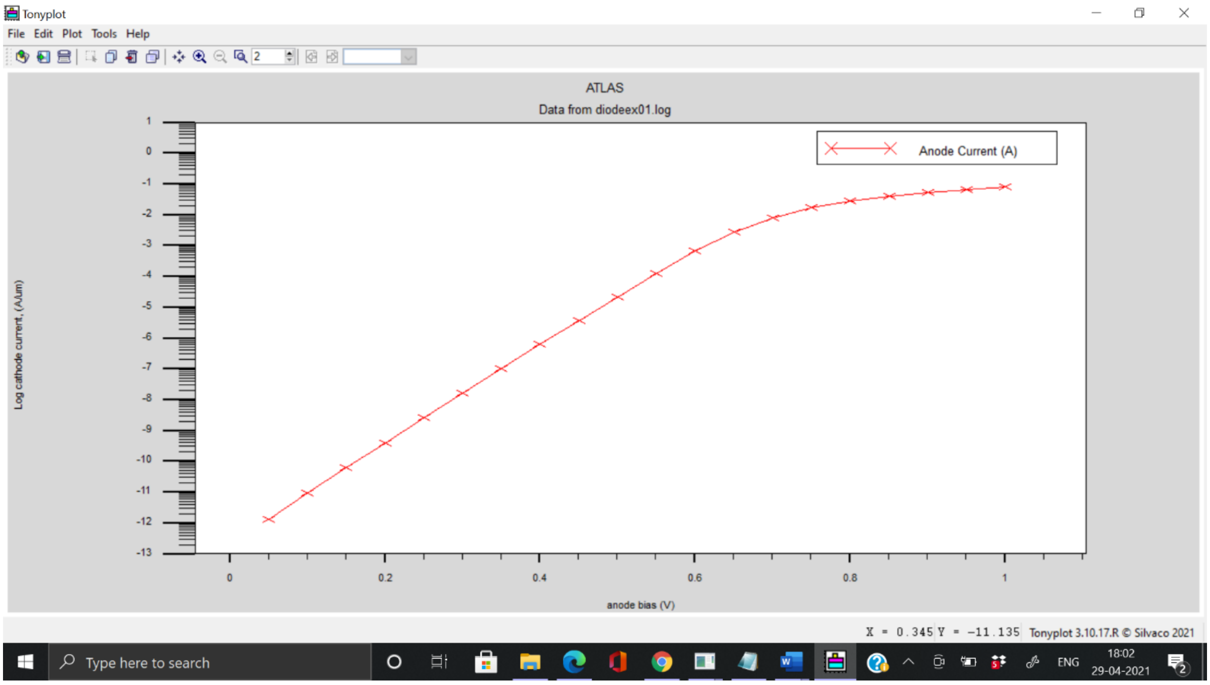
$10^{19}(cm^{-3})$:


ATLAS
Data from diodeex01.log
Anode Current (A)
0.03
0.025
0.02
0.015
0.01
0.005
0
0
0.2
0.4
0.6
0.8
1
anode bias (V)

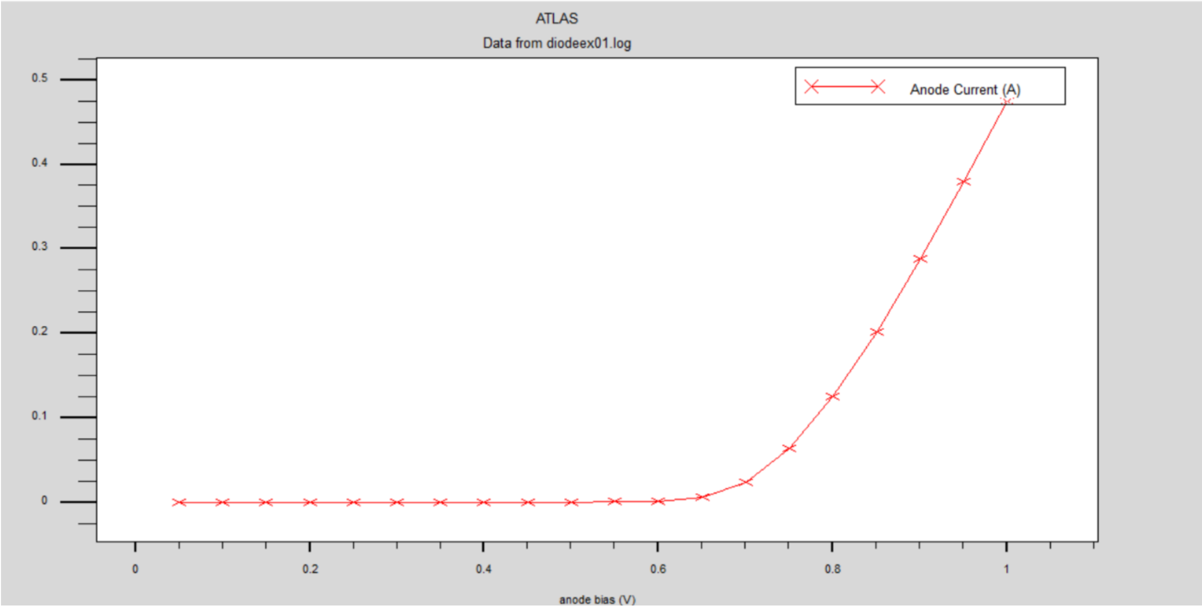

Tonyplot
File Edit Plot Tools Help
ATLAS
Data from diodeex01.log
Anode Current (A)
Log cathode current, (A/um)
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
0
0.2
0.4
0.6
0.8
1
anode bias (V)
X = 0.497 Y = -10.133
Tonyplot 3.10.17.R © Silvaco 2021
Type here to search
ENG
17:59
29-04-2021

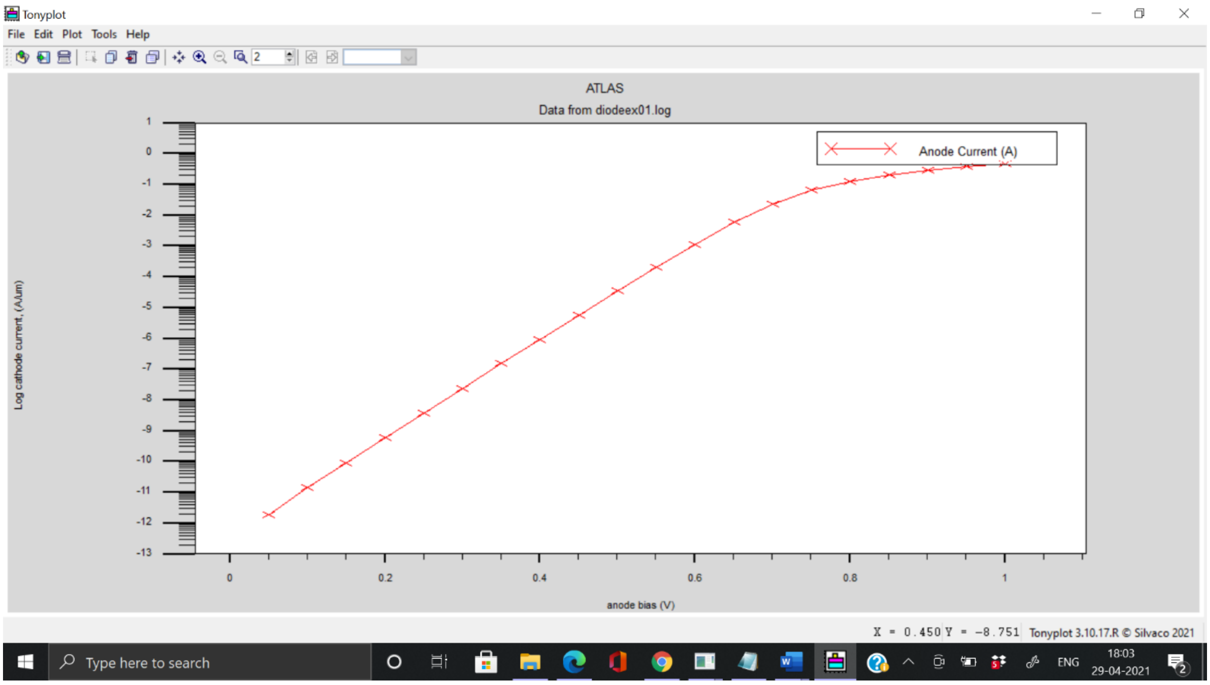
$10^{20}(cm^{-3})$:


ATLAS
Data from diodeex01.log
Anode Current (A)
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.2
0.4
0.6
0.8
1
anode bias (V)


Tonyplot
File Edit Plot Tools Help
ATLAS
Data from diodeex01.log
Anode Current (A)
Log cathode current, (A/um)
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
0
0.2
0.4
0.6
0.8
1
anode bias (V)
X = 0.345 Y = -11.135 Tonyplot 3.10.17.R © Silvaco 2021
Type here to search
ENG
18:02
29-04-2021

$10^{21}(cm^{-3})$:


ATLAS
Data from diodeex01.log
Anode Current (A)
0.5
0.4
0.3
0.2
0.1
0
0
0.2
0.4
0.6
0.8
1
anode bias (V)


Tonyplot
File Edit Plot Tools Help
ATLAS
Data from diodeex01.log
Anode Current (A)
Log cathode current, (A/um)
1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
0
0.2
0.4
0.6
0.8
1
anode bias (V)
X = 0.450 Y = -8.751
Tonyplot 3.10.17.R © Silvaco 2021
Type here to search
ENG
18:03
29-04-2021