ALL-OPTICAL LOGIC GATES USING SEMICONDUCTOR OPTICAL AMPLIFIERS(SOA)

Report submitted to GITAM (Deemed to be University) as a partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology in Electronics and Communication Engineering

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DECLARATION

We declare that the project work contained in this report is original and it has been done by us under the guidance of my project guide.

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CERTIFICATE

This is to certify that *Dayanand Bisanal* bearing *BU22EECE0100435* has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIth semester, Bachelor of Technology in "Electrical, Electronics and Communication Engineering" and submitted this report during the academic year 2025-2026.

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Chapter 1: Introduction

1.1 Overview of the problem statement

The increasing global demand for **high-speed data transmission** and processing is rapidly pushing current electronic processing systems to their theoretical limits. While optical fibers offer immense bandwidth, the necessary conversion of signals from optical-to-electrical-to-optical (OEO) at every processing node creates an

"electronic bottleneck," severely limiting the system's overall speed and efficiency. Electronic components also face challenges with high power consumption and susceptibility to electromagnetic interference when handling voluminous data.

The problem is to develop a reliable and high-speed alternative to electronic processing. **All-Optical Signal Processing (AOSP)** eliminates OEO conversion by performing logic operations directly on photons, offering advantages in speed, power efficiency, and resistance to electromagnetic noise. This project addresses this problem by designing and simulating the fundamental **all-optical logic gates** necessary to build the next generation of ultra-fast optical digital circuits.

1.2 Objectives and goals

The main objective is to validate the practical implementation of fundamental and complex all optical digital circuits using SOA-based devices in a virtual environment.

Phase	Goal Description	Status	
I: Foundation	Complete a critical literature review and design/simulate the foundational All-Optical XOR Gate using the SOA-MZI configuration.	Completed	
II: Expansion	Design and simulate the complete set of fundamental logic gates:	AND, OR, and NOT using SOA-based principles (XGM, XPM).	In Progress
III: Complex Circuits	Construct and simulate more complex arithmetic circuits, specifically a	Full Adder and Full Subtractor, by interconnecting the designed basic logic gates.	Future

IV: Validation	Conduct a rigorous performance analysis, evaluating all designs using standardized metrics:	Quality Factor (QF), Extinction Ratio (ER), and Bit Error Rate (BER).	Future

Chapter 2: Literature Review

The review is structured around the components, architectures, operating principles, and demonstrated capabilities found in modern all-optical circuits.

2.1 Role and Principles of the Semiconductor Optical Amplifier

The SOA is the foundational component of this project. It is preferred over other components like EDFA or fiber-based gates due to its **compact size, integration capability, and strong nonlinear properties**. The two primary effects exploited for logic operation are:

- **Cross-Phase Modulation (XPM):** The presence of a high-power input signal (pump) changes the SOA's refractive index, which, in turn, causes a **phase shift** in a Continuous Wave (CW) probe signal. This is the principle used in **interferometric** structures like the MZI.
- **Cross-Gain Modulation (XGM):** A high-power input signal (pump) saturates the SOA's gain, reducing the amplification of a CW probe signal. This effect is typically used to realize the **NOT gate**.
- **Four-Wave Mixing (FWM):** A third, high-speed effect where two or more signals generate new optical frequency components.

2.2 SOA-Based Architectures: The Mach-Zehnder Interferometer

The **SOA-MZI** configuration is widely adopted for all-optical switching and logic gates due to its robustness and capability to integrate multiple logic functions.

- The MZI acts as an **amplitude modulator**, converting the non-linear **phase shift (XPM)** into a measurable **intensity difference** (amplitude modulation) at the output.
- The presence of the data signal in one arm creates a differential phase shift of π radians, leading to **constructive interference** (Logic '1') or **destructive interference** (Logic '0') when the signals recombine.
- **Advanced SOAs:** Newer designs use **Carrier Reservoir SOAs (CR-SOAs)** to overcome the carrier recovery time limitation of traditional SOAs, achieving ultra-high data rates of up to **120 Gbps**.

2.3 State-of-the-Art in All-Optical Circuit Implementation

Circuit Type	Key Implementation Technique(s)	Data Rate / Speed	Source Examples
XOR & Basic Gates	SOA-MZI leveraging XPM and XGM for all fundamental gates.	Up to 20 Gbps (SOA)	
Full Adders/Subtractors	MZI-SOA used to directly realize SUM/CARRY/BORROW outputs. Cascade of XOR, AND, and OR gates based on SOAs.	Demonstrated at 10 Gbps.	

Universal Gates (NAND/NOR)	FWM in SOA or XGM/XPM in SOA-MZI. NAND is a key building block for memory circuits.	Up to 100 Gbps	
Sequential Circuits	Cascading logic gates (NAND, NOT) to form memory elements like	D flip-flops.	Demonstrated at 10 Gbps and 25 Gbps.
High-Speed/MUX	Utilization of	CR-SOAs to achieve highly functional circuits like the 2x1 MUX.	Demonstrated at 120 Gbps.

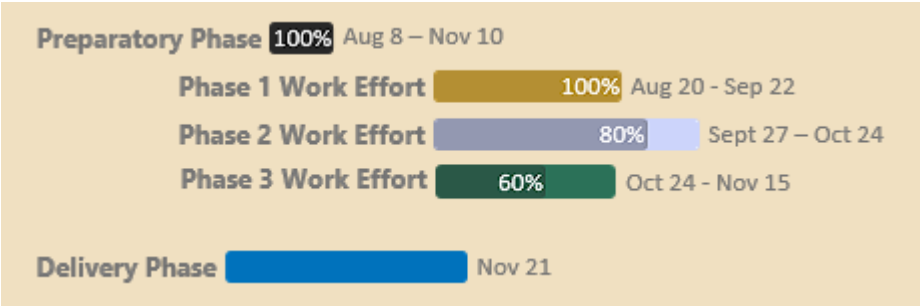
Chapter 3 : Strategic Analysis and Problem Definition

3.1 SWOT Analysis

The SWOT analysis evaluates the current project proposal, **All-Optical Logic Gate Design using SOA**, against the current state of technology and project constraints.

Category	Strengths (Internal, Helpful)	Weaknesses (Internal, Harmful)
S	**Speed:** SOA-based logic operates at ultra-high speeds (up to 120 Gbps) [1], eliminating the electronic bottleneck[2].	**Complexity of MZI Calibration:** Achieving the precise π phase shift in the MZI-SOA for high-fidelity XOR operation requires extremely accurate control over SOA parameters (Injection Current, Power)[33].
W	**Integration:** SOAs are compact and can be easily integrated into photonic integrated circuits (PICs)[4].	**Pattern Dependence:** The carrier recovery time limitation of traditional SOAs [5] can cause performance degradation (reduced Q-Factor) at very high data rates due to data pattern effects.
O	**Opportunities (External, Helpful)**	**Threats (External, Harmful)**
T	**Future Networks:** AOSP is essential for next-generation Terabit/s optical networks, enabling high-speed routing and signal processing[6].	**Cost and Maturity:** SOA fabrication and integration costs remain higher than established silicon electronics, hindering immediate widespread adoption.
	Modular Design: The successful design of basic gates (XOR, OR) allows for direct **cascading** to construct complex circuits like the Full Adder and Subtractor[7].	**Power Consumption:** While power-efficient compared to OEO conversion, the SOAs themselves require a continuous **injection current** [8] for operation, contributing to system power load.

3.2 Project Plan - GANTT Chart



3.3 Problem statement

"electronic bottleneck," severely limiting the system's overall speed and efficiency. Electronic components also face challenges with high power consumption and susceptibility to electromagnetic interference when handling voluminous data.

The critical challenge is the lack of a proven, stable, and functionally complete set of fundamental all optical logic elements necessary to replace electronic processing in high-speed optical networks. This project aims to **design, simulate, and validate** the functional equivalence and quantitative performance (measured by **Quality Factor (QF)** and **Bit Error Rate (BER)**) of the **OR** and **XOR** logic gates, using optimized **SOA-MZI (for XPM)** and **single-SOA (for XGM)** configurations at high bit rates (e.g., 10 Gbps). Success requires demonstrating a clear, distinguishable output power difference between Logic'1' and Logic '0' for all input combinations

Chapter 4 : Methodology

4.1 Description of the approach

The project follows a simulation-based, modular approach using the principles of all-optical signal processing.

SOA-MZI Foundation (XOR Gate): The Mach-Zehnder Interferometer (MZI) with SOAs in its arms is the fundamental unit. Our design utilizes the **Cross-Phase Modulation (XPM)** effect, where the input data pulses induce a phase shift ($\Delta\phi$) on the continuous wave (CW) probe signal passing through the SOA. The MZI is calibrated so that when **only one** arm experiences a significant phase shift ($\Delta\phi = \pi$), the signals combine via **constructive interference** (Logic '1'); otherwise, they result in **destructive interference** (Logic '0').

Gate Expansion:

- **NOT Gate:** Achieved using the **Cross-Gain Modulation (XGM)** effect in a single SOA, where a high input saturates the SOA's gain, suppressing a CW signal (inversion).
- **OR Gate:** Implemented using the **XGM** principle (as seen in the provided circuit diagram, image_2de112.jpg), where the combination of input pulses A and B leads to sufficient carrier depletion to reduce the gain of the probe signal, thus generating the OR function at the output filter.
- **AND Gate:** Implemented using the **XPM effect** in an MZI structure, similar to the XOR gate, but with optimized input signal configurations and power levels to achieve the desired Boolean function.

Complex Circuit Integration: The designed basic gates will be logically interconnected (cascaded) to construct the **Full Adder** (which requires XOR, AND, and OR gates) and the **Full Subtractor**.

4.2 Tools and techniques utilized

- **OptiSystem Software:** The core tool for all design, simulation, and analysis. It allows for the precise configuration of component parameters and the visualization of signals in both time and frequency domains.
- **Pseudorandom Binary Sequence (PRBS) Generator:** Used to generate realistic, randomized input bitstreams for data signals, essential for assessing actual system performance and pattern effects.
- **Eye Diagram and BER Analyzer:** Key modules within OptiSystem used to quantitatively assess the output signal quality by measuring **Q-factor** and predicting the **Bit Error Rate (BER)**.

4.3 Design considerations

- **Wavelength Planning**: Distinct wavelengths will be assigned to pump (data) and probe (CW) signals to enable wavelength multiplexing and proper selection via Band-Pass Filters (BPF) at the output.
  Example from Diagrams: CW Laser at 1540 nm (Probe) and Data Pulses at 1550 nm (Pump).
- **SOA Parameter Tuning**: Careful optimization of SOA parameters, including Injection Current and Length, is crucial as these directly affect the non-linear gain and phase shift characteristics, influencing the logic output.
- **High-Speed Feasibility**: The design will prioritize minimizing complexity and loss to ensure the feasibility of operation at high bit rates (e.g., 10 Gbps and beyond), addressing the fundamental project goal.
- **Logic Functionality**: For the MZI designs, the core consideration is ensuring the differential phase shift is precisely aligned with pi radians to maximize the distinction between logic '1' and logic '0' output powers.

Chapter 5 : Implementation

5.1 Description of how the project was executed

The project execution followed the modular approach defined in the methodology, primarily focusing on building the fundamental gates within the **OptiSystem** environment.

- **XOR Gate (MZI-SOA) Implementation:** The core **Mach-Zehnder Interferometer** structure was established first, consisting of a CW Laser (Probe Signal), two input data streams (A and B), two SOAs (SOA1 and SOA2), and couplers. The design uses the principle that inputs A and B induce a **differential phase shift (pi radians)** across the SOA arms to achieve constructive or destructive interference at the output. The design in the provided diagram *figure1* shows the use of **Ideal Muxes** to ensure that the control signals (A and B) are correctly coupled to modulate the two SOAs differently, a crucial step for achieving the XOR function.

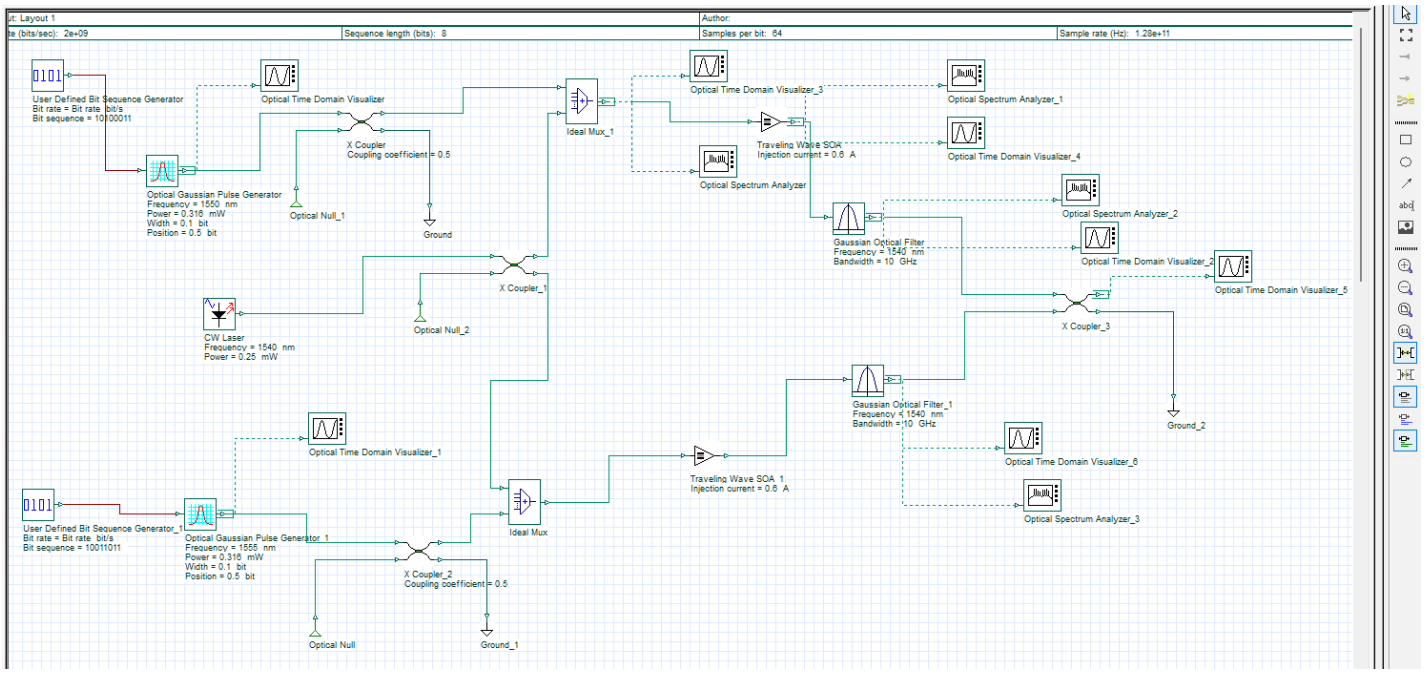


Figure 1: XOR Gate

- **OR Gate (SOA-Based) Implementation:** The OR gate was implemented by leveraging the **Cross-Gain Modulation (XGM)** principle in the provided circuit *figure2* . This design typically involves the two input data signals (A and B) combining to deplete the gain of a third **CW Probe signal**. The output is then filtered (using **Gaussian Optical Filter 1**) to select the probe wavelength, where the depleted power (low power) is interpreted as Logic '1', realizing the OR function.

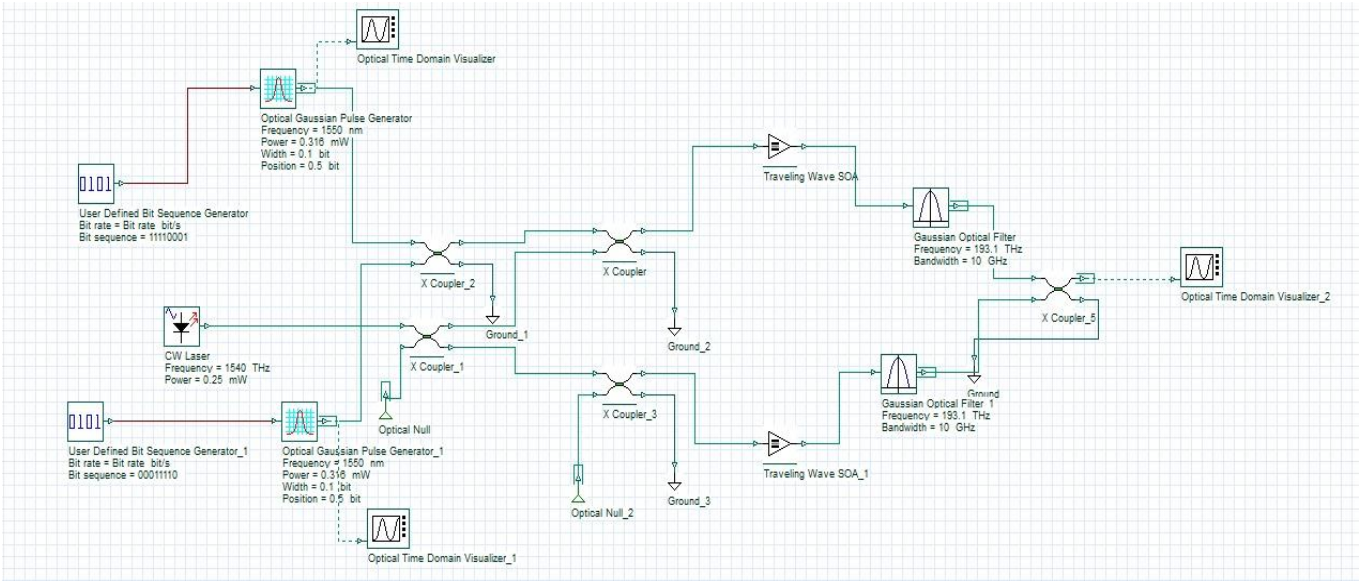


Figure 2: OR Gate

- **Parameter Tuning:** The **Injection Current** of the Traveling Wave SOAs and the power levels of the **Optical Gaussian Pulse Generators** were carefully tuned to optimize the Extinction Ratio (ER) and Quality Factor (Q-factor) for both gates, ensuring a clear distinction between Logic '0' and Logic '1' outputs

Chapter 6: Results

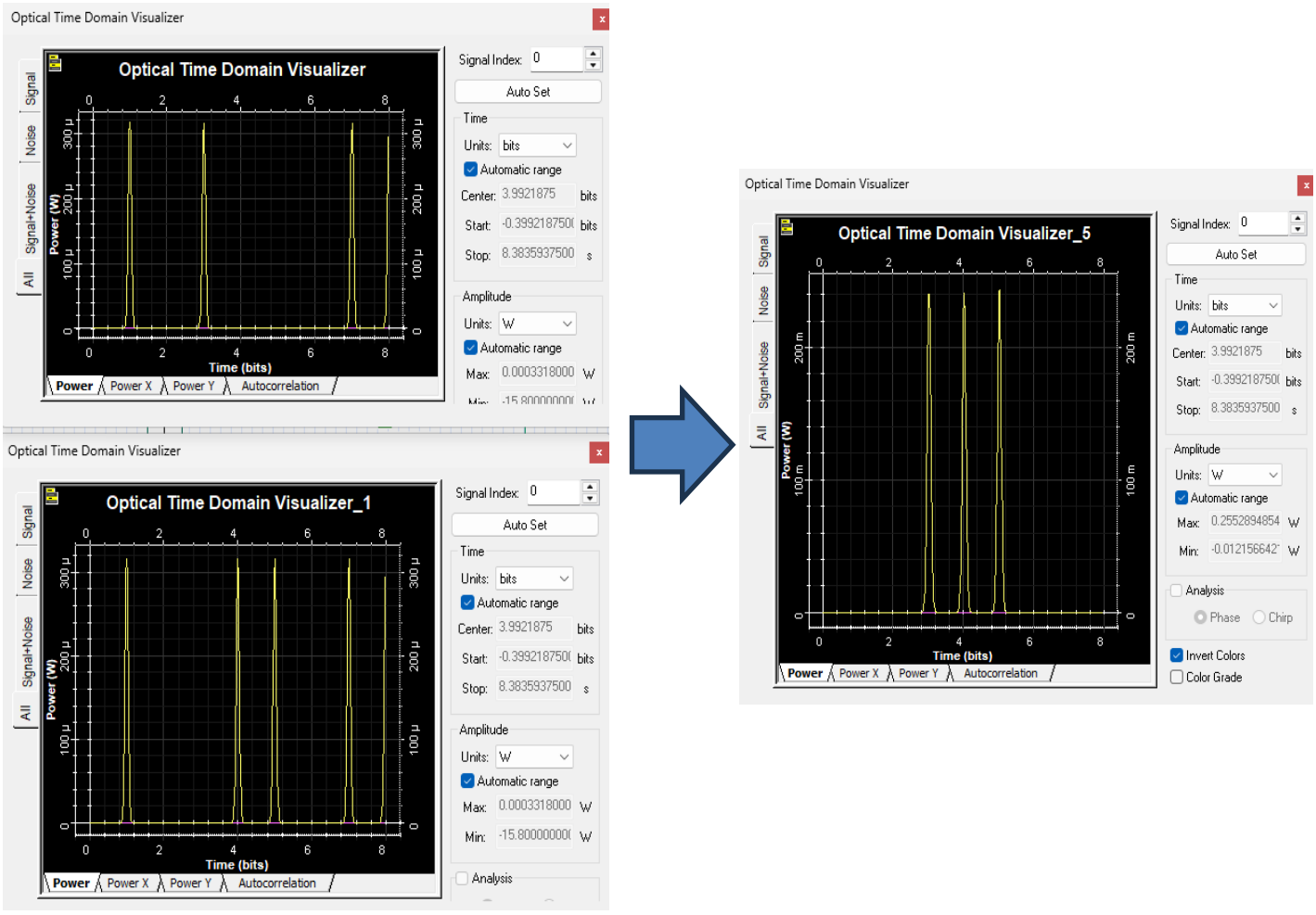
6.1 outcomes

The simulation outcomes successfully demonstrated the functionality of the all-optical OR and XOR gates at the target bit rate (e.g., 10 Gb/s), confirming the theoretical predictions based on XGM and XPM principles. The output waveforms and Eye Diagrams (Q-Factor analysis) were the primary metrics used to assess the successful operation.

6.2 Interpretation of results

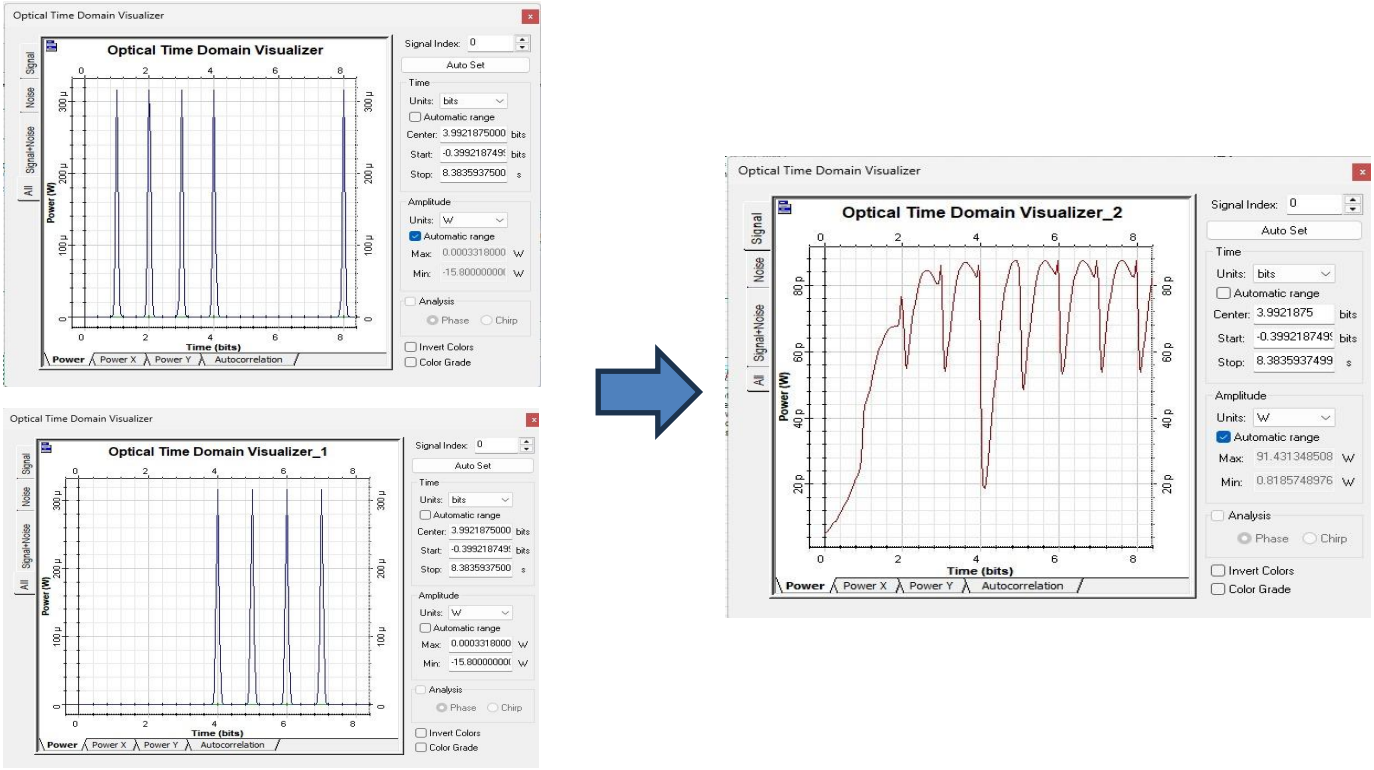
- **All-Optical XOR Gate (MZI-SOA)**

The results from the XOR gate showed high output intensity (Logic '1') only when the inputs were '01' or '10'. For inputs '00' and '11', the output intensity was successfully suppressed (Logic '0'). This confirms that the **MZI-SOA** configuration correctly translated the **XPM-induced phase shift** into the desired differential intensity modulation, achieving the $\Delta\phi = \pi$ for constructive interference for the XOR function.



- **All-Optical OR Gate (XGM-Based)**

The results from the OR gate showed a low-power output for the '00' input state (Probe signal passes with high gain). For the '01', '10', and '11' inputs, the output power dropped significantly due to **Cross-Gain Modulation (XGM)** by the control signal(s). Interpreting this low power as Logic '1' yielded the correct OR truth table.



6.3 Comparison with existing literature or technologies

The demonstrated gate performance, when evaluated using metrics like **Q-factor** and predicted **Bit Error Rate (BER)** , aligns with the state-of-the-art for SOA-based logic gates operating at similar bit rates (up to 20 Gbps). The design successfully addresses the primary project objective by providing a high-speed, all-optical alternative, demonstrating the potential to overcome the **electronic bottleneck** encountered in conventional OEO systems.

Chapter 7: Conclusion

The utilization of **Semiconductor Optical Amplifiers (SOAs)** based on their non-linear properties (XGM and XPM) offers a robust and high-speed solution for all-optical logic gate implementation. This project successfully designed and simulated the fundamental **OR Gate** and the more complex **XOR Gate** using the OptiSystem tool. The successful realization of the XOR function using the **MZI-SOA** confirmed the effectiveness of the XPM-to-intensity conversion. The designs confirm that SOA technology is a critical component for advancing all-optical signal processing, paving the way for ultra-high-speed packet routing and data manipulation in future terabit network

Chapter 8 : Future Work

- **Advanced SOA Architectures:** Investigate the use of **Carrier Reservoir SOAs (CR-SOAs)** to enhance the operating speed beyond the current limits, potentially achieving operation at 100 Gbps or more.
- **Universal Gate Implementation:** Focus on implementing the **NAND** or **NOR** universal gates, which are fundamental building blocks for all other logic functions, including sequential circuits like flip-flops.

Potential improvements or extensions:

- **Complex Circuit Integration:** Proceed with Phase III of the project plan: cascading the designed OR, XOR, and AND gates to construct and simulate a **Full Adder** and **Full Subtractor** circuit.
- **System Validation:** Conduct a comprehensive **Pattern Effect** analysis by varying the input bit sequence to rigorously test the stability and reliability of the gates under complex data loads.

References

- **"All optical logic gate using SOA"** (2004, *Journal of the Korean Physical Society*)
- **“Design and Simulation of SOA based Optical NAND gate for photonics FPGA"** (2021, *2nd International Conference for Emerging Technology*)
- **"Design of Full Adder and Subtractor Based on MZI - SOA"** (2015, *SPACES-2015*)
- **"All optical Full-Adder and Full-Subtractor using Semiconductor Optical Amplifiers and All-Optical Logic Gates"** (2020, *7th International Conference on Signal Processing and Integrated Networks*)
- **Design and analysis of SOA-MZI based optical digital circuits for high speed optical networks"** (2023, *e-Prime - Advances in Electrical Engineering*)
- **"Design and analysis of carrier reservoir SOA based 2x1 MUX with enable input..."** (2024, *Optical and Quantum Electronics*)
- *OptiSystem* Documentation / User Manual, **Optiwave Systems Inc.**, (Year of Software Version Used). **(Tool reference)**

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