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# *"Design of 6T and 8T SRAM using 15nm FinFET Technology and 45nm CMOS Technology"*

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# CHAPTER 1: INTRODUCTION

## A) SRAM

Memory arrays often account for most transistors in a CMOS system-on-chip. Static RAMs use a memory cell with internal feedback that retains its value as long as power is applied. It has the following attractive properties:

- Denser than flip-flops
- Compatible with standard CMOS processes
- Faster than DRAM
- Easier to use than DRAM

For these reasons, SRAMs are widely used in applications from caches to register files to tables to scratchpad buffers. The SRAM consists of an array of memory cells along with the row and column circuitry SRAM cell needs to be able to read and write data and to hold the data as long as the power is applied. An ordinary flip-flop could accomplish this requirement, but the size is quite large. A standard 6-transistor (6T) SRAM cell can be an order of magnitude smaller than a flipflop. The 6T cell achieves its compactness at the expense of more complex peripheral circuitry for reading and writing the cells. This is a good trade-off in large RAM arrays where the memory cells dominate the area. The small cell size also offers shorter wires and hence lower dynamic power consumption. The 6T SRAM cell contains a pair of weak cross-coupled inverters holding the state and a pair of access transistors to read or write the state. The positive feedback corrects disturbances caused by leakage or noise. The cell is written by driving the desired value and its complement onto the bitlines, bit and bit_b, then raising the wordline, word. The new data overpowers the cross-coupled inverters. It is read by precharging the two bitlines high, then allowing them to float. When word is raised, bit or bit_b pulls down, indicating the data value. The central challenges in SRAM design are minimizing its size and ensuring that the circuitry holding the state is weak enough to be overpowered during a write, yet strong enough not to be disturbed during a read. In phase 2, the SRAM is precharged. In phase 1, the SRAM is read or written.

Dual-port SRAM cell using eight transistors to provide independent read and write ports. For a write, the data and its complement are applied to the WBL and WBL_B bitlines and the WWL wordline is asserted. For a read, the RBL bitline is precharged, then the RWL wordline is asserted. Notice that read operation does not backdrive the state nodes through the access transistor, so read margin is as good as hold margin. The trade-off between read margins, write margin, transistor sizes, and operating voltage limits the minimum operating voltage of a compact 6T cell. Using an 8T dual- port cell for single-ported operation circumvents these trade-offs and allows lower-voltage operation. Intel switched from 6T to 8T cells within the cores for its 45 nm line of Core processors.

## B) FinFET Technology

A Fin Field-effect transistor (FinFET) is a MOSFET built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. These devices have been given the generic name "finfets" because the source/drain region forms fins on the

silicon surface. The FinFET devices have significantly faster switching times and higher current density than the mainstream CMOS technology.

FET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed. The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name. The thickness of the fin determines the effective channel length of the device. In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin.

The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel. This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects. The term FinFET is used somewhat generically. Sometimes it is used to describe any fin-based, multigate transistor architecture regardless of number of gates.

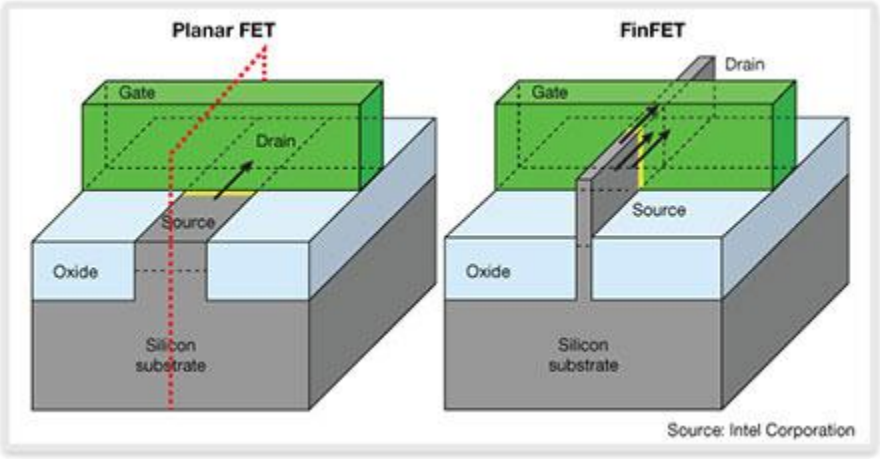


Fig 1: FinFET

# CHAPTER 2: IMPLEMENTATION

## 1) Setup of 15nm FinFET Technology using NCSU Free PDK15

1. Log in to a Linux machine. The setup for this tutorial is currently supported only on Linux machines.
2. Create a directory to run this tutorial, called something like "adetut" (for Analog Design Environment Tutorial). Change to this directory.
3. Type "add cadence2016" at the command prompt. This will add the Virtuoso tools to your search path.
4. Type "add synopsys2015" at the command prompt. This will add Synopsys HSPICE to your search path.
5. Type "setup_freepdk15" at the command prompt. This will setup your directory by copying in various files that are needed to run the Cadence tools, including.*cdsinit*, *lib.defs*, and *cds.lib*. It will also define environment variables needed by the HSPICE libraries.
6. Start the Cadence Design Framework by typing "virtuoso &".
7. Use the ‘Library Manager’ window, to create and browse through the libraries of our own.

## 2) Design of 6T SRAM using 45nm CMOS Technology

### A. Sizing of 6T SRAM cell

The SRAM cell should be sized as small as possible to achieve high density in memory design. The transistor ratio between M3 and M6 must be greater than 1.2 to keep a proper noise margin during the read operation. The proposed 6T SRAM cell uses 1v for its operation when compared to 1.8V used by conventional 180 nm SRAM cell. In this paper, we propose transistor of size 45nm whose voltage of operation is less than 1V. As the supply voltage used for operation is low, the power consumption is scaled down by maximum extent.

Each bit in SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional transistors serve as the access transistors to control the storage cell during the read and write operations. Generally, fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells reduces the cost per bit of memory.

Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL bar. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell.

Table 1: 6T SRAM sizing

| Transistor | Width(nm) |
|---|---|
| M4, M5 | 180 |
| M3, M6 | 180 |
| M1, M2 | 460 |

### B. 6T SRAM Operation

A SRAM has two different working states which are- reading, where the previously stored data is retrieved; writing, where any modification in data is being done.

❖ **Reading**

- Reading only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M6, BL.
- To speed-up reading, a more complex process is used in practice: The read cycle is started by pre-charging both bit lines BL and BLbar, i.e. driving the bit lines to a threshold voltage (midrange voltage between logical 1 and 0) by an external module. Then asserting WL, enabling both the access transistors M5 and M6 which causes the bit line BL voltage to either slightly drop (bottom transistor M3 is ON and top transistor M4 is off) or rise (top transistor M4 is on).
- It should be noted that if BL voltage rises, the BLbar voltage drops, and vice versa. Then the BL and BLbar lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored. The higher the sensitivity of the sense amplifier, the faster the read operation.

❖ **Writing**

- The write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BLbar to 0. A 1 is written by inverting the values of the bit lines.
- WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the transistor.
- In practice, access NMOS transistors M5 and M6 must be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently, when one transistor pair (e.g. M3 and M4) is only slightly overridden by the write process, the opposite transistors pair (M1 and M2) gate voltage is also changed. This means that the M1 and M2transistors can be easily overridden, and so on. Thus, cross-coupled inverters magnify the writing process.

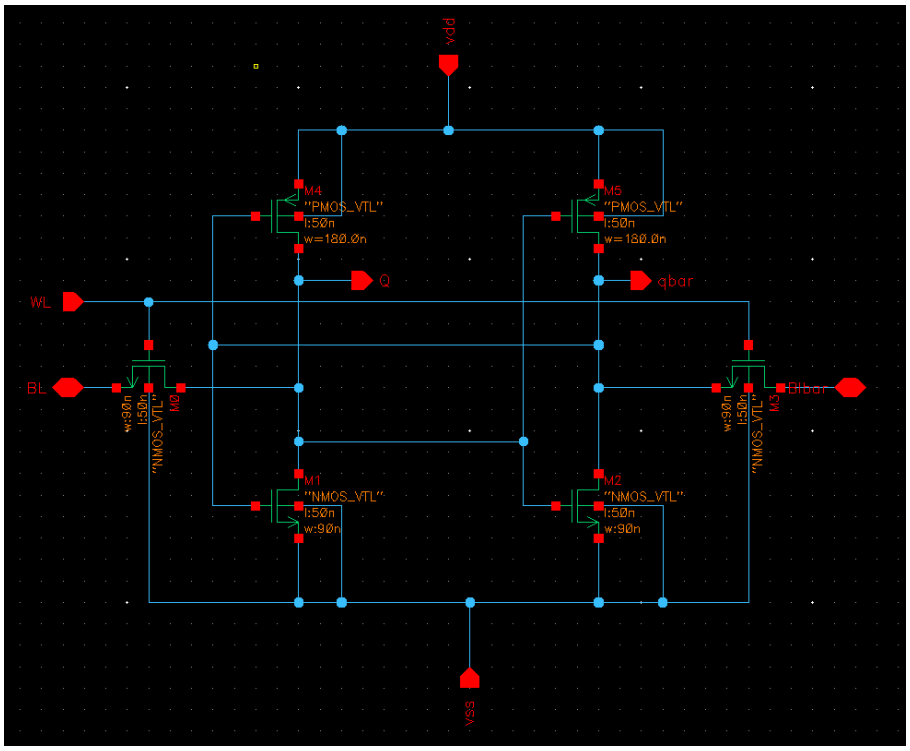


Fig 2: Schematic of 6T SRAM

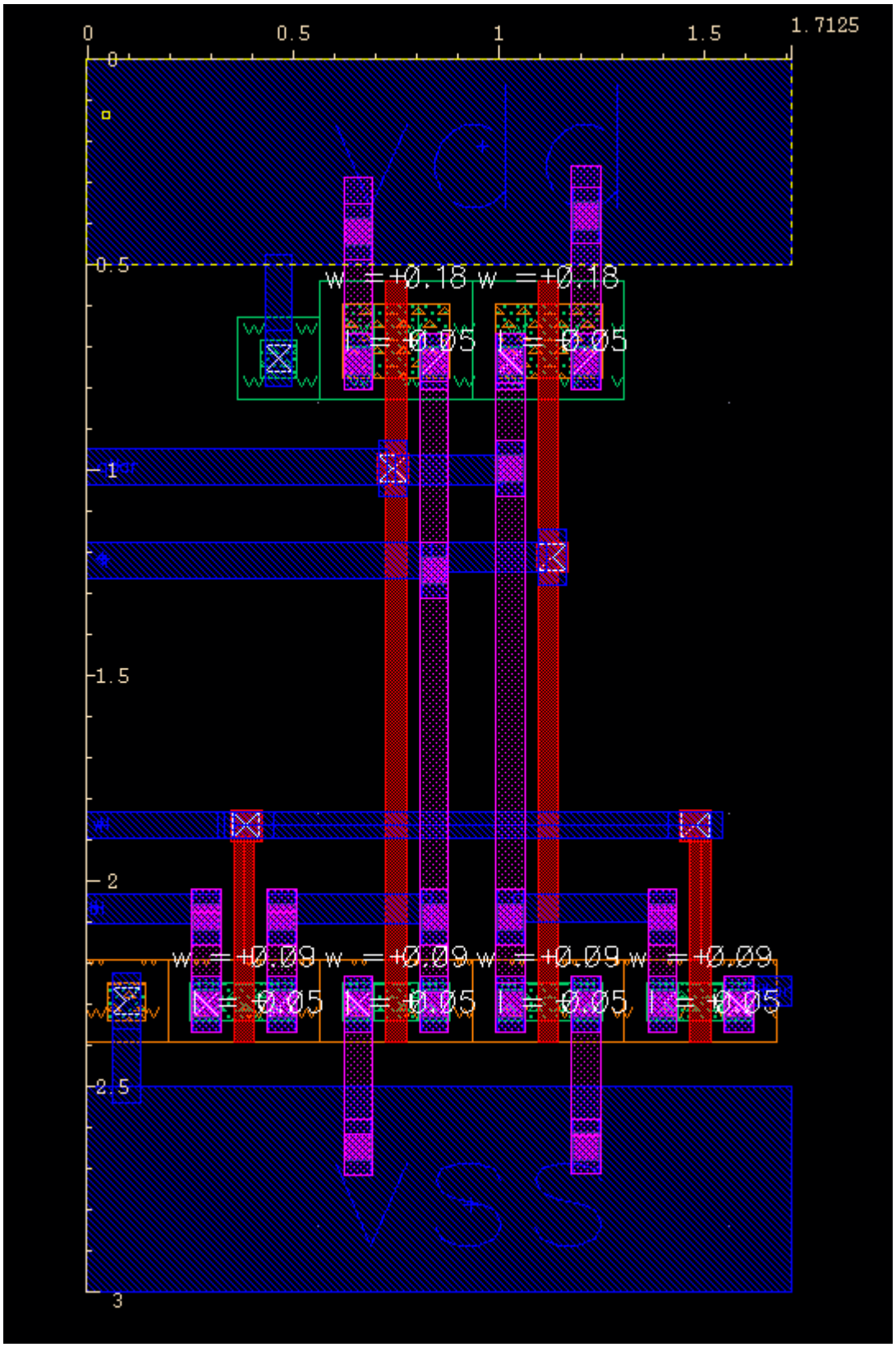


Fig 3: Layout of 6T SRAM in 45nm CMOS Technology

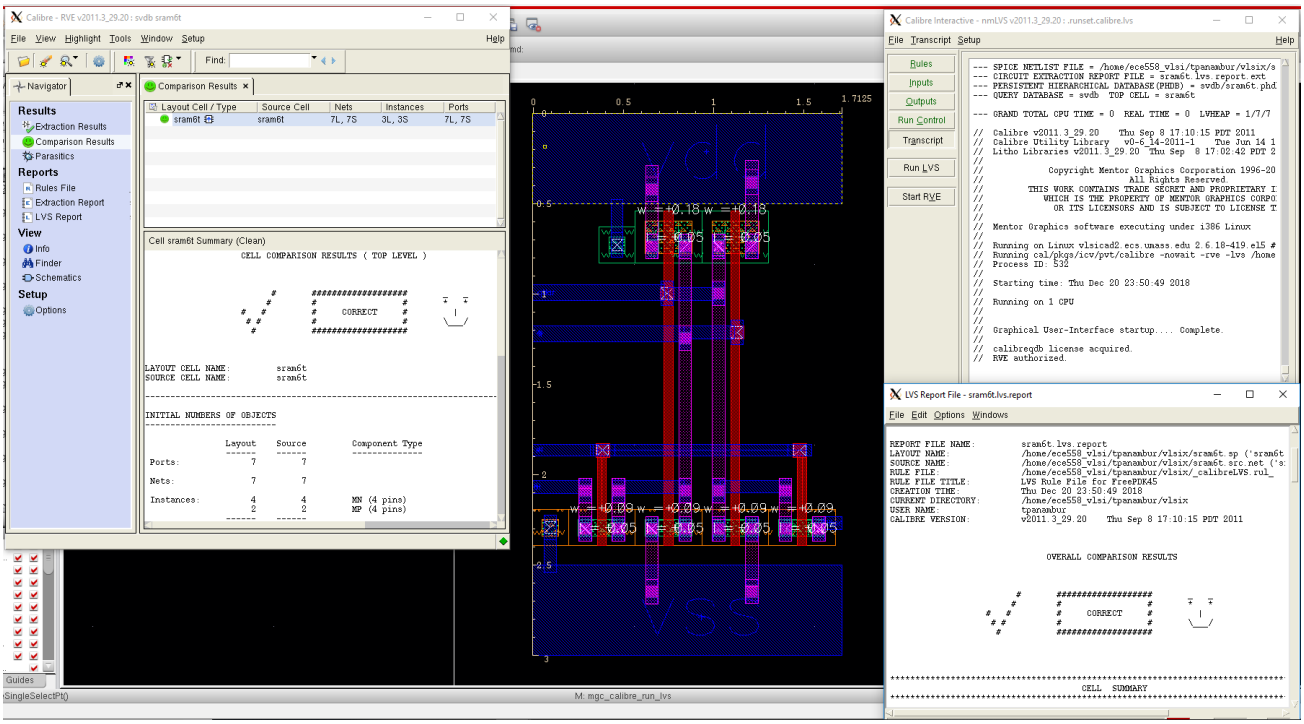


Fig 4: LVS Check of 6T SRAM in 45nm CMOS Technology

## 3) Design of 8T SRAM using 45nm CMOS Technology

8T SRAM utilizes a single bit line and two separate word lines WWL and RWL for write and read operation respectively. The proposed cell has two cross coupled inverters, right inverter has three transistors M1, M4, M3 and left inverter has two transistors M8 and M9. The proposed cell uses an extra transistor CS to cut off the feedback in cross coupled inverters.

In proposed cell the read and write operation are controlled by separate wordlines, which enhances the write ability and read stability of the cell. The write word-line WWL is used to transfer data from single bit-line BL to Q and the inverted information is stored at QBAR. When read word line RWL is activated, the bitline BL is used to transfer data from the cell as the output during read operation. In this proposed cell the stored data at node Q, passes through the PMOS_3 transistor, which control the read operation of the cell. When 0 is stored at node Q, PMOS_3 turn ON and while enabling RWL the charged stored at bit line discharges through the transistors PMOS_3 and NMOS_5. Sense amplifier detects the stored 0 at Q. when 1 is stored at node Q, the connected PMOS_3 transistor remains off. That forces the BL to charge at 1 and sense amplifier read the stored 1.

Table 2: Sizing of 8T SRAM

| Transistor | Width(nm) |
|---|---|
| M3, M9 | 1440 |
| M7, M5, M4 | 720 |
| M1, M8 | 180 |
| M6 | 90 |

**B. 8T SRAM Operation**

The schematic of 8T SRAM memory cell, consists of two inverters connected back to back, two access transistors (M5 & M4) and a read buffer, that consists of two transistors (M6 & M7). During write operation word line WWL, bit line WBL and WBLB are used and RWL & RBL are used during read operation. The RBL is precharged to VDD and the current flows through the transistor of read buffer, not through the internal nodes. So, the internal nodes remain at the same status as they are.

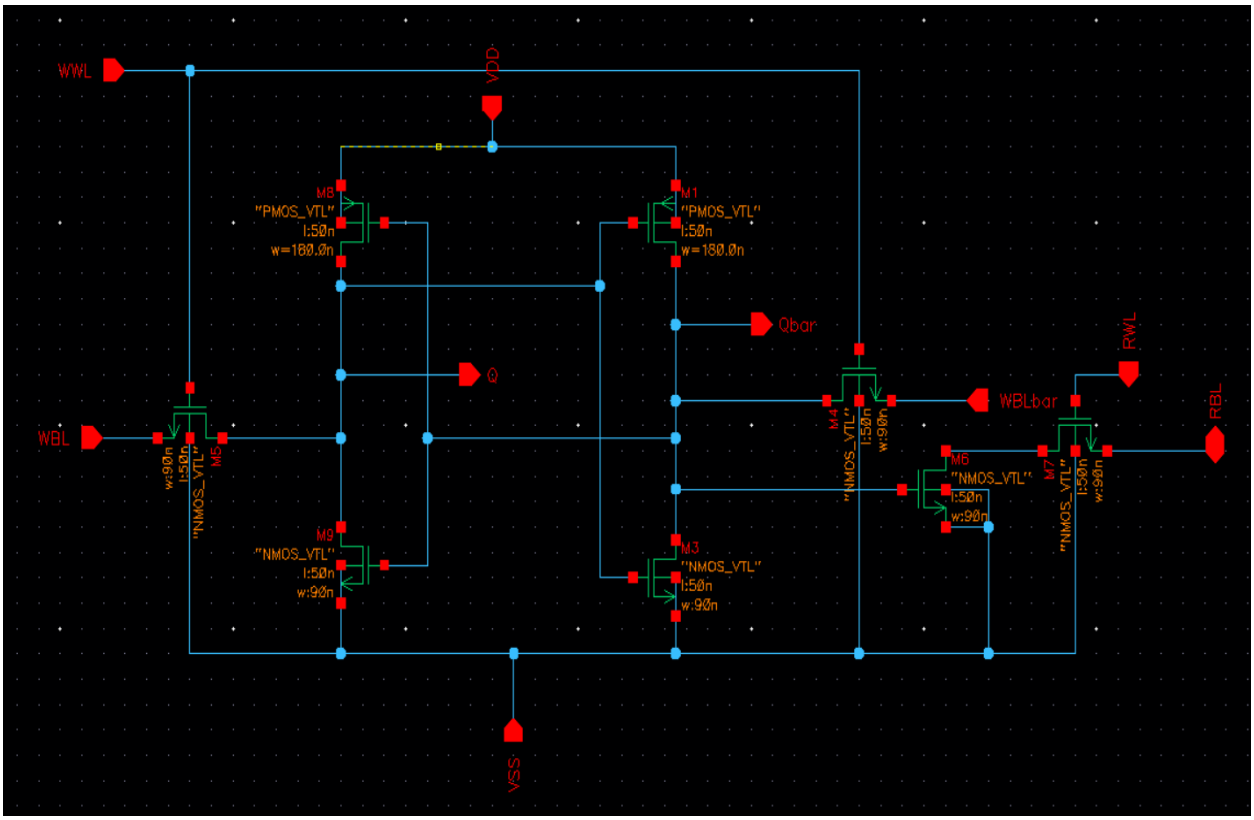


Fig 5: Schematic of 8T SRAM

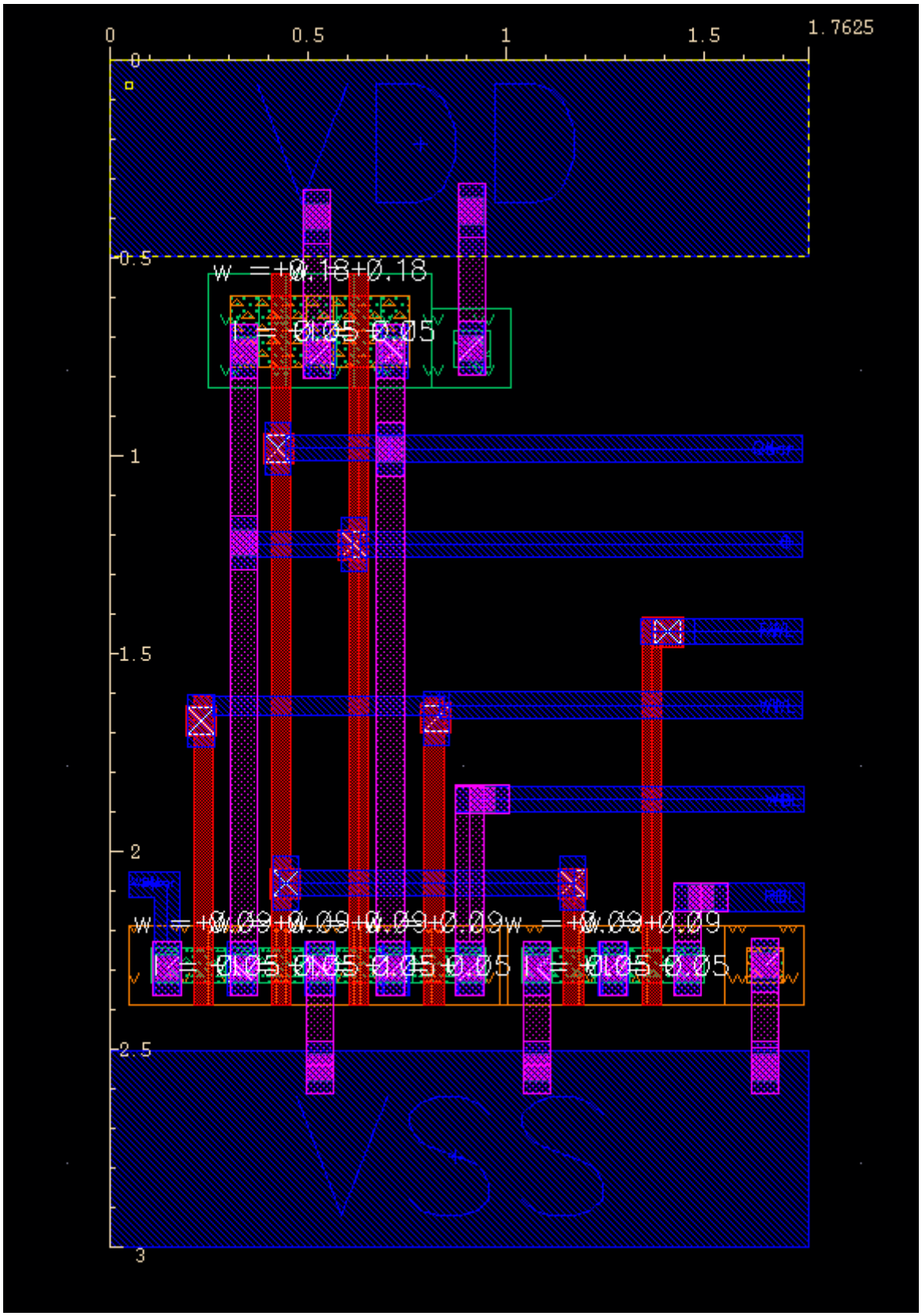


Fig 6: Layout of 8T SRAM in 45nm CMOS Technology

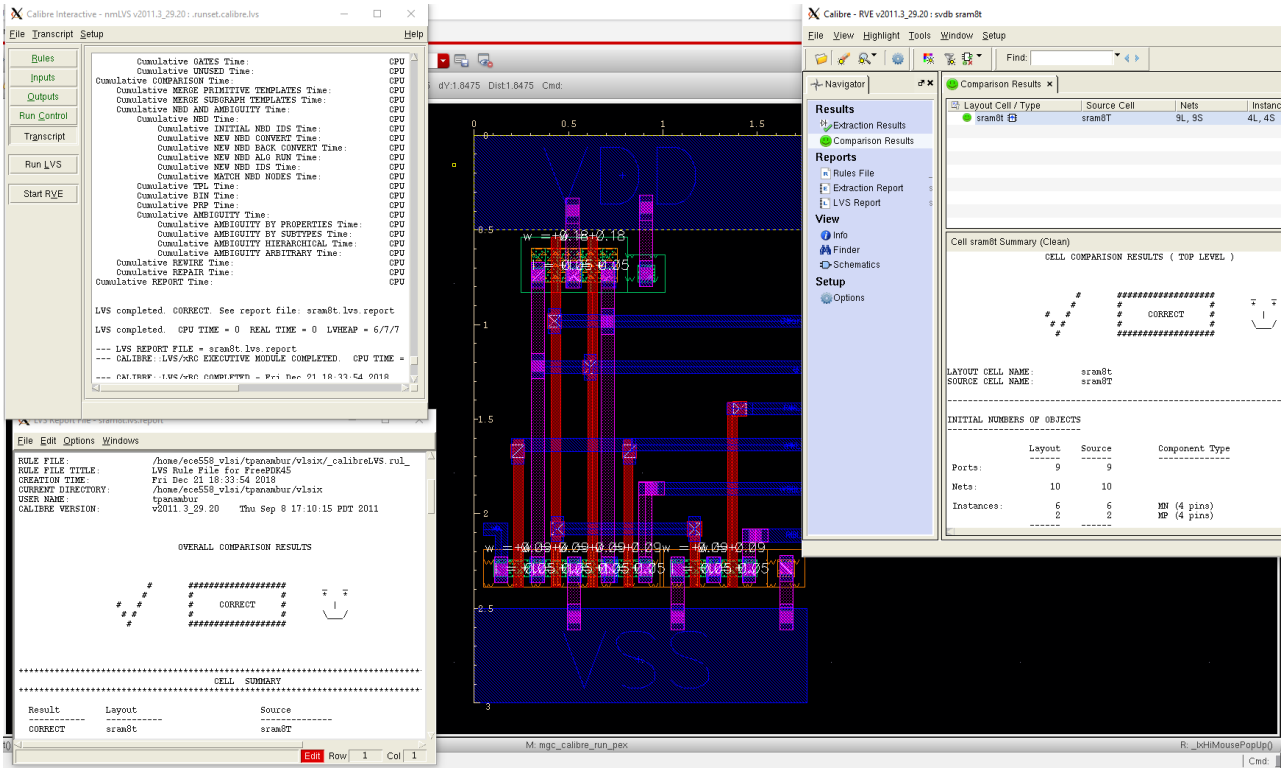

Fig 7: LVS Check of 8T SRAM in 45nm CMOS Technology

# 4) Design of 6T SRAM and 8T SRAM using 15nm FinFET Technology

Using the installed FinFET library from NCSU, FinFET designs are made in Cadence tool. The working of both the 6T and 8T SRAMS are like the working described for the CMOS technology for both Reading and Writing operations.

### a) Design of 6T SRAM using 15nm FinFET Technology

Table 3: Sizing of 6T SRAM

| Transistor | Width(nm) |
|---|---|
| M4, M5 | 180 |
| M3, M6 | 180 |
| M1, M2 | 460 |

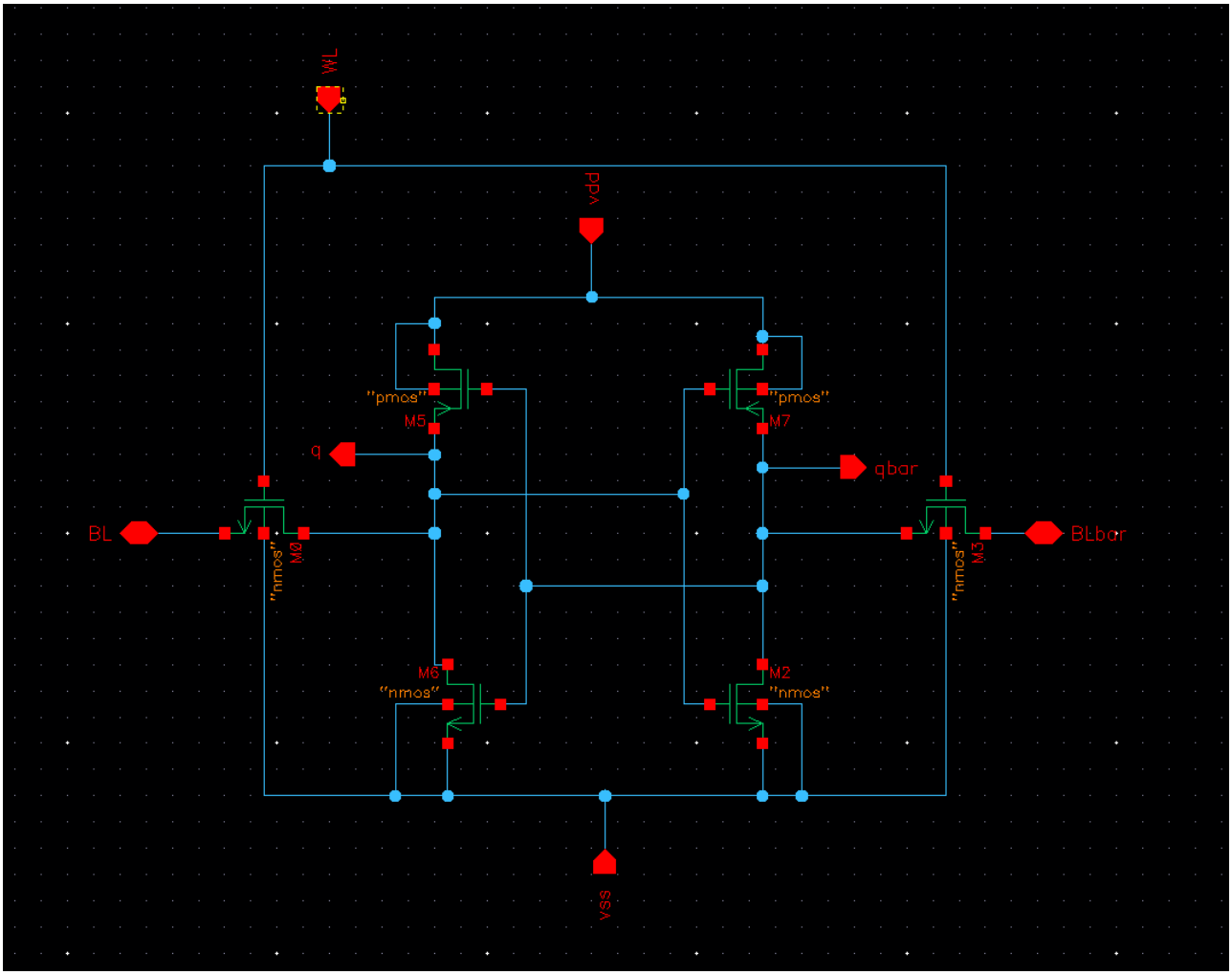


Fig 8: 15nm FinFET Schematic of 6T SRAM

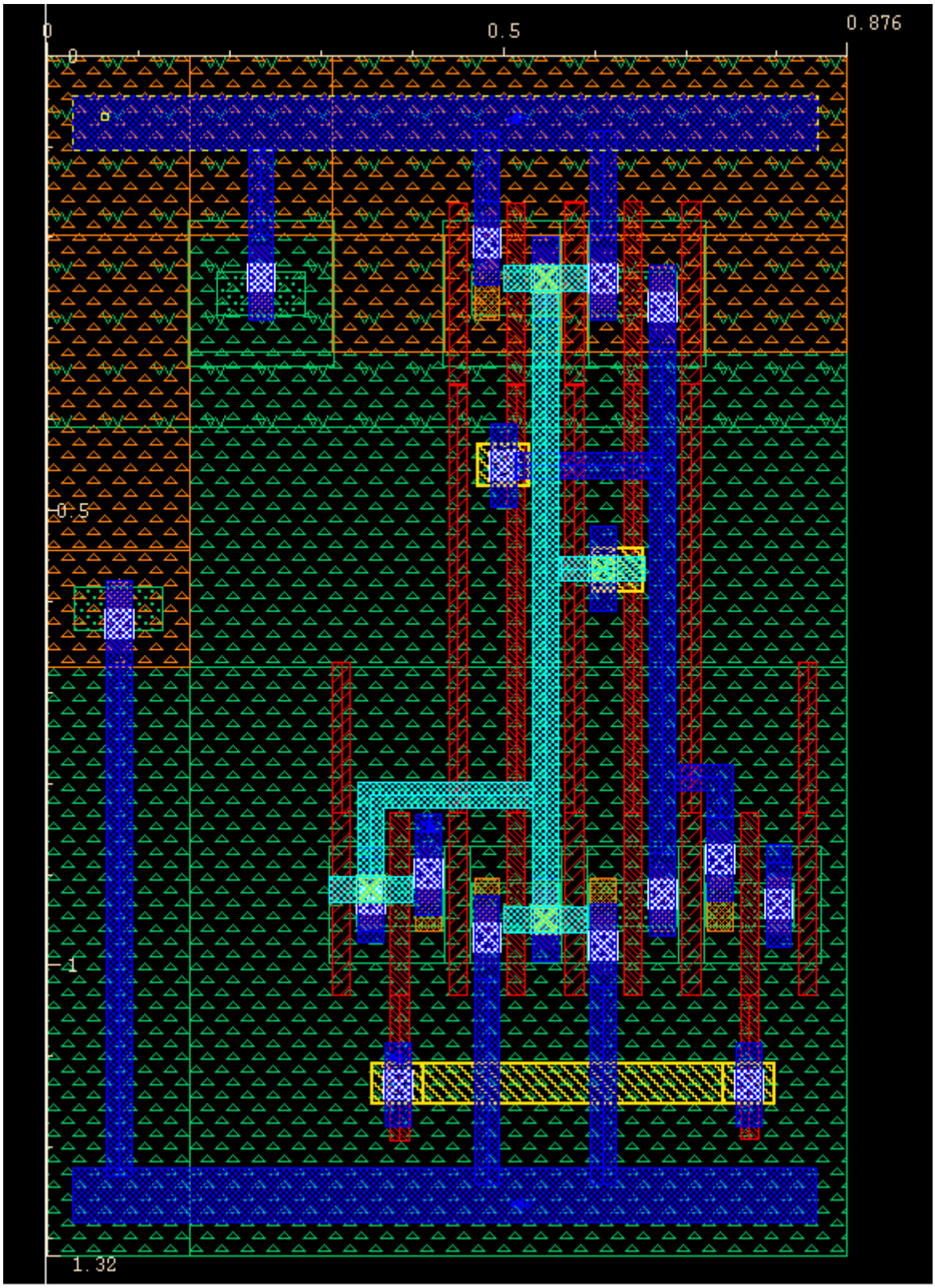


Fig 9: Layout of 6T SRAM in 15nm FinFET Technology

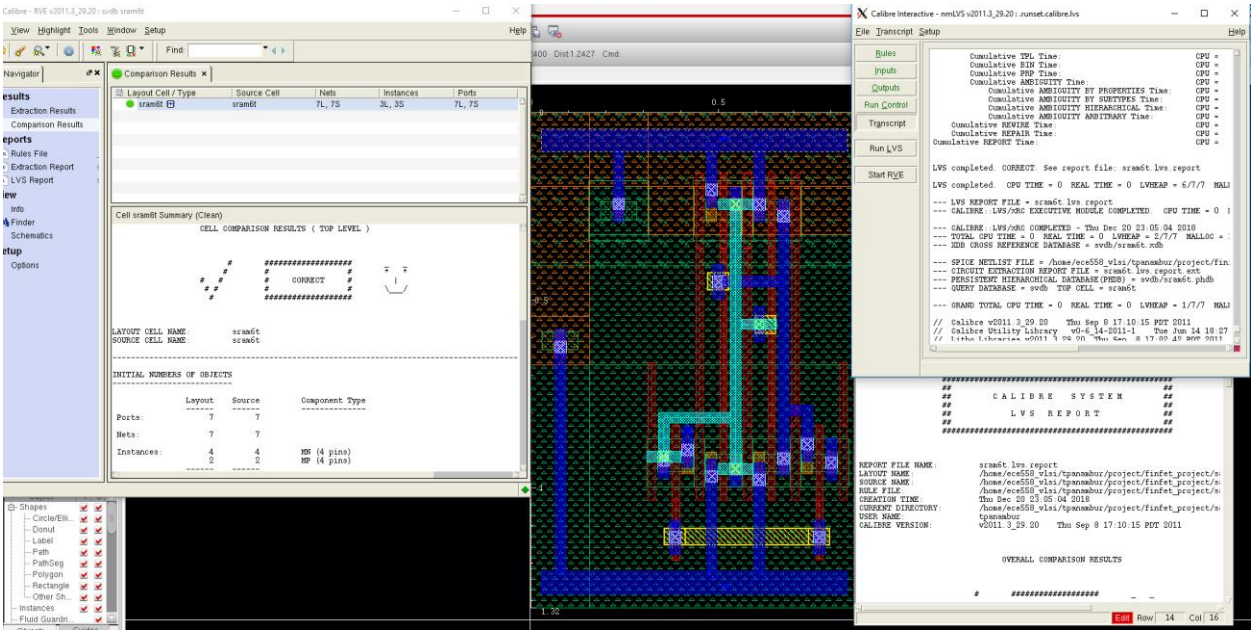

Fig 10: LVS Check of 6T SRAM in 15nm FinFET Technology

## b) Design of 8T SRAM using 15nm FinFET technology

Table 4: Sizing of 8T SRAM

| Transistor | Width(nm) |
|---|---|
| M3, M9 | 720 |
| M7, M5, M4 | 360 |
| M1, M8 | 90 |
| M6 | 45 |

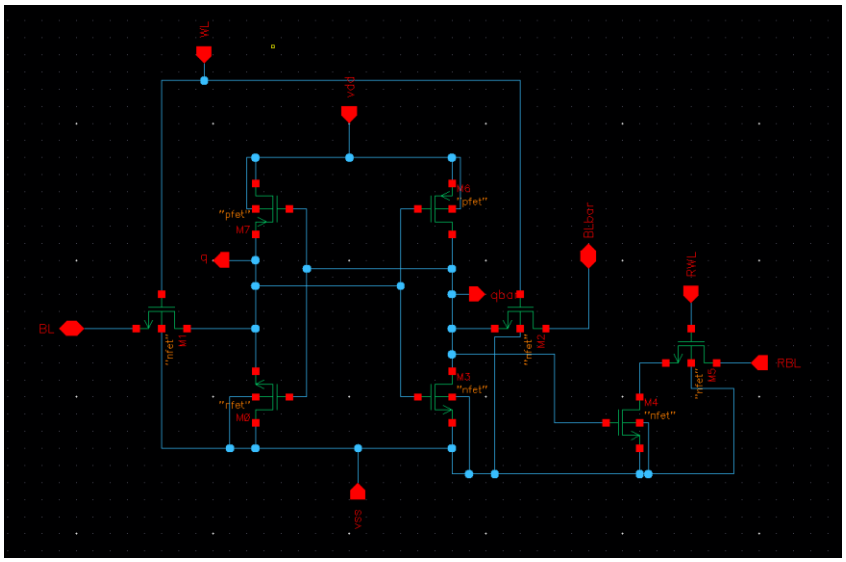


Fig 11: 15nm FinFET Schematic of 8T SRAM

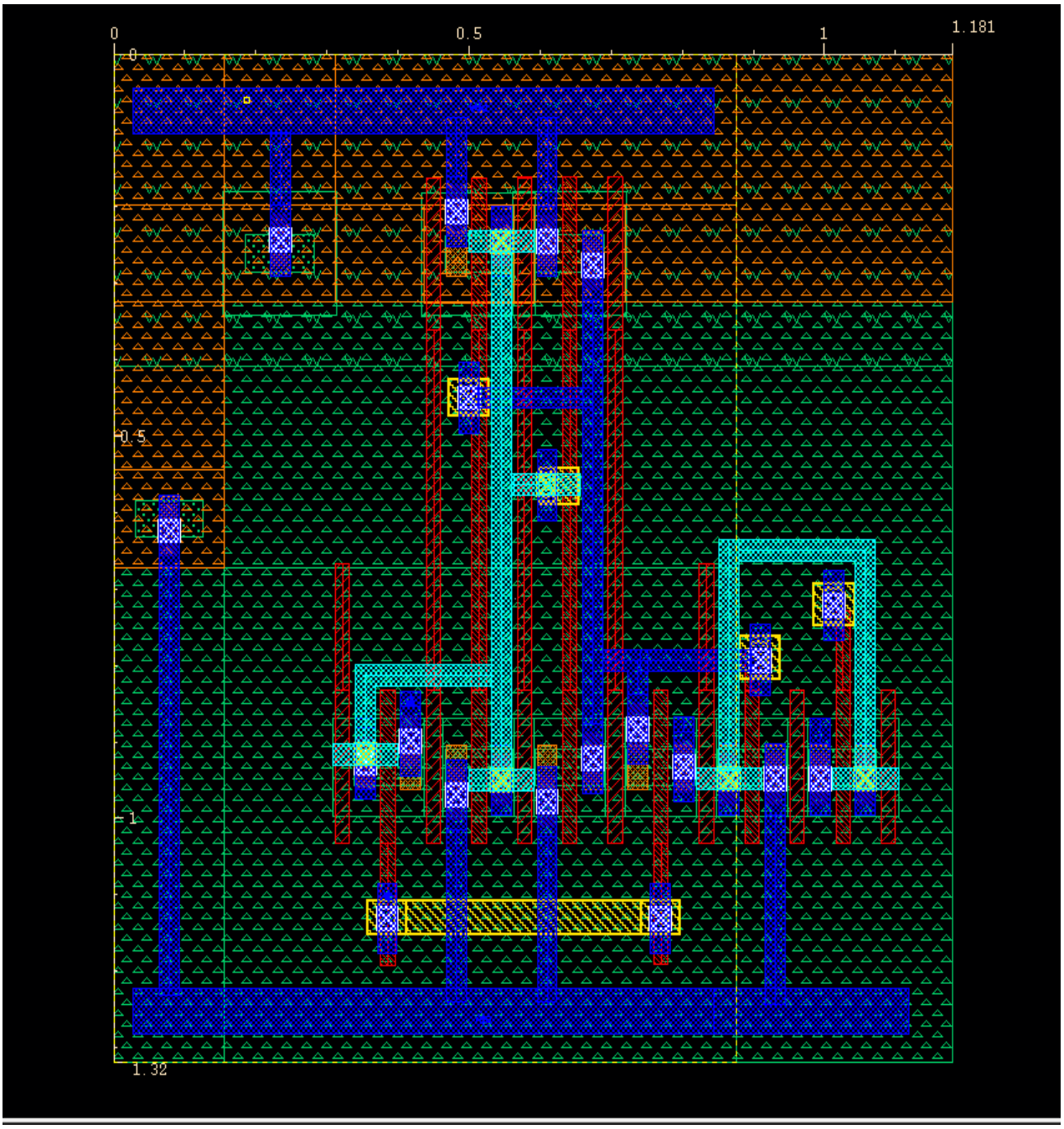


Fig 12: Layout of 8T SRAM in 15nm FinFET Technology

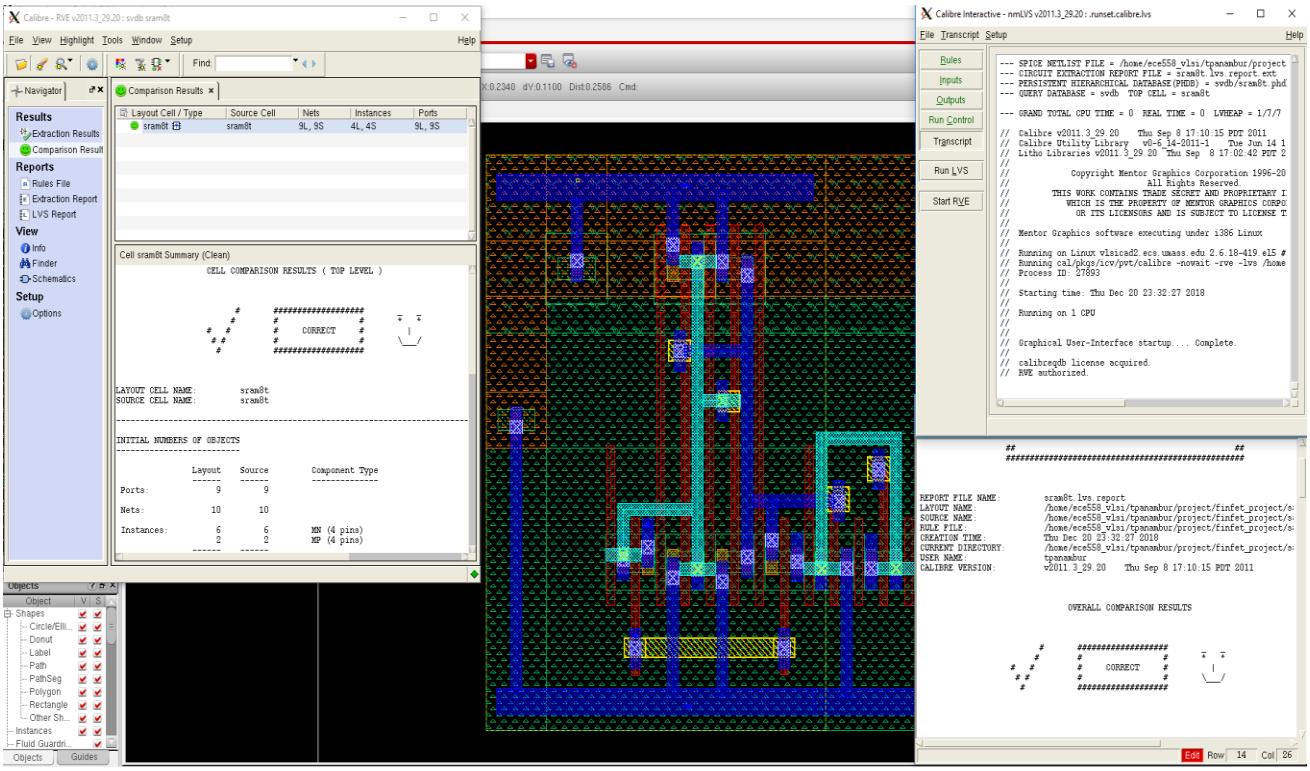


Fig 13: LVS Check of 8T SRAM in 15nm FinFET Technology

# CHAPTER 3: RESULTS AND ANALYSIS

The schematic and layouts are simulated using HSpice and CScope and the waveforms were observed. Various parameters like Write Time, Read Time, Dynamic Power and Static Power are calculated from the obtained waveforms.

## 1) 45nm CMOS TECHNOLOGY

Table 4: Comparison of Various parameters

| 45nm CMOS Technology | Write Time (ps) | Read Time (ps) | Dynamic Power (uW) | Static Power (uW) |
|---|---|---|---|---|
| 6T SRAM schematic | 23.941 | 21.32 | 242.26 | 98.86 |
| 6T SRAM Layout | 27.676 | 32.575 | 262.75 | 106.88 |
| 8T SRAM schematic | 10.496 | 6.6 | 715.26 | 134.5 |
| 8T SRAM Layout | 14.02 | 11.96 | 515.2 | 113.86 |

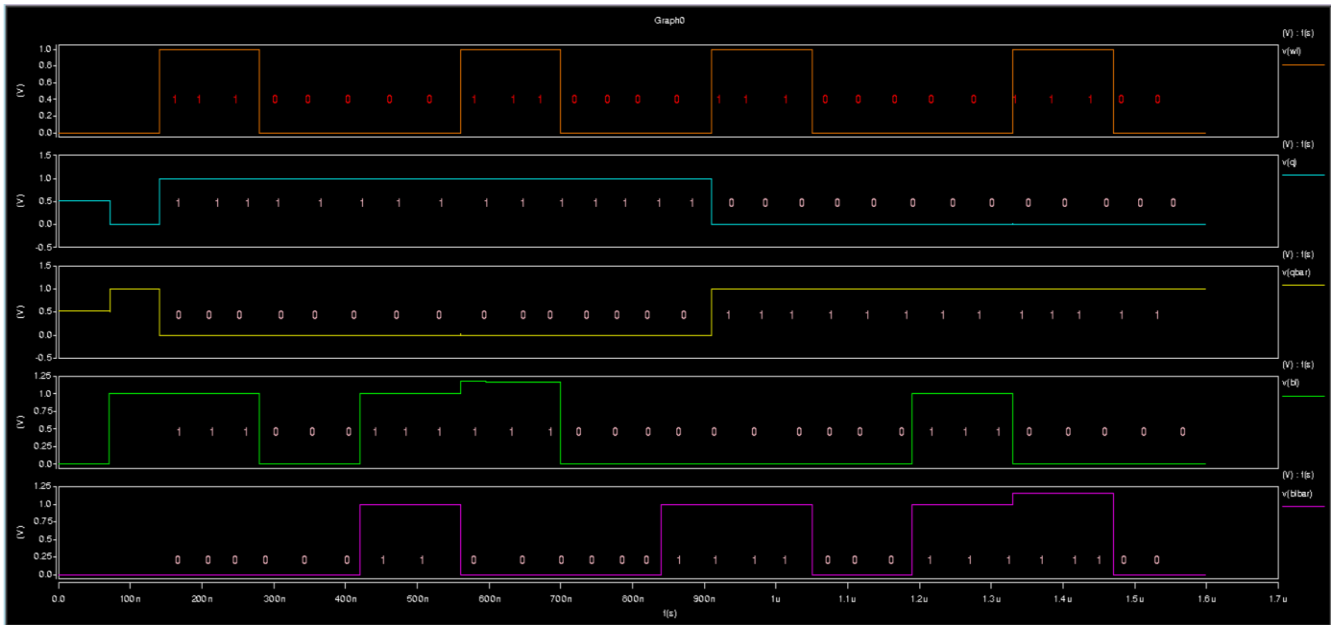


Fig 14: Waveforms of 6T SRAM Schematic in 45nm CMOS Technology

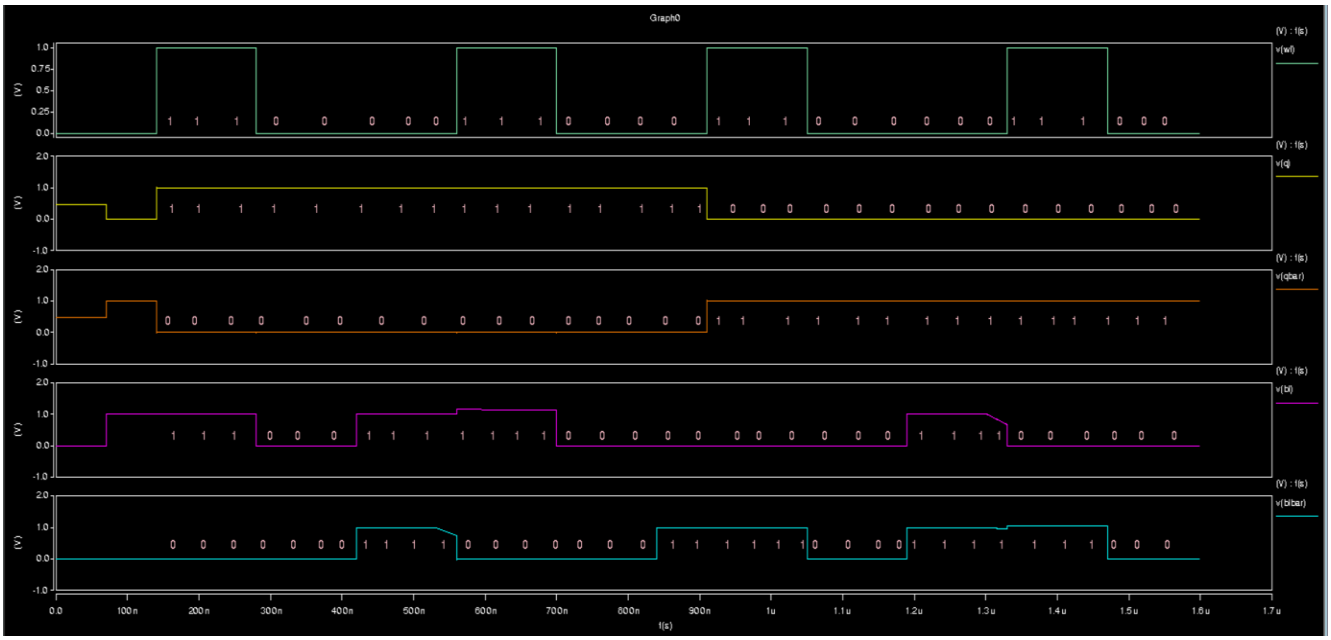


Fig 15: Waveforms of 6T SRAM Layout in 45nm CMOS Technology

It is seen in the above waveforms, during write operation WL=1, the data to be written is present at BL or BLbar and is passed onto the cross-coupled transistors and observed at Q or Qbar respectively. When WL=0, the access transistors (BL, BLbar) are precharged to '1'. During the read operation, WL='1'; BL and BLbar ='1'. The data is read and observed on BL and BLbar where BL reflects the data present at Q and BLbar reflects Qbar.

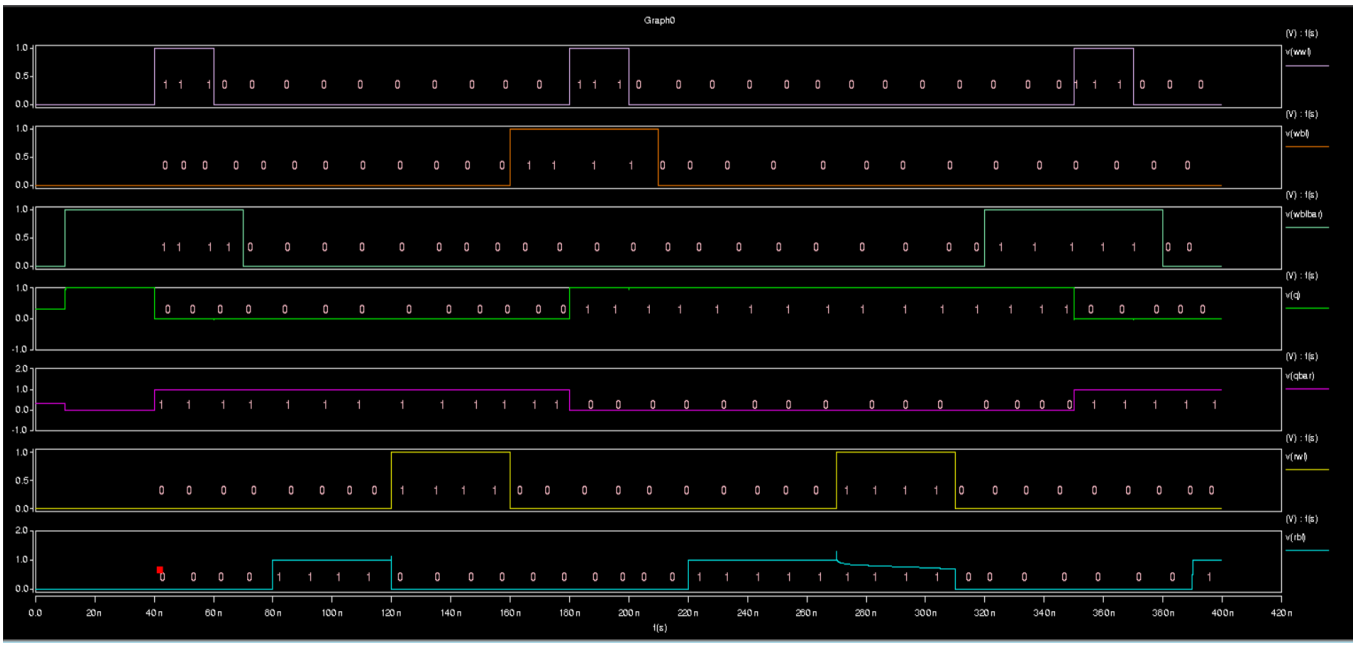


Fig 16: Waveforms of 8T SRAM Schematic in 45nm CMOS Technology

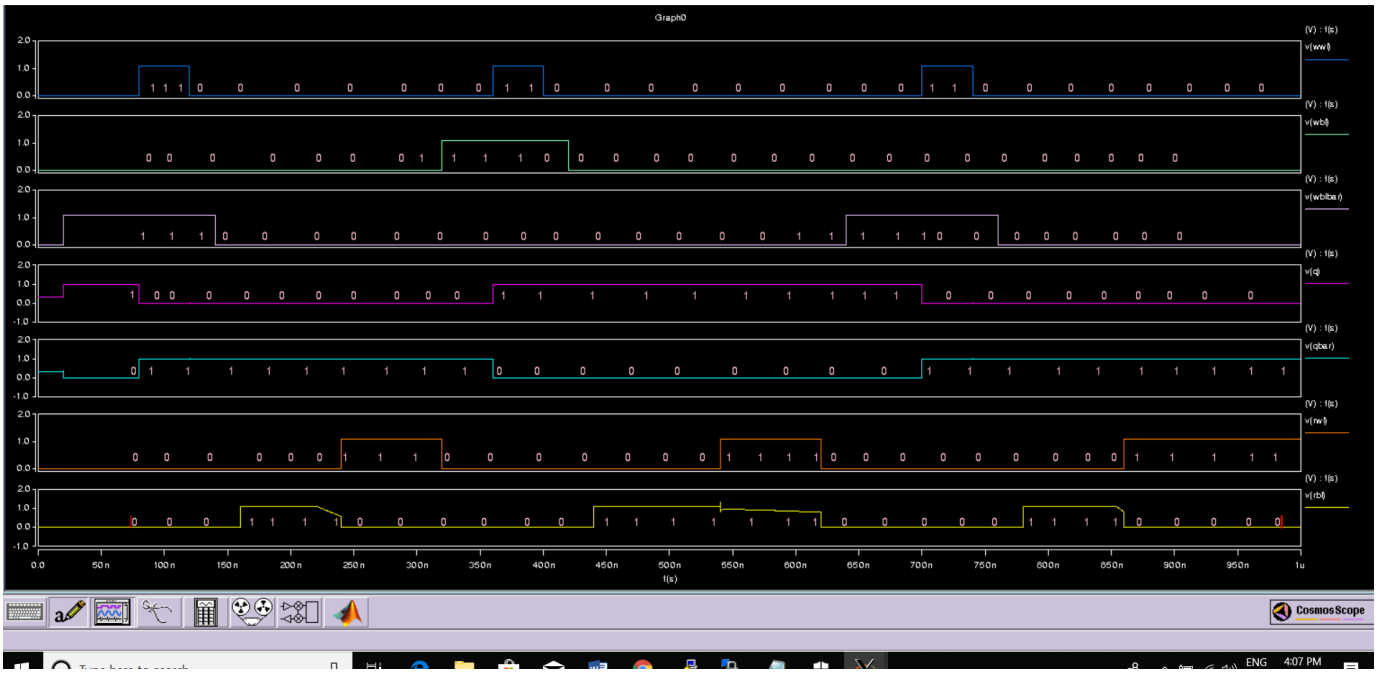


Fig 17: Waveforms of 8T SRAM Layout in 45nm CMOS Technology

As seen in the waveforms above, when WWL=1, the data to be written is passed through the access transistors onto ‘Q’ or ‘Qbar’. When WWL=’0’, the WBL and WBLbar are precharged to ‘1’. The data is read at RBL when RWL=’1’. RWL reflects the data present at Q.

## 2) 15nm FinFET TECHNOLOGY

The schematic and layouts are simulated using HSpice and CScope and the waveforms were observed. Various parameters like Write Time, Read Time, Dynamic Power and Static Power are calculated from the obtained waveforms. The working is same as explained for the CMOS Technology.

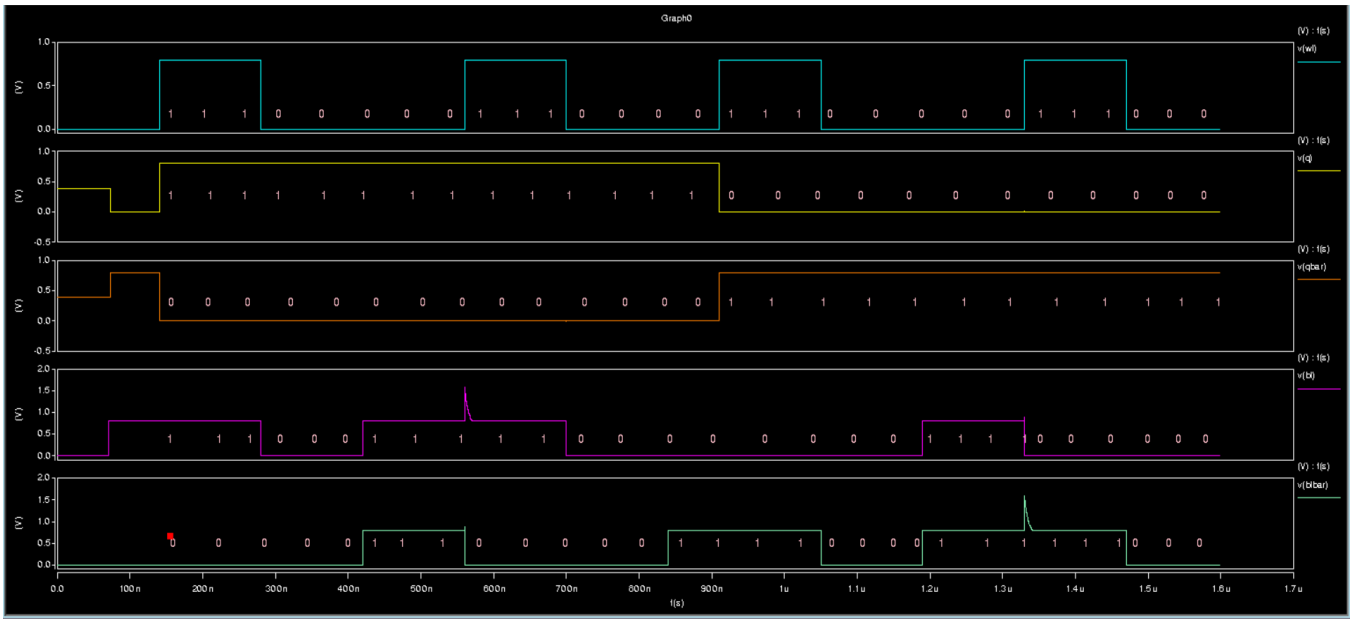


Fig 18: Waveforms of 6T SRAM Layout in 15nm FinFET Technology

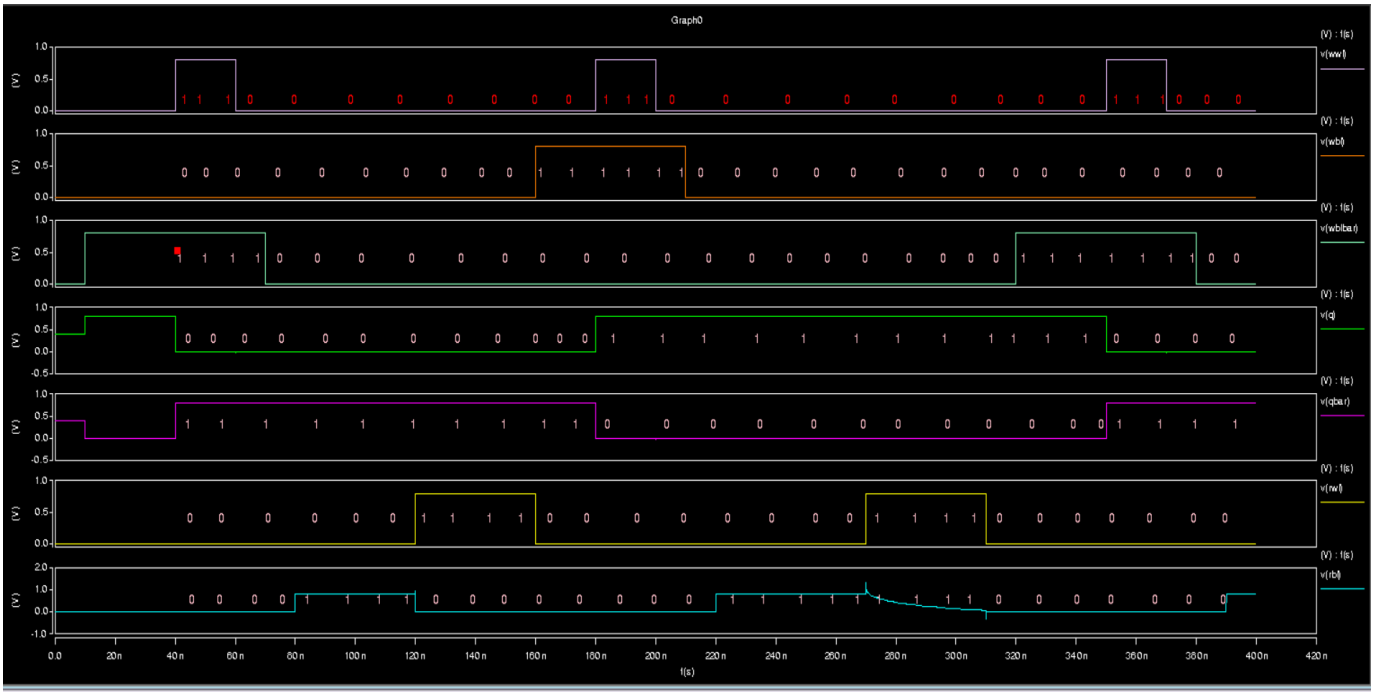


Fig 19: Waveforms of 8T SRAM Layout in 15nm FinFET Technology

Table 5: Comparison of Various Parameters

| 15nm FinFET Technology | Write Time (ps) | Read Time (ps) | Dynamic Power (uW) | Static Power (uW) |
|---|---|---|---|---|
| 6T SRAM Schematic | 17.361 | 14.245 | 143.2 | 43.6 |
| 8T SRAM Schematic | 5.070 | 4.567 | 192.1 | 56.65 |

# CHAPTER 4: REFLECTIONS

Table 6: Comparison of Area

| Technology | Component | Length (um), Width (um) | AREA ($um^2$) |
|---|---|---|---|
| 45 nm CMOS Technology | 6T SRAM | 1.7125, 3.0 | 5.1375 |
| | 8T SRAM | 1.7625, 3.0 | 5.2875 |
| 15 nm FinFET Technology | 6T SRAM | 0.876, 1.32 | 1.1563 |
| | 8T SRAM | 1.181, 1.32 | 1.5589 |

- We can calculate the length and width of the SRAMs from the Layout from which the Area can be calculated. We observe that the area of FinFET Technology is lesser than the CMOS Technology.
- The access and write time of 8T SRAM is lesser than the access and write time of 6T SRAM.
- The access and write time of both SRAMs are lesser in 15nm FinFET Technology than the 45nm CMOS Technology.
- The Dynamic and Static power of 8T SRAM is greater than the Dynamic and Static power of 6T SRAM.
- Both the Dynamic and Static Powers of 6T and 8T SRAMs in 15nm FinFET Technology are lesser than 45nm CMOS Technology.

# CHAPTER 5: FUTURE SCOPE

The Layout of both 6T and 8T SRAMs in 15nm FinFET Technology was DRC and LVS verified. But since the version of 'Rules' of FREEPDK15 is not supported by xRC Calibre, the PEX netlist could not be generated. Hence, if the corresponding version of Calibre is provided, the SRAMs read and write operation of Layout can be simulated and checked for correctness. The corresponding Error in log file is shown below.

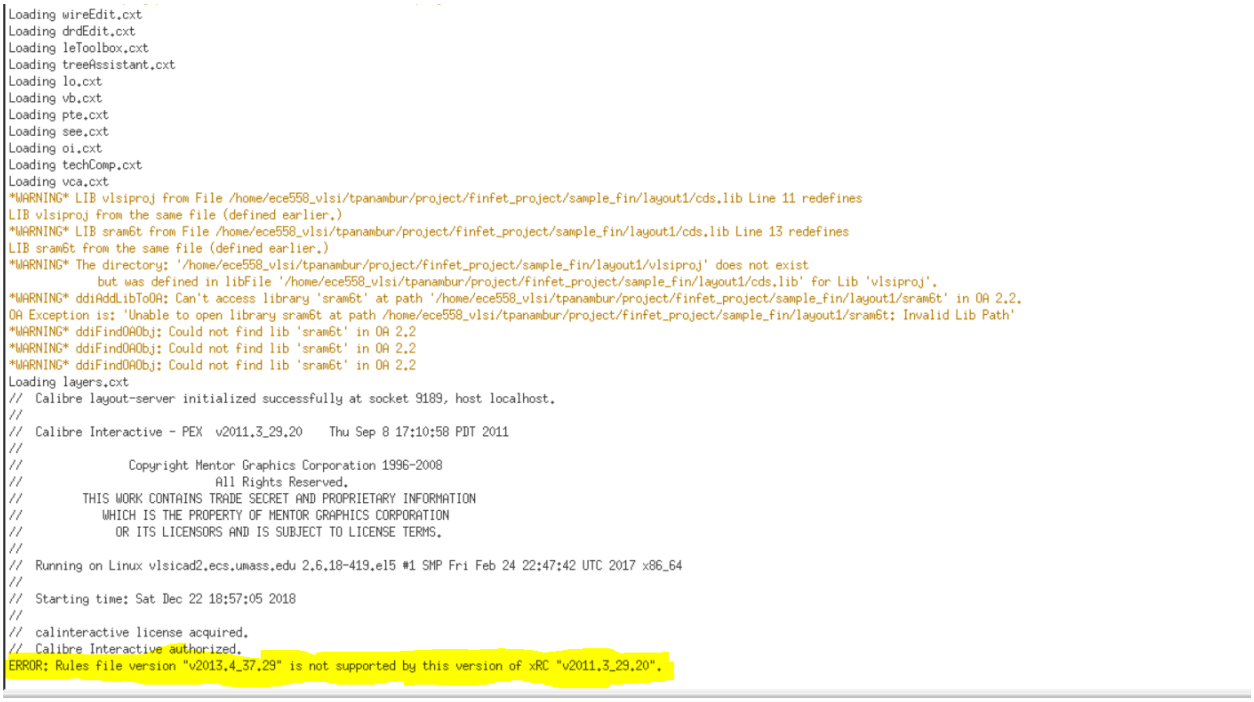


Fig 20: Error in Log File

# CHAPTER 6: REFERENCES

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