

# GOVERNMENT POLYTECHNIC, NAGPUR.

(An Autonomous Institute of Govt. of Maharashtra)

## COURSE CURRICULUM

<b>PROGRAMME</b>	<b>: DIPLOMA IN CM/IT</b>
<b>LEVEL NAME</b>	<b>: ENGINEERING SCIENCES AND TECHNICAL ARTS COURSES</b>
<b>COURSE CODE</b>	<b>: EC310E</b>
<b>COURSE TITLE</b>	<b>: DIGITAL TECHNIQUES</b>
<b>PREREQUISITE</b>	<b>: NIL</b>
<b>TEACHING SCHEME:</b>	<b>TH: 03; TU: 00; PR: 02(CLOCK HRs.)</b>
<b>TOTAL CREDITS</b>	<b>: 04 (1 TH/TU CREDIT = 1 CLOCK HR., 1 PR CREDIT = 2 CLOCK HR.)</b>
<b>TH. TEE</b>	<b>: 03 HRs</b>
<b>PR. TEE</b>	<b>: 02 HRs (Internal)</b>
<b>PT. EXAM</b>	<b>: 01 HR</b>

### ❖ **RATIONALE:**

This course forms the foundation of digital electronics to the students of Information Technology. It deals with learning the concepts of number Systems logic gates, combinational and sequential logic circuits. Now a day, many electronic systems are digitized. Hence, it is necessary to know the concept of design of a digital system. This course emphasizes on the combinational and sequential logic design.

### ❖ **COURSE OUTCOMES:**

**After completing this course students will be able to–**

1. Analyze digital logic circuits.
2. Perform conversion of different number system
3. Describe operation of various digital circuits like combinational circuits and sequential circuits.
4. Identify various pins of logic gate ICs.
5. Assemble various digital circuits like combinational circuits, Sequential circuits on breadboard.
6. Interpret the output of various combinational and sequential circuits.

❖ **COURSE DETAILS:****A. THEORY :**

Units	Specific Learning Outcomes (Cognitive Domain)	Topics and subtopics	Hrs.
1.Digital system and Number system	1. Define the terms analog and digital system. 2. Describe various logic levels. 3. Solve numerical on conversion of number system 4. Perform binary addition and subtraction.	1.1 Digital and Analog System, 1.2 Comparison of analog and digital system 1.3 Logic levels. 1.4 Binary, decimal, octal and hexadecimal number systems and their conversions. 1.5 Binary addition and subtraction. 1.6 Binary subtraction by using 1's & 2's complement	08
2.Logic gates & Boolean Algebra	1. Define logic gates. 2. Describe various logic gates. 3. Draw various logic gates using universal gates. 4. Solve various Boolean expressions. 5. State and prove De-Morgans theorem.	2.1 Definition and types of logic gates 2.2 Operating principle, truth table, 2.3 Boolean equation and symbol of NOT, OR, AND, NAND, NOR, EX-OR and EX-NOR gates. 2.3 Universal logic gates. Design of other logic gates using universal gates. 2.4 Basic laws of Boolean algebra.2.5De-Morgan's theorem.	08
3.Combinational circuits	1. Define min term and max term. 2. Describe K-map method of simplification 3. Design adder and subtractor using logic gates. 4. Design BCD to 7 segments decoder. 5. Design binary to gray and gray to binary converter.	3.1 Min-term and Max-term representation of logical function. 3.2 K-map minimization up to 4 variables. Don't care condition. 3.3 Binary half & full adder and binary half and full subtractor. 3.4 BCD to 7 Segment decoder. 3.5 Binary to gray and gray to binary conversion.	10
4.Multiplexers and Demultiplexers	1. State the need of multiplexers and de multiplexers. 2. Design of various multiplexers and de multiplexers using logic	4.1 Types, advantages, design steps and applications of multiplexers 2:1, 4:1, 8:1 and 16:1 multiplexers up to 16:1. 4.2 Multiplexers tree	08

	<p>gates.</p> <p>3. Design higher order multiplexers and demultiplexers using lower order.</p> <p>4. Compare multiplexers and demultiplexers.</p>	<p>4.3 Types advantages and application of demultiplexers 1:2, 1:4 and 1:8 demultiplexers.</p> <p>4.4 Demultiplexers tree upto 1 to 16 demultiplexers.</p> <p>4.5 Comparison between multiplexers and demultiplexers</p>	
5.Sequential Circuits	<p>1. Compare combinational and sequential systems.</p> <p>2. Compare latch and flip flop.</p> <p>3. Design of various flip flops.</p> <p>4. Describe Race around condition.</p> <p>5. List various applications of flip flops.</p>	<p>5.1 Combinational and sequential logic systems.</p> <p>5.2 Triggering Methods.</p> <p>5.3 RS latch using NOR gates and NAND gates.</p> <p>5.4 Clocked RS flip flop, J-K flipflop, D and T Flip Flop.</p> <p>5.5 Propagation delay time and race-around condition.</p> <p>5.6 MS J-K flip flop .</p> <p>5.7 Applications of flip flops</p>	08
6.Counters & Shift Registers	<p>1. Define Counters.</p> <p>2. Compare Asynchronous and Synchronous Counters.</p> <p>3. Define MOD N Counter.</p> <p>4. Define various shift registers.</p> <p>5. Design Bi-directional and circulating shift register.</p> <p>6. List various applications of shift registers.</p>	<p>1.1 Counters– Asynchronous (ripple) and synchronous counters. (Definition)</p> <p>1.2 Design of asynchronous counter (UP and DOWN) using JK or T flip flop (up to 4 bit)</p> <p>1.3 MOD – N Counter</p> <p>1.4 Ring Counter, Johnson Counter.</p> <p>1.5 Decade counter IC 7490.</p> <p>1.6 Definition and types of shift registers (SISO, SIPO, PISO, PIPO)</p> <p>1.7 Bi-directional shift register.</p> <p>1.8 Universal Shift Register.</p> <p>1.9 Application of shift register</p>	06
<b>Total Hrs.</b>			<b>48</b>

**B. LIST OF PRACTICALS/LABORATORY EXPERIENCES/ASSIGNMENTS:**

Practical's	Specific Learning Outcomes (Psychomotor Domain)	Units	Hrs.
1	Identify different pins of logic gate IC, apply input, measure output and relate it with the truth table. .	Logic gates & Boolean algebra	02
2	Assemble various basic gates using universal gates and relate it with the truth table.		02
3	Assemble the logic circuit using AND/OR/NOT logic gatesand NAND gates for verification of Boolean expression.		02
4	Assemble the logic circuit using AND/OR/NOT logic gatesand NAND gates for verification of De Morgan's Theorem		02
5	Identify different pins of 8:1 multiplexer IC, apply input, measure output and relate it with the truth table.	Multiplexers and Demultiplexers	02
6	Identify different pins of 1: 8 de multiplexer IC, apply input, measure output and relate it with the truth table.		02
7	Assemble the logic circuit for half adder and full adder using logic gates and verify its truth table.	Combinational Circuits	02
8	Identify different pins of S R flip flop IC, apply input, measure output and relate it with the truth table.	Sequential Circuits	02
9	Identify different pins of S R flip flop IC, apply input, measure output and relate it with the truth table.		02
10	Identify different pins of D flip flop IC, apply input, measure output and relate it with the truth table.		02
11	Identify different pins of T flip flop IC, apply input, measure output and relate it with the truth table.		02
12	Assemble 4 bit synchronous counter using Flip Flop, show its output on LED and relate it with the truth table.	Counters & shift registers	02
13	Assemble decade counter using IC 7490, show its output on LED and relate it with the truth table. .		02
14	Assemble 4 bit SISO register using flip flop, show its output on LED and relate it with the truth table. .		02
15	Assemble 4 bit PIPO register using flip flop, show its output on LED and relate it with the truth table.		02
Skill Assessment			02
Total Hrs			32

## ❖ SPECIFICATION TABLE FOR THEORY PAPER:

Unit No.	Units	Levels from Cognition Process Dimension			Total Marks
		R	U	A	
01	Digital System and Number System.	02(00)	04(04)	04(00)	10(04)
02	Logic Gates& Boolean Algebra	04(04)	04(04)	04(00)	12(08)
03	Combinational Circuits	06(02)	04(06)	04(00)	14(08)
04	Multiplexerand De multiplexers	02(00)	04(06)	04(00)	10(06)
05	Sequential Circuits	06(04)	06(00)	00(04)	12(08)
06	Counters&Shift registers	06(00)	06(00)	00(06)	12(06)
	<b>Total</b>	<b>26(10)</b>	<b>28(20)</b>	<b>16(10)</b>	<b>70 (40)</b>

R – Remember

U – Understand

A – Analyze / Apply

## ❖ QUESTION PAPER PROFILE FOR THEORY PAPER:

Q. No	Bit 1			Bit 2			Bit 3			Bit 4			Bit 5			Bit 6			option
	T	L	M	T	L	M	T	L	M	T	L	M	T	L	M	T	L	M	
01	1	R	2	2	R	2	3	R	2	4	R	2	2	R	2	3	R	2	5/7
	3	U	2																
02	1	A	4	2	A	4	3	R	4	1	U	4	2	U	4				3/5
03	1	U	4	2	U	4	3	U	4	2	R	4	5	R	4				3/5
04	3	A	4	4	U	4	4	A	4	3	U	4	5	A	4				3/5
05	5	R	6	5	U	6	4	U	6										2/3
06	6	R	6	6	U	6	6	A	6										2/3

T= Unit/Topic Number

L= Level of Question

M= Marks

R-Remember

U-Understand

A-Analyze/ Apply

❖ **ASSESSMENT AND EVALUATION SCHEME:**

	What		To Whom	Frequency	Max Marks	Min Marks	Evidence Collected	Course Outcomes
Direct Assessment Theory	CA (Continuous Assessment)	Progressive Test (PT)	Students	Two PT (average of two tests will be computed)	20	--	Test Answer Sheets	1, 2, 3
		Assignments		Continuous	10	--	Assignment Book / Sheet	1, 2, 3
	TEE (Term End Examination)	End Exam	Students	End Of the Course	70	28	Theory Answer Sheets	1, 2, 3
				Total	100	40		
Direct Assessment Practical	CA (Continuous Assessment)	Skill Assessment	Students	Continuous	20	--	Rubrics & Assessment Sheets	4,5,6
		Journal Writing		Continuous	05	--	Journal	4,5,6
				TOTAL	25	10		
	TEE (Term End Examination)	End Exam	Students	End Of the Course	50	20	Rubrics &Practical Answer Sheets	4,5,6
Indirect Assessment	Student Feedback on course		Students	After First Progressive Test	Student Feedback Form		1, 2, 3, 4,5,6	
	End Of Course			End Of The Course	Questionnaires			

❖ **SCHEME OF PRACTICAL EVALUATION:**

S.N.	Description	Max. Marks
1	Drawing circuit diagram, truth table, writing procedure etc.	10
2	Identifying various pins of IC	10
3	Performance on bread board	20
4	Viva voce	10
	<b>TOTAL</b>	<b>50</b>

❖ **MAPPING COURSE OUTCOMES WITH PROGRAM OUTCOMES:**

Course Outcomes (COs)	Program Outcomes (POs)										PSOs	
	1	2	3	4	5	6	7	8	9	10	1	2
1	-	3	-	-	-	-	-	-	-	3	-	-
2	-	3	-	-	-	-	-	-	-	3	-	-
3	-	3	-	-	-	-	-	-	-	3	-	-
4	-	3	2	2	-	-	2	2	-	3	-	-
5	-	3	2	2	-	-	2	2	-	3	-	-
6	-	3	2	2	-	-	2	2	-	3	-	-

1: Slight (Low)    2: Moderate (Medium)    3: Substantial (High)

❖ **REFERENCE & TEXT BOOKS:**

S.N.	Title	Author, Publisher, Edition and Year Of publication	ISBN Number
1.	Digital Integrated Electronics	H. Taub and D.Schilling. McGraw-Hill, 2008, Second Edition	ISBN 10: 0070857881 ISBN 13: 9780070857889
2.	Digital Principles and Applications	Malvino Leach. McGraw-Hill, Seventh Edition, 2011	ISBN 10: 0070398836 ISBN 13: 9780070398832
3.	Digital electronics- R.P.Jain.	R.P.Jain. McGraw-Hill, Third Edition, 2003	SBN 10: 0070669112 ISBN 13: 9780070669116
4.	CMOS/TTL: A user's guide with projects	Carr, Joseph J. Tab Books; 1st edition (1984)	SBN 10: 0830616500 ISBN 13: 9780830616503

❖ **E-REFERENCES:**

- [www.electrical4u.com/digital-electronics](http://www.electrical4u.com/digital-electronics) , assessed on 20<sup>th</sup> January 2016
- <http://nptel.ac.in/courses/108108076/1> , assessed on 20<sup>th</sup> January 2016
- <http://www.electrical4u.com> , assessed on 20<sup>th</sup> January 2016
- <https://www.youtube.com/watch?v=A9KSGAnjo2U>, assessed on 20<sup>th</sup> January 2016

❖ **LIST OF MAJOR EQUIPMENTS/INSTRUMENTS WITH SPECIFICATION**

1. Digital Multi-Meter.
2. Logic Gates ICs (7400,7402,7404,7408,7432,7486)
3. Multiplexer and De multiplexer IC(74150,74151,74138,74139)
4. Flip Flops ICs (7472,7474,74H71,74L71)
5. Breadboard and LEDs.
6. Power Supply

❖ **LIST OF EXPERTS & TEACHERS WHO CONTRIBUTED FOR THIS CURRICULUM:**

S.N.	Name	Designation	Institute / Industry
1.	Prof. A A Ali	HOD in Electronics and Telecommunication Engg. (II Shift)	Government Polytechnic, Nagpur
2.	Prof. V M Sakode	Lecturer in Electronics and Telecommunication Engg.	Government Polytechnic, Nagpur
3	Mr. Sandip V Darwhekar	Director	Beta computronics Pvt Ltd, Nagpur
4	Mrs Gajala Ali	Head of Electronics Engg	Anjuman Polytechnic , Nagpur
5	Mr. S. M. Kale	Lecturer, Electronics Engg.	Government Polytechnic, Gadchiroli.

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 (Member Secretary PBOS)

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 (Chairman PBOS)