Hardware Design Methodology

Assignment 2 & 3 (10 marks each)

Deadline: 28th March 2022

This assignment needs to be performed using LT-SPICE. Please adhere to the deadlines strictly.

Note:

* For SPICE simulation kindly use 180 nm technology library by PTM. Details of the model file can be found here: http://ptm.asu.edu/modelcard/180nm_bulk.txt

*For SPICE-based assignment, use output load capacitance to be **500 fF** in your design (if not stated). **Take VDD = 1.8 V.**

* It is necessary to show the calculations/ steps done to design the circuit.

* Schematic needs to be neat and clean. It should be labeled properly.

* Copying the report/ plagiarism shall result in 0 marks

* All the necessary simulation snapshots need to be included with white background. Labels should be visible

* A group size of a maximum of 3 students is permissible

Statement 1. (8+2 marks)

Implement TSPC positive edge-triggered D Flip Flop (Follow the Textbook for the design). **Compute its setup and hold time. Optimize its power delay product.** Compute the maximum operating frequency.

Statement 2. (8+2 marks)

Implement a Band Gap reference Circuit, with **Vref = 1.2 V, Temp. coefficient < = 200 ppm/^{0}C** (for the worst case). **You can use any topology of your choice.** Also, show Vout *vs.* VDD and minimize the effect of supply voltage variation in output voltage.