# ASSIGNMENT- 2 AND 3

# HARDWARE DESIGN METHODOLOGY

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# Question

**This assignment needs to be performed using LT-SPICE. Please adhere to the deadlines strictly.**

**Note:**

* For SPICE simulation kindly use 180 nm technology library by PTM. Details of the model file can be found here: http://ptm.asu.edu/modelcard/180nm_bulk.txt

*For SPICE-based assignment, use output load capacitance to be **500 fF** in your design (if not stated).

**Take VDD = 1.8 V.**

* It is necessary to show the calculations/ steps done to design the circuit.

* Schematic needs to be neat and clean. It should be labeled properly.

* Copying the report/ plagiarism shall result in 0 marks

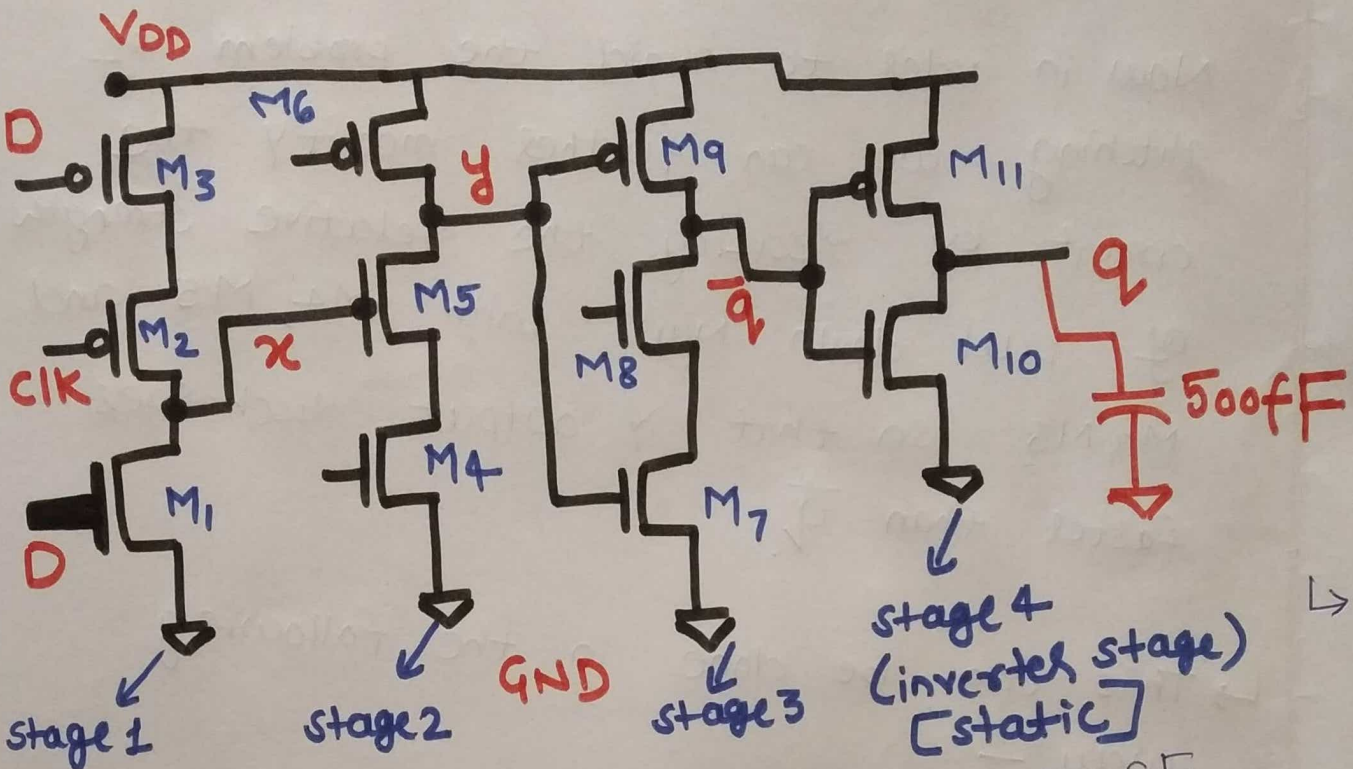
* All the necessary simulation snapshots need to be included with white background. Labels should be visible

* A group size of a maximum of 3 students is permissible

**Statement 1.** (8+2 marks)

Implement TSPC positive edge-triggered D Flip Flop (Follow the Textbook for the design). **Compute its setup and hold time. Optimize its power delay product.** Compute the maximum operating frequency.

⇒ For optimizing the circuit completely let us calculate and apply modified values of (W/L) for each of the Tx.




as we have been given a $C_{load} = 500fF$

let us optimize the given circuit to have stage ratio of 2 with $l_n/l_p = 4/1$

(using 180nm modle file)

**Part (1) → optimization for (W/L)**

⇒ Stage 4 -

$$\frac{C_L}{C_4} = 2 = \frac{500}{C_4} \Rightarrow \boxed{C_4 = 250fF}$$

but $C_4 = C_{gate} = WLC_{ox}$

where $L = 180nm$

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{C_{ox}}$$

$$\therefore LC_{ox} = 180\times10^{-9} \times \frac{8.85\times3.97\times10^{-12}}{4\times10^{-9}}$$

$\therefore \quad L C_{ox} = 1581.052 \times 10^{-12}$

$\Rightarrow \quad \omega_T L C_{ox} = 250 \times 10^{-15}$

but $\because \quad \mu_n / \mu_p = 4/1$

$\therefore \quad \omega_p = 4 \times \omega_n$

$\therefore \quad \omega_T = \omega_n + \omega_p = \omega_n + 4\omega_n$

$= 5\omega_n$

$\therefore \quad 5\omega_n \times 1581.052 \times 10^{-12} = 250 \times 10^{-15}$

$\therefore \quad \boxed{\omega_n = 31.6\ \mu} \quad (M_{10})$

and $\omega_p = 4 \times 31.6\ \mu$

$\therefore \quad \boxed{\omega_p = 126.4\ \mu} \quad (M_{11})$

→ Stage 3 –

$\frac{C_4}{C_3} = 2 \Rightarrow C_3 = \frac{C_4}{2} = \frac{250}{2} = 125f$

$\therefore \quad \boxed{C_3 = 125fF}$

$\Rightarrow \quad 5\omega_n L C_{ox} = 125 \times 10^{-15}$

$5 \times \omega_n \times 1581.052 \times 10^{-12} = 125 \times 10^{-15}$

$\therefore \quad \boxed{\omega_n = 15.81\ \mu} \quad (M_7, M_8)$

and $\omega_p = 4 \times 15.81\ \mu$

$\therefore \quad \boxed{\omega_p = 63.24\ \mu} \quad (M_9)$

↳ stage 2 – $\frac{C_3}{C_2} = 2 \Rightarrow \frac{125}{2} = C_2$

$\therefore \boxed{C_2 = 62.5fF}$

$\Rightarrow 5\omega_n \times 1581.052 \times 10^{-12} = 62.5 \times 10^{-15}$

$\therefore \boxed{\omega_n = 7.9 \text{ rad}}$ (M4, M5)

and $\omega_p = 4 \times 7.9 \text{ rad}$

$\therefore \boxed{\omega_p = 31.6 \text{ rad}}$ (M6)

↳ stage 1 – $\frac{C_2}{C_1} = 2 \Rightarrow C_1 = \frac{C_2}{2} = \frac{62.5}{2}$

$\therefore \boxed{C_1 = 31.25fF}$

$\Rightarrow 5 \times \omega_n \times (C_{OX}) = 31.25 \times 10^{-15}$

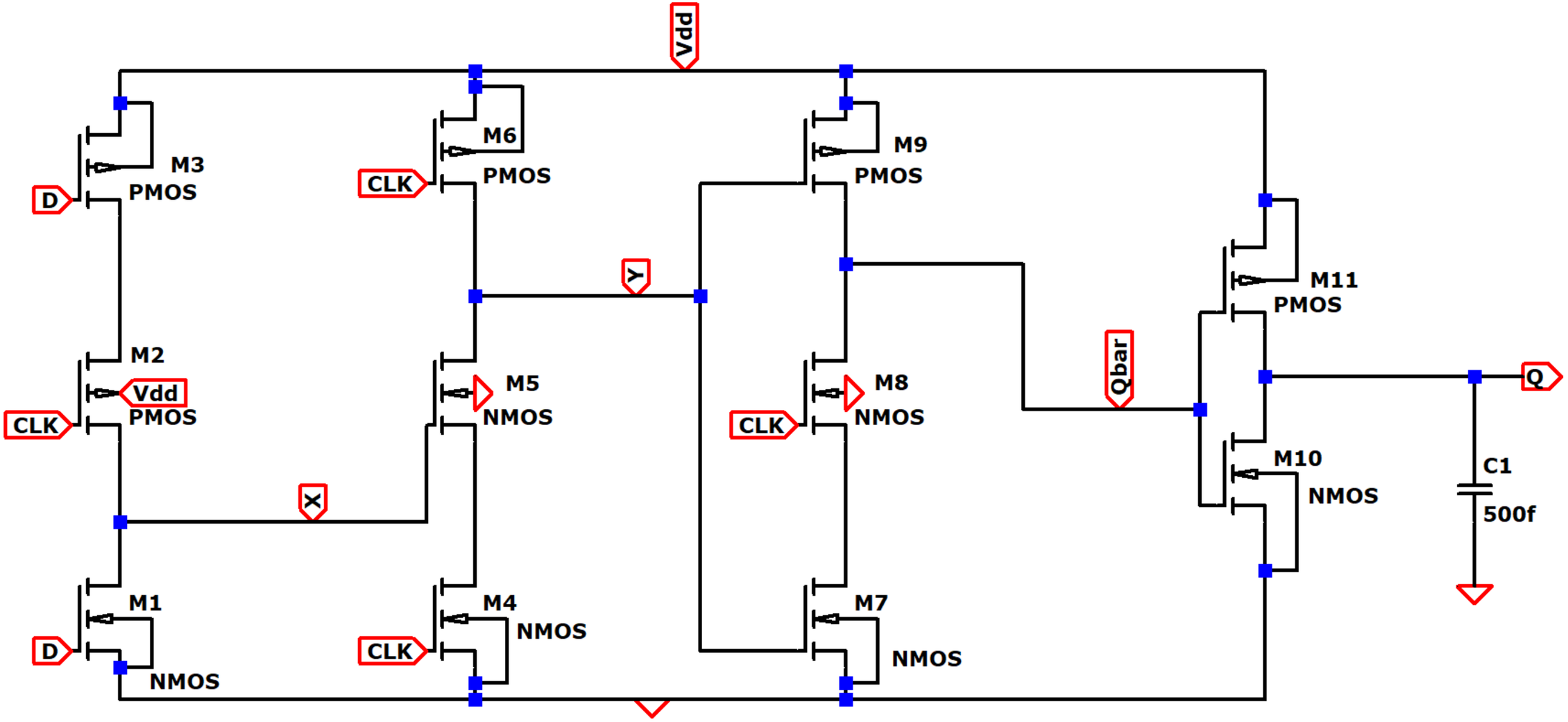
$5\omega_n \times 1581.052 \times 10^{-12} = 31.25 \times 10^{-15}$

$\therefore \boxed{\omega_n = 3.95 \text{ rad}}$ (M1)

and $\omega_p = 4 \times 3.95 \text{ rad}$

$\therefore \boxed{\omega_p = 15.8 \text{ rad}}$ (M2, M3)

# Optimized Circuit



# Optimized circuit Netlist

```
M9 Vdd Y Qbar Vdd PMOS l=180nm w=63.24u
M8 Qbar CLK 3 0 NMOS l=180nm w=7.905u
M7 3 Y 0 0 NMOS l=180nm w=7.905u
M6 Vdd CLK Y Vdd PMOS l=180nm w=31.6u
M5 Y X 2 0 NMOS l=180nm w=15.8u
M4 2 CLK 0 0 NMOS l=180nm w=15.8u
M11 Vdd Qbar Q Vdd PMOS l=180nm w=126.5u
M10 Q Qbar 0 0 NMOS l=180nm w=31.625u
M3 Vdd D 1 Vdd PMOS l=180nm w=15.8u
M2 1 CLK X Vdd PMOS l=180nm w=15.8u
M1 X D 0 0 NMOS l=180nm w=3.95u
V1 Vdd 0 1.8
V2 CLK 0 PULSE(0 1.8 0 0.01n 0.01n 7n 14n)
V3 D 0 PULSE(0 1.8 7.077n 0.01n 0.01n 7n 14n)
C1 Q 0 500f
.model NMOS NMOS
.model PMOS PMOS

* PSPICE TSMC180nm.lib file  RWN  04/18/2010
* library  file for transistor parameters for TMSC 0.18 micron process
* uses BIM parameters added 01/15/98
* can configure and attach to Nbreak and Pbreak transistors in PSpice
****
*****************  180nm TSMC parameters  *************
*T14B SPICE BSIM3 VERSION 3.1 PARAMETERS
* downloaded from MOSIS 04/18/10
*http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/
* tsmc-018/t92y_mm_non_epi_thk_mtl_params.txt
*SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8
* DATE: Jun  8/01
* LOT: T14B                  WAF: 06
* Temperature_parameters=Default
*$
.MODEL TSMC180nmN NMOS (                                LEVEL   = 7
+VERSION = 3.1            TNOM    = 27              TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 2.3549E17       VTH0    = 0.354505
+K1      = 0.5733393      K2      = 3.177172E-3     K3      = 27.3563303
+K3B     = -10            W0      = 2.341477E-5     NLX     = 1.906617E-7
+DVT0W   = 0              DVT1W   = 0               DVT2W   = 0
+DVT0    = 1.6751718      DVT1    = 0.4282625       DVT2    = 0.036004
+U0      = 327.3736992    UA      = -4.52726E-11    UB      = 4.46532E-19
```

## ↳ Part (2) - optimization for glitches

Now in order to avoid the problem of glitching we can further modify the circuit by resizing the relative strength of pull down N/W with M4, M5 and M7, M8 so that Y output discharges faster than $\overline{q}$.

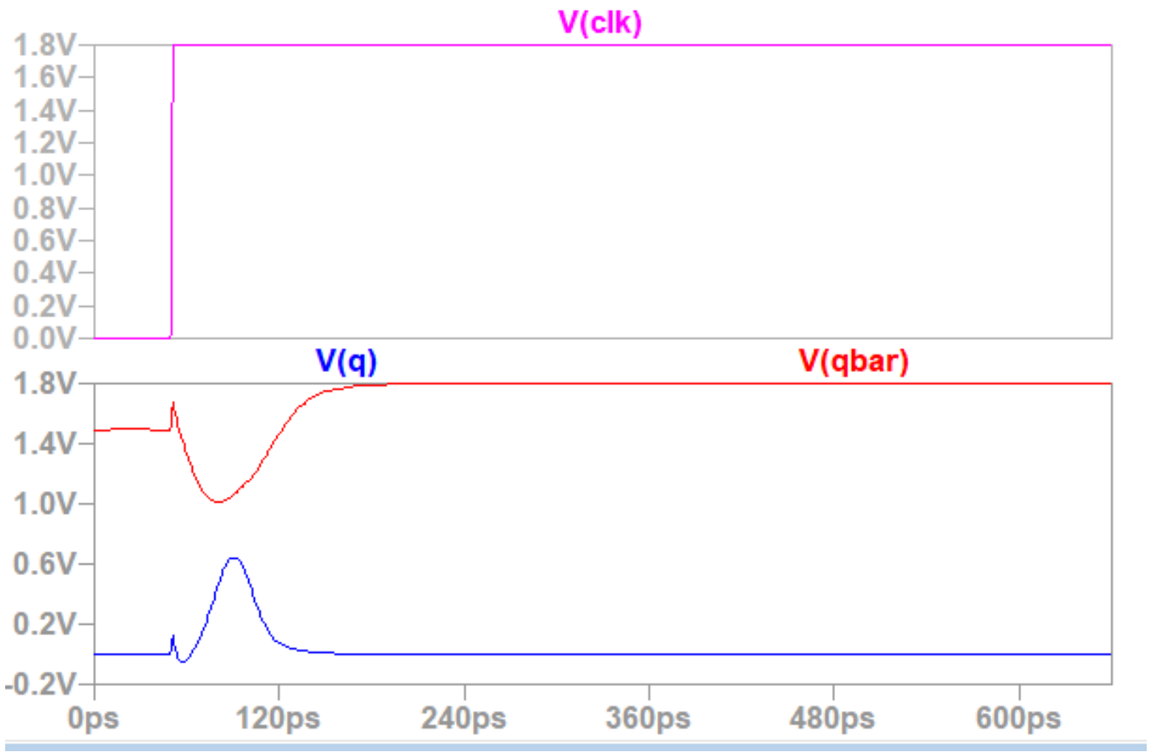
↳ This can be done in the following way -

$$M_4, M_5 = 2 \times (W/L)_{4,5} = 15.8 \text{ um}$$

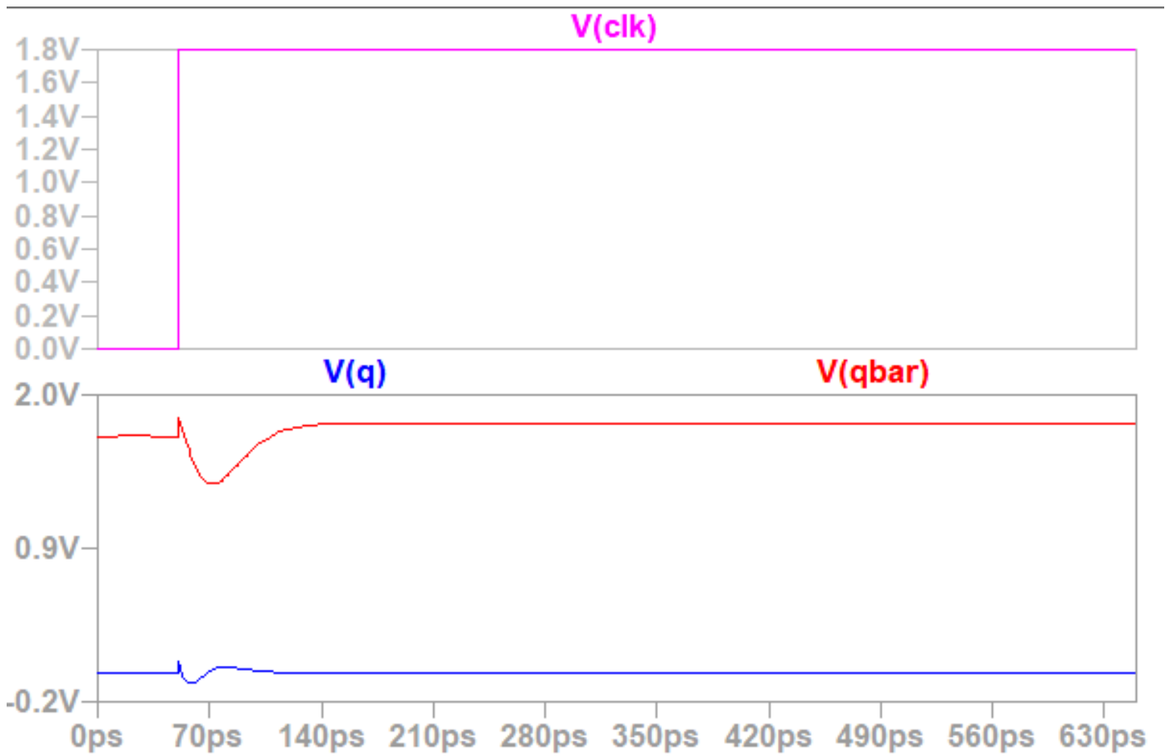
$$M_7, M_8 = \frac{1}{2} \times (W/L)_{7,8} = \frac{15.8}{2} \text{ um}$$

$$= 7.905 \text{ um}$$

# optimization for glitches

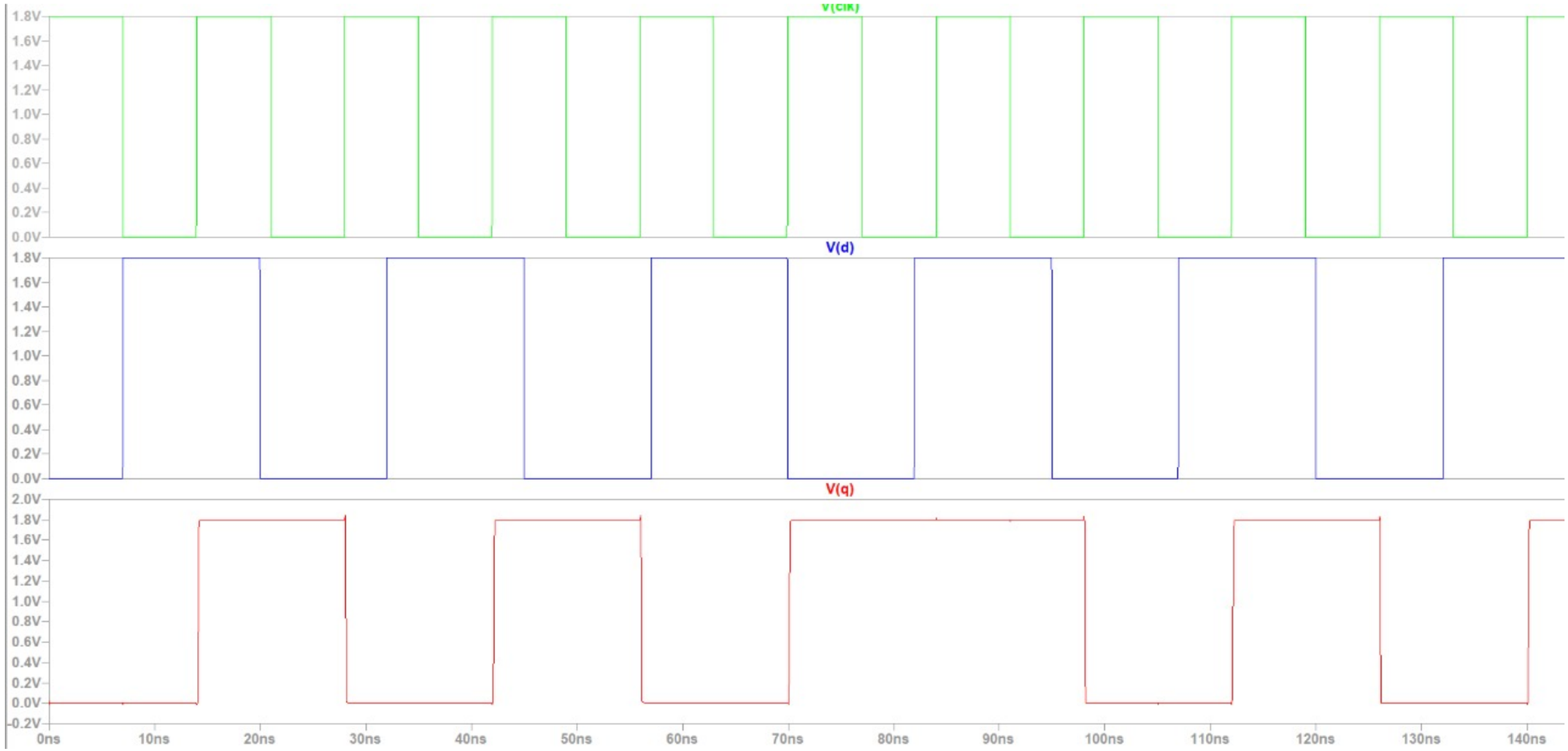



Before




After

# optimized Output



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## Calculations for STA -

The input must be kept stable before and after the rising edge of the CLK.

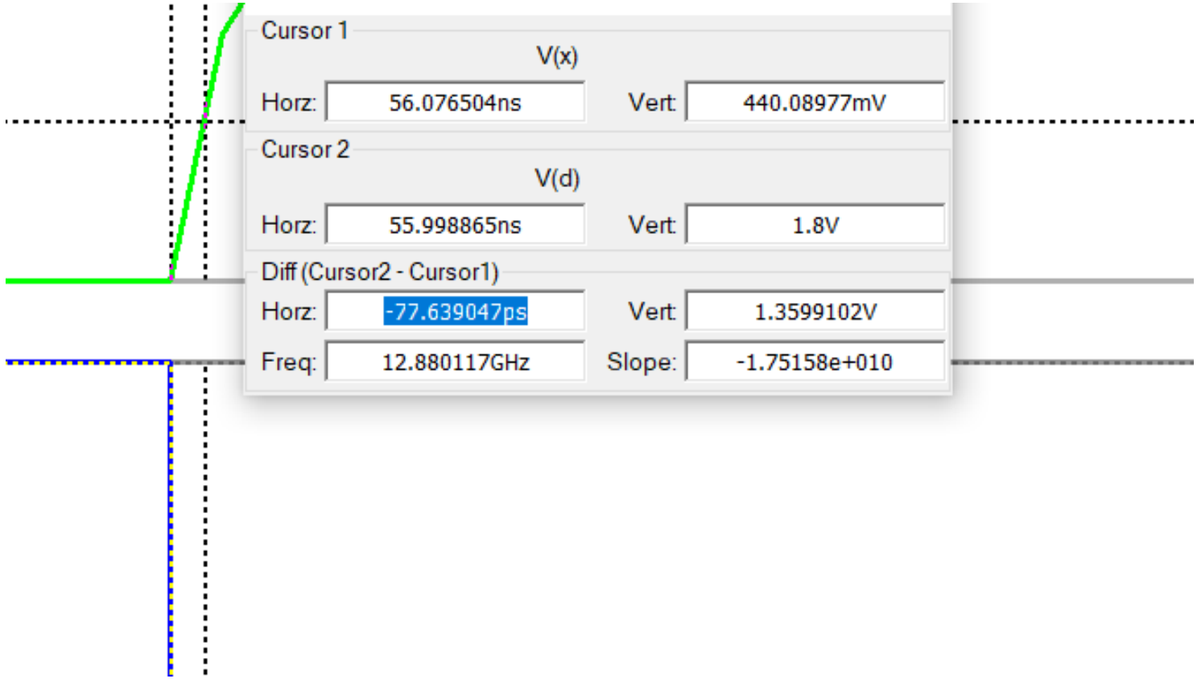
From simulation and the type of model file (180 umc T14B BSIM3 version 3.1 TSMC) we got 1 inverter delay found tobe 77.639 PS.

As the hold time and setup time both should retain their values for 1 inv delay

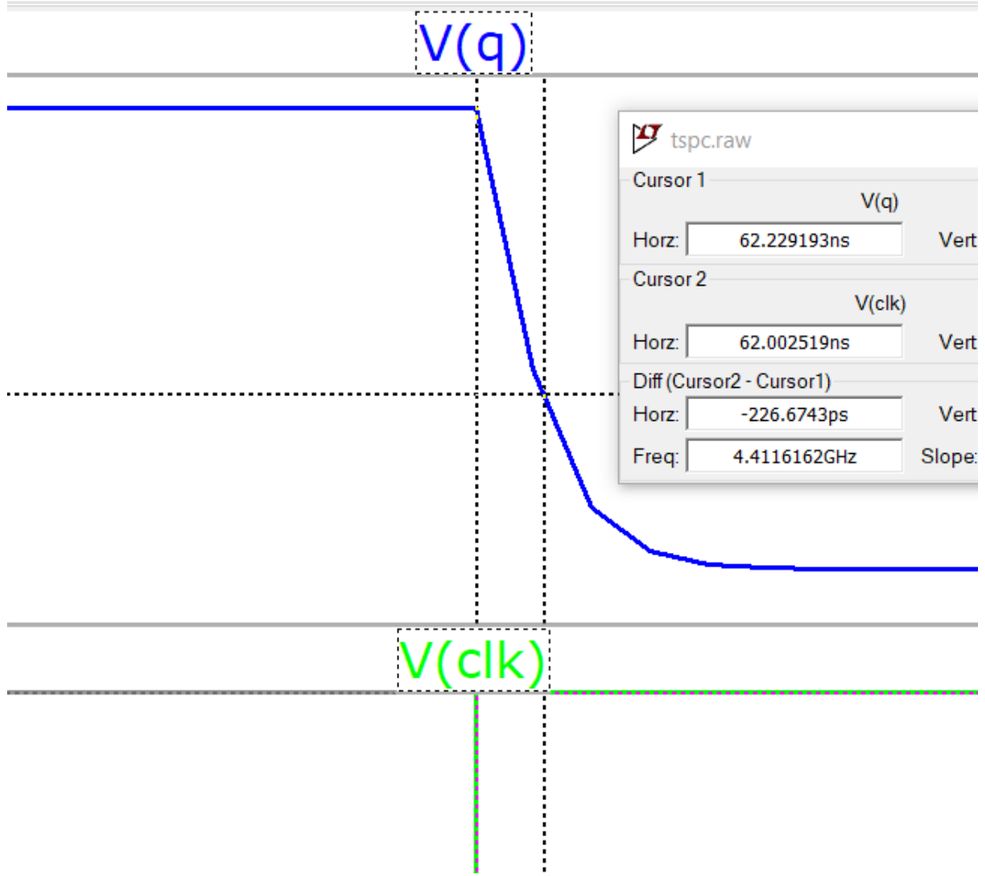
$$\therefore \boxed{t_h = t_s = 77.639 \text{ PS}}$$

and also the tc-q delay comes out tobe 3 x 77.639 (excluding the static 4th stage inv) is = 232.917 PS

# inverter delay and clock to q




one inverter delay




clock to q delay

↳ The operating (max^m) frequency can be calculated as –

$$T \geq t_{c-q} + t_{logic} + t_s$$

$$T \geq (3 \times 77.639) + 77.639 + 77.639$$

$$T \geq 388.195 \text{ PS}$$

hence, $f_{max} = \frac{1}{T} = \frac{1}{388.195}$

$$\Rightarrow \boxed{f_{max} = 2.576 \text{ GHz}}$$

## ↳ Calculation for power delay product -

PDP is the average energy consumed per switching event.

And its value can be calculated as

$$PDP = P_{avg} \times T_p = [C_L \times V_{DD}^2] / 2$$

(and its unit is watts · sec = Joule)

for us, $C_L = 500 fF$

and $V_{DD} = 1.8$

$$\therefore \quad PDP = 500 \times 10^{-15} \times (1.8)^2 \times \frac{1}{2}$$

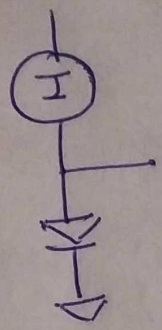
$$\Rightarrow \boxed{PDP = 810 \text{ fJoule}}$$

# Question

**Statement 2.** (8+2 marks)

Implement a Band Gap reference Circuit, with **Vref = 1.2 V, Temp. coefficient < = 200 ppm/$^0$C** ( for the worst case). **You can use any topology of your choice.** Also, show Vout *vs.* VDD and minimize the effect of supply voltage variation in output voltage.

## ↳ CTAT calculations —




$V_D$ = CTAT voltage

$$\frac{\partial V_D}{\partial T} = V_D - (4+m)V_T - E_g/q$$

for $m = -1.5$

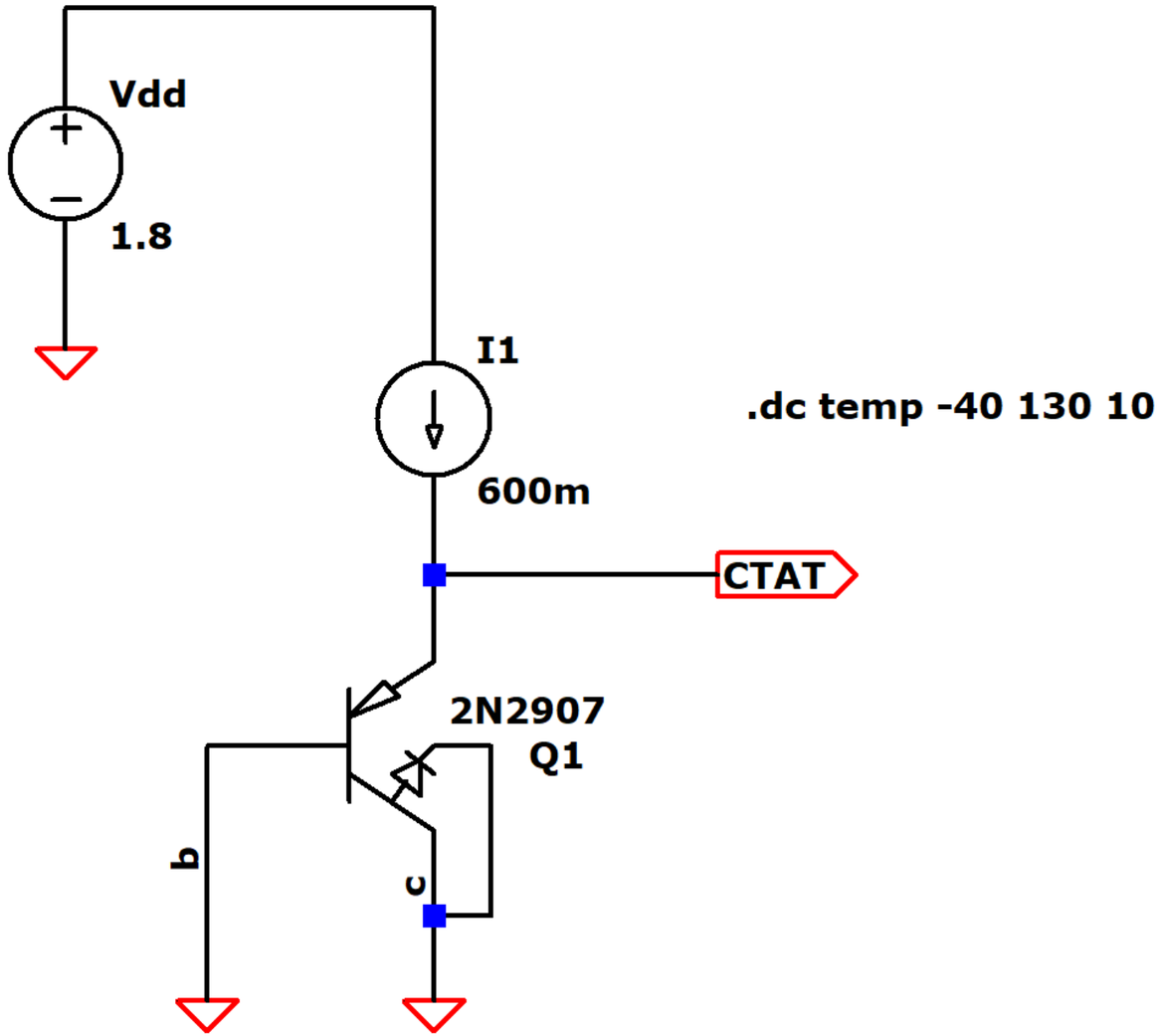
$V_T = 26\,mV$

$T = 300^\circ K$

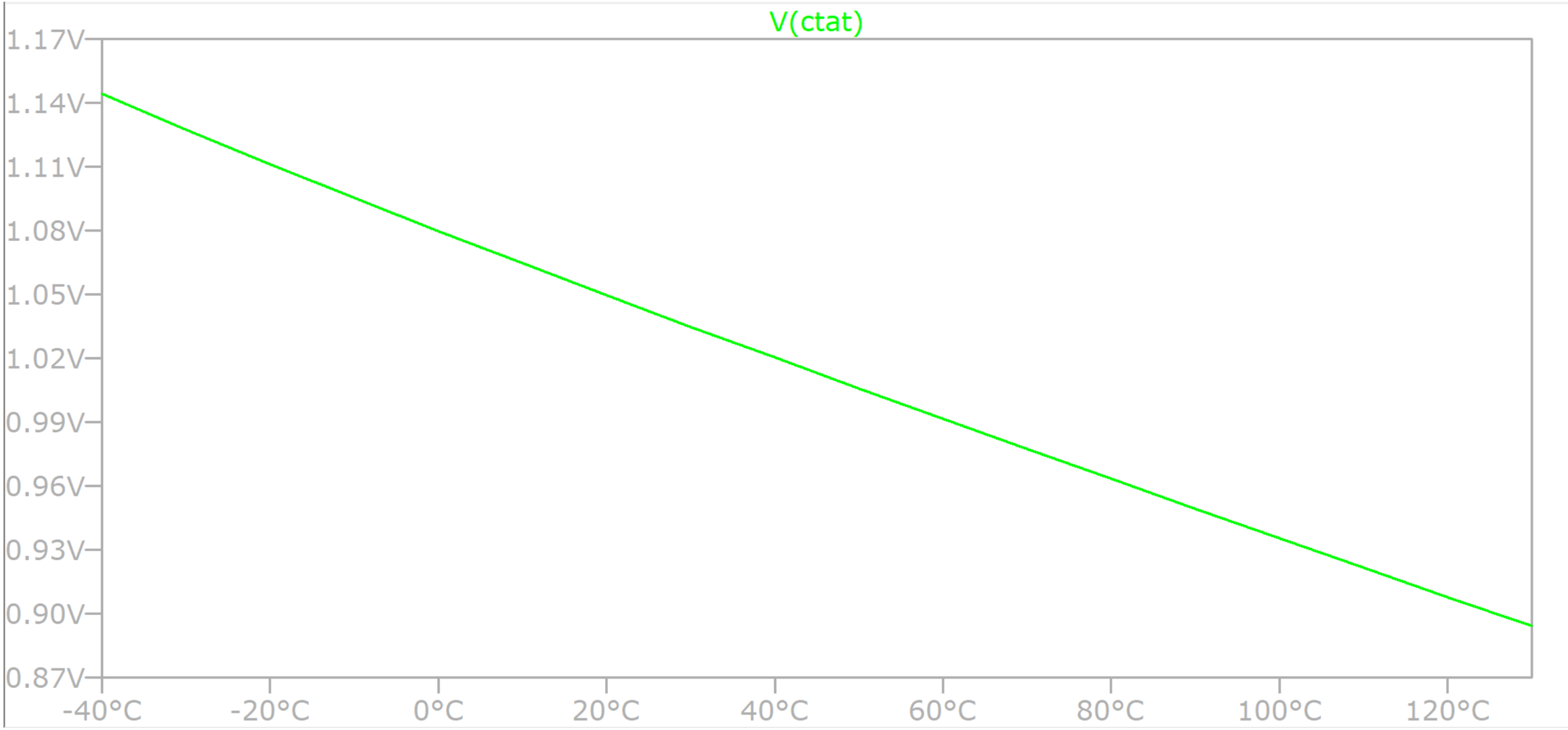
we have $\frac{\partial V_D}{\partial T} = -1.88\ mV/^\circ K$

and from the simulations done we got $\frac{\partial V_D}{\partial T} = -1.4\ mV/^\circ C$

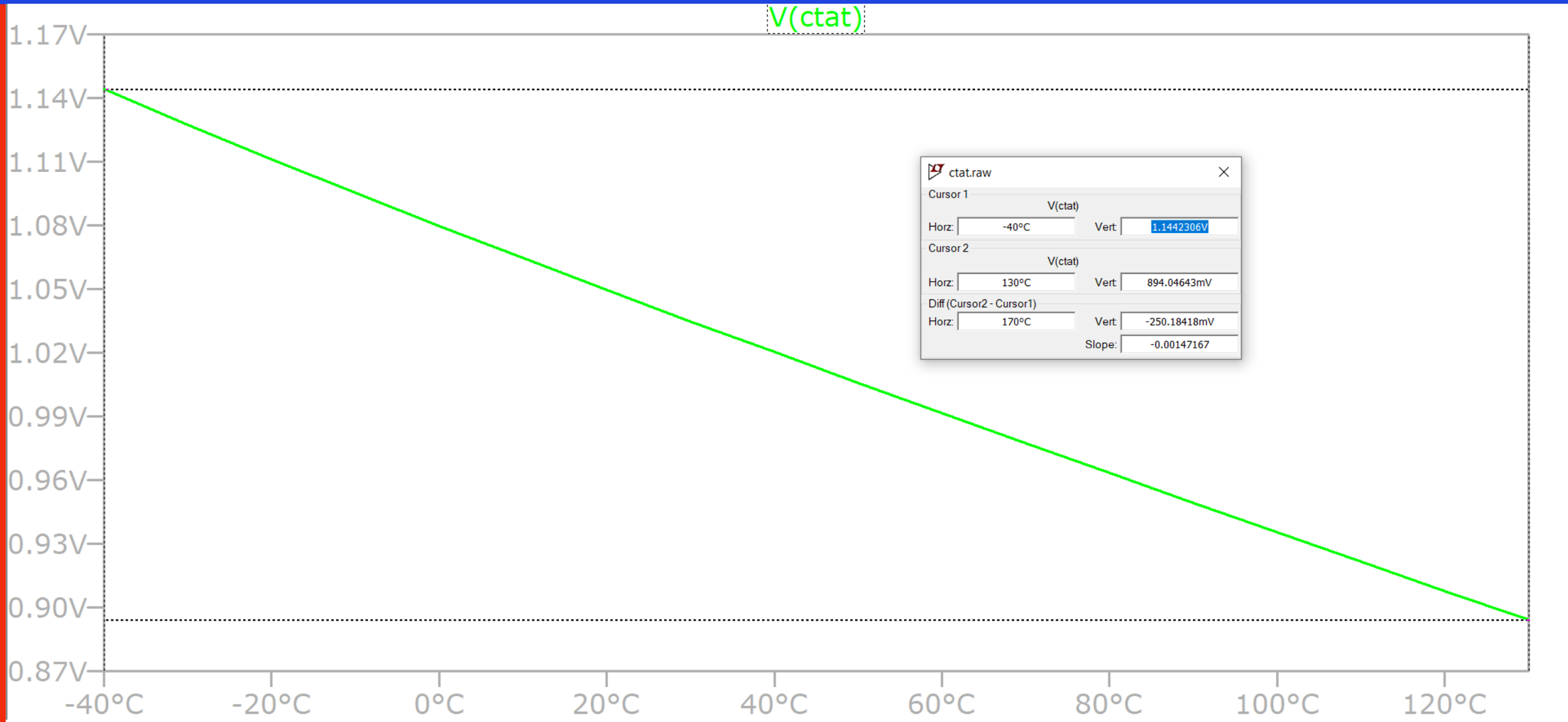
# CTAT



# CTAT simulation



# CTAT simulation



## ↳ PTAT and BGR calculations –

$\because V_T = \frac{KT}{q} \quad \therefore \boxed{V_T \propto \text{Temp}^{\wedge}}$

and also $V_D = V_t \ln \frac{I_o}{I_s} \longrightarrow$ CTAT

but $V_{D_1} = V_t \ln \frac{I_o}{n I_s} \longrightarrow$ PTAT

$\Rightarrow V_D - V_{D_1} = V_t \ln(n)$

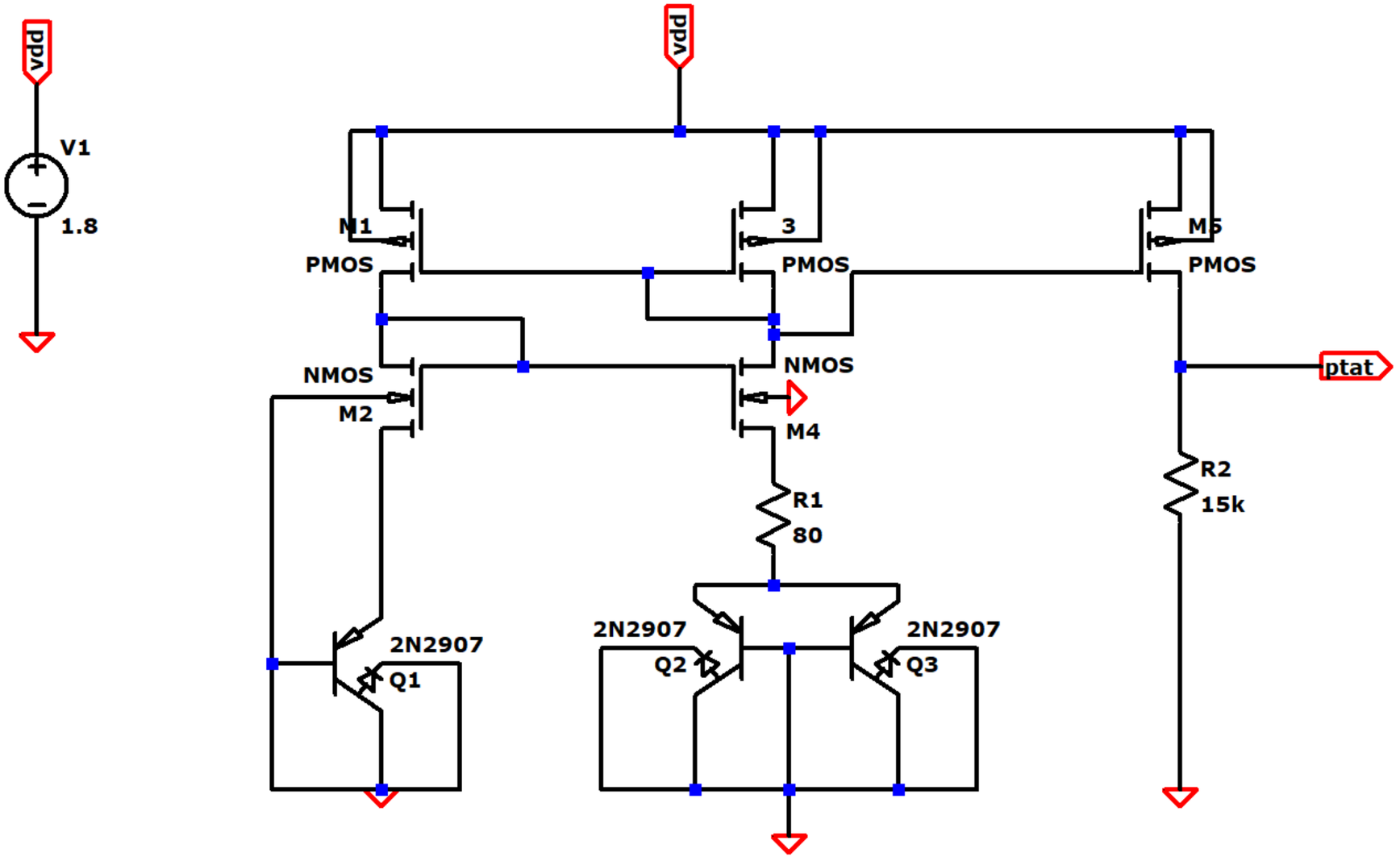
also for our simulations,

$V_{R_2} = \frac{R_2}{R_1} V_T \ln(n)$

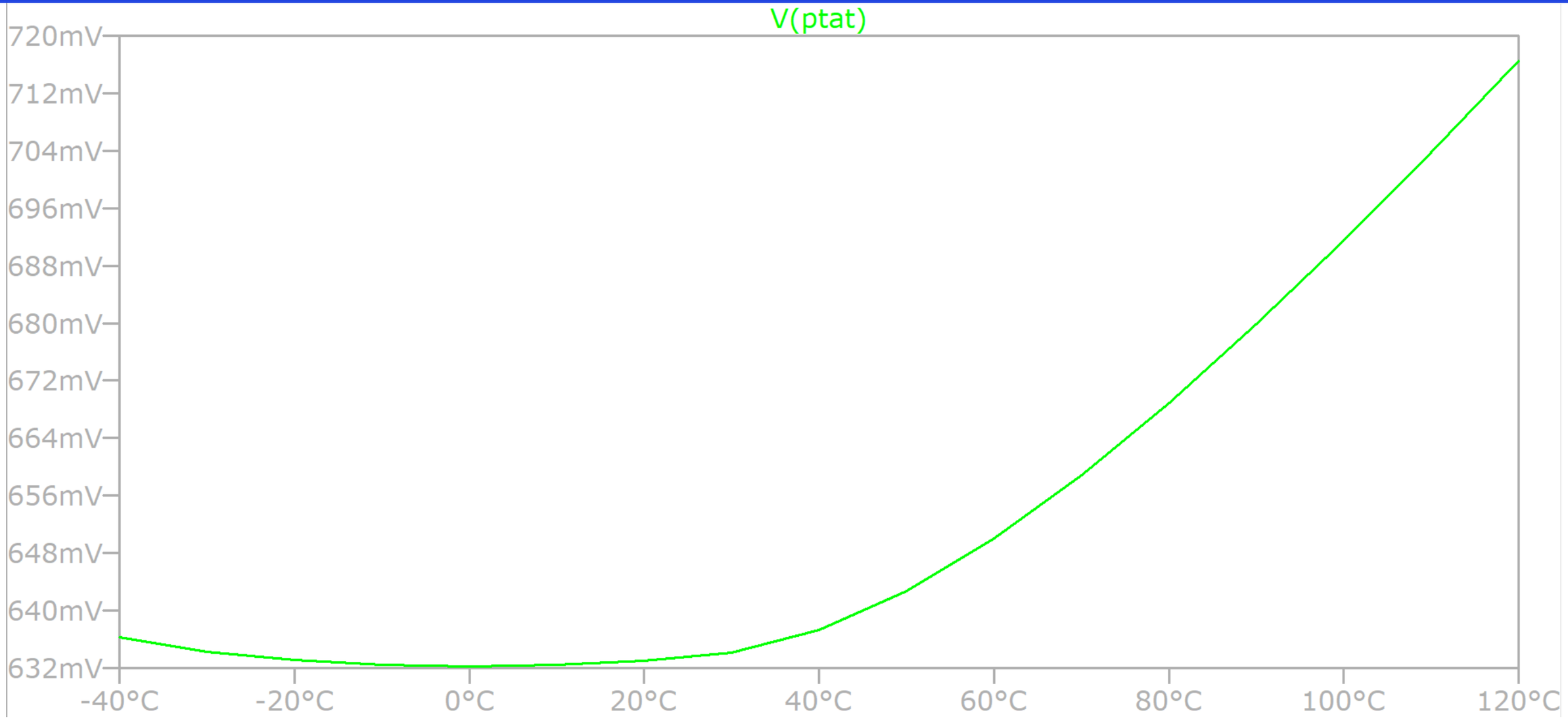
$\frac{\partial V_{R_2}}{\partial T} = \frac{\partial V_T}{\partial T} = \frac{K}{q} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

$= 87 \text{ uV/K}$

# PTAT


vdd
V1
1.8
vdd
M1
PMOS
3
PMOS
M5
PMOS
NMOS
M2
NMOS
M4
ptat
R2
15k
R1
80
2N2907
Q1
2N2907
Q2
2N2907
Q3

# PTAT simulation



↳ Note- To improve our B4R responses we increase our (W/L) ratios for pmos and Nmos.

The other reason for this is to make it as much as independent of the temp^ variations

$$\Rightarrow V_{REF} = V_{EB3} + \frac{R_2}{R_1} \times V_T \times \ln(n)$$

$$1.2 = 0.7 + \frac{R_2}{R_1} \times 0.026 \ln(n)$$

$$\Rightarrow \boxed{19.23 = \frac{R_2}{R_1} \ln(n)}$$

for ideal cases we have

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_T}{\partial T} \times \frac{R_2}{R_1} \ln(n) + \frac{\partial V_{EB3}}{\partial T} = 0$$

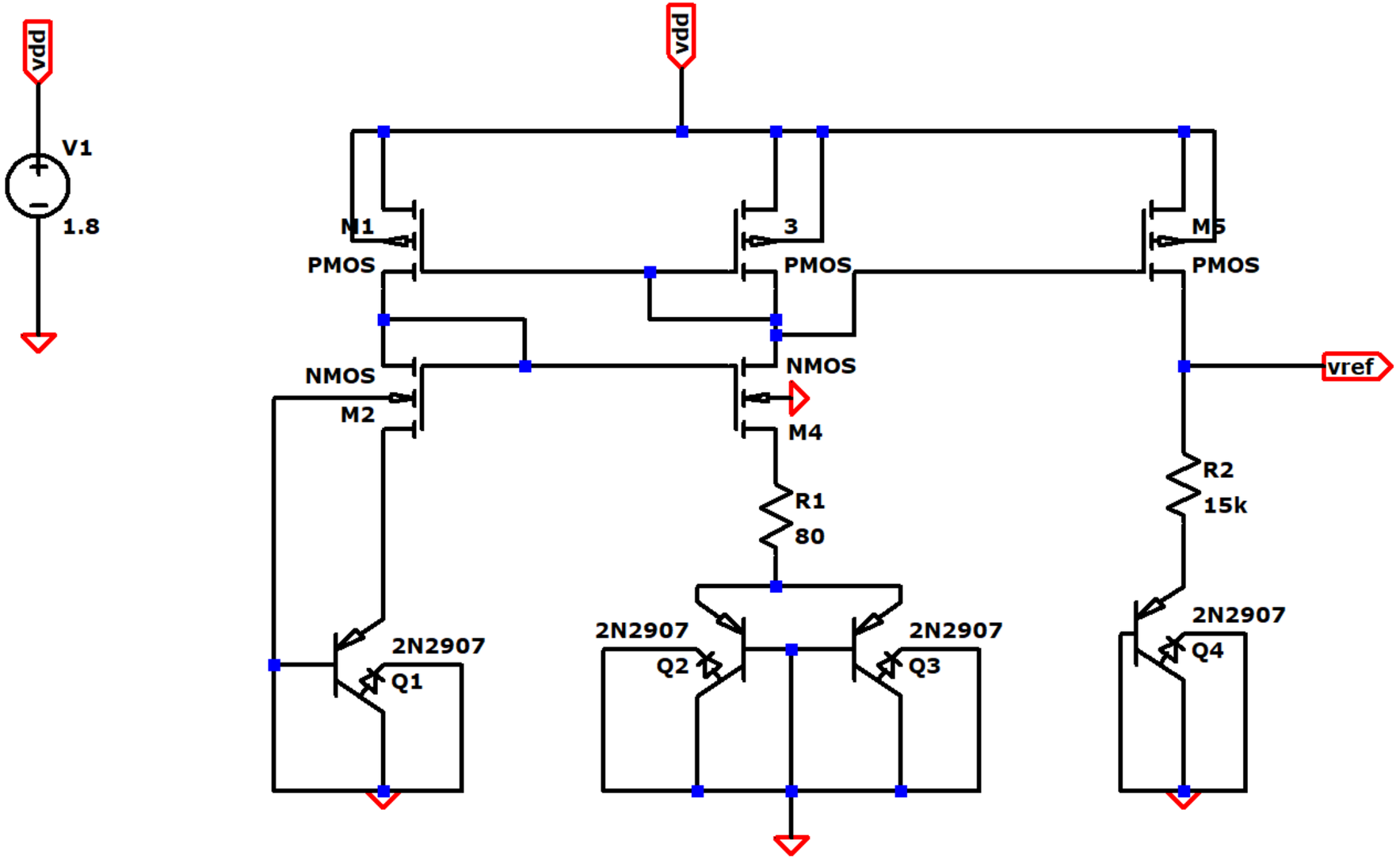
↳ for making it zero temp^ coeff.

also for the ideal cases we have—

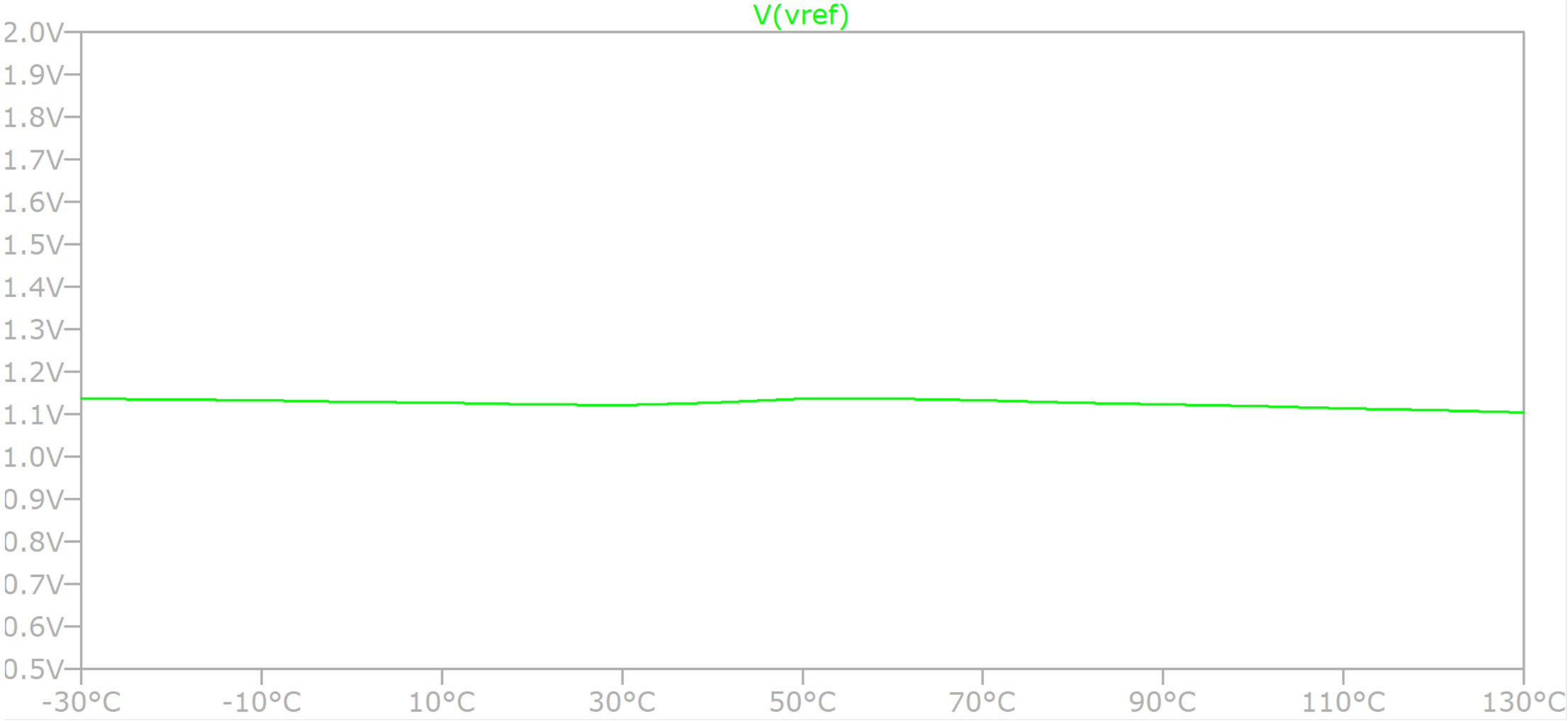
$$\frac{R_2}{R_1} \ln(n) \times 0.087 mV/°C - 1.5 mV/°C = 0$$

$$\Rightarrow \boxed{\frac{R_2}{R_1} \ln(n) = 17.2413}$$

# BGR circuit

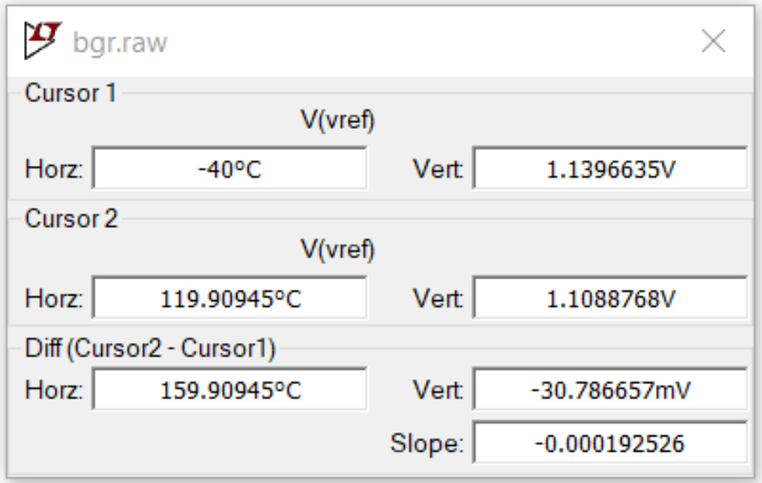

vdd
V1
1.8
vdd
M1
PMOS
3
PMOS
M5
PMOS
NMOS
M2
NMOS
M4
vref
R1
80
R2
15k
2N2907
Q1
2N2907
Q2
2N2907
Q3
2N2907
Q4

# BGR simulation



# BGR simulation

V(vref)



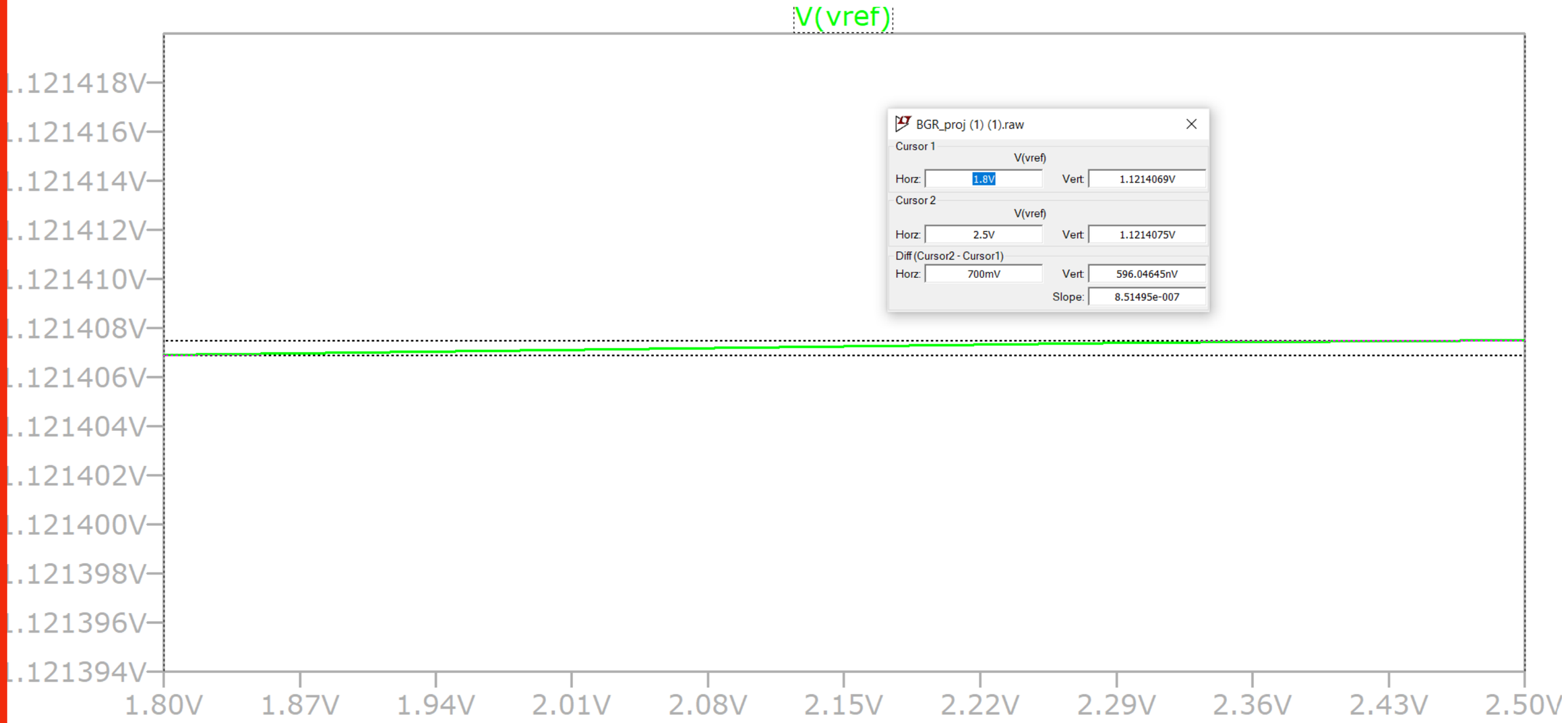
↳ Temp^ Coeff calculation -

$$\Rightarrow TC = \frac{1}{V_{Ref}} \times \frac{\partial V_{REF}}{\partial T}$$

$$= \frac{1}{1.2} \times \frac{30.78\,m}{120-(-40)}$$

$$= 160.03125 \text{ ppm/°C} \leq 200 \text{ ppm/°C}$$

# effect of increasing supply voltage on vref



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Thank you

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