Assignment -1, HDM

Submission deadline: **15th February 2022** **Max. Marks:** **[10* + 5 Marks for viva]**

Each submitted assignment should have:
1. SPICE Netlist of each circuit
2. Circuit schematic with the node numbers as given in the SPICE netlist
3. All the relevant simulation snapshots with white background
4. Relevant analysis and final results. Take VDD = 3.3 V, Cin = 2 pF if not given. Use SPICE level-3 model file.

1 Implement 4 bit ripple carry adder. Optimize the adder for speed. Assume load capacitance to be 50 pF, V_{DD} = 3.3 V. You may assume input capacitance to be 2 pF (for the input A [3:0], B [3:0] and Cin) if required in the calculation. The basic full adder block and 4bit adder architecture is given below. Reference [Weste & Harris, CMOS VLSI Design, Chapter 11 { 11.2.1, 11.2.2}]

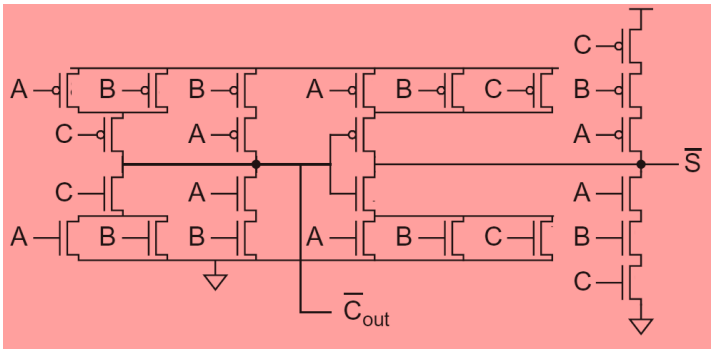

Fig.1 Basic Full adder with complementary output

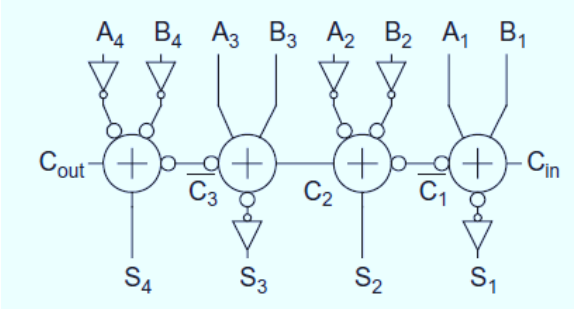

Fig.2 4 bit ripple carry adder using Fig.1

2 Design a superbuffer using CMOS inverters to drive a load of 100 pF, assume the input capacitance to be 2 pF.

//Use the following SPICE model for MOSFETs to simulate the circuits:

```
.model nch NMOS
+ LEVEL = 3
+ VTO = 0.70
+ UO = 660
+ TOX = 1.40E-08
+ NSUB = 3E+16
+ XJ = 2.0e-7
```

```
+ LD = 1.6E-08
+ NFS = 7e+11
+ VMAX = 1.8e5
+ DELTA = 2.40
+ ETA = 0.1
+ KAPPA = 0.15
+ THETA = 0.1
+ CGDO = 2.20E-10
+ CGSO = 2.20E-10
+ CGBO = 7.00E-10
+ MJ = 0.50
+ CJSW = 3.50E-10
+ MJSW = 0.38
.model pch PMOS
+ LEVEL = 3
+ VTO = -0.70
+ UO = 210
+ TOX = 1.40E-08
+ NSUB = 6.00e16
+ XJ = 2.0e-7
+ LD = 1.5E-08
+ NFS = 6E+11
+ VMAX = 2.00e5
+ DELTA = 1.25
+ ETA = 0.1
+ KAPPA = 2.5
+ THETA = 0.1
+ CGDO = 2.20E-10
+ CGSO = 2.20E-10
+ CGBO = 7.00E-10
+ MJ = 0.50
.end
```