DESIGN AND STUDY OF SRAM CELL CIRCUITRY FOR THE PROTECTION AGAINST SINGLE EVENT UPSET

SUBMITTED TO

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Abstract

This work mainly focuses on studying the behaviour of different sram cells that have been proposed and their advantages and disadvantages in comparison to one another. A novel 14T sram cell design in a 45-nm cmos technology to protect the circuit from the uncertain seu events is also proposed which is to be further studied and optimized for low power dissipation.

I. Introduction

The 6T sram cell is the most basic structure which is generally used in the cache memory. It is kind of a volatile memory because it is not able to retain its original state when the power is switched off. But when we want this memory to work in tough environment, lets say in aviation field or under the sea for the equipments of submarines then 6T somehow comes out to be a big failure. The reason behind this is when some particle trying to strike the drain of the pmos or nmos that is involved in the circuit then it forcefully charges it which is leading to change the originally stored state. So if the circuit is not protected then the false value will propagate during read and write operations and hence leading to the failure of the circuit and so the equipment. So in order to skip this unfortunate event various cell designs have been proposed like 7T, 10T, 12T, 13T, 14T etc. This circuits have their own advantages and disadvantages in terms of various parameters like power, area, noise margins and most importantly the ability to protect the design from single event upsets.

II. Literature review

- In 2009 a research paper was published in which a 10T cell was proposed with the aim of seu recovery. The challenge that it faced was it was only able to do a recovery from 1 to 0 only and hence protecting the circuit partially from seu events.

- In 2012 a 13T cell was proposed but faced the issues of lesser writing speed and more power consumption with increased area.
- In 2015, inspired from the previously proposed 13T a new and modified topology of 11T and 13T were proposed but in them also no much significant improvements were observed.
- In 2016 a new cell design 12T was proposed which performed well than the already available designs but in their topology as they have use two nmos in the pull up which lead to bad values of read noise margins of the cell.
- In 2018 a newly proposed 14T was introduced which included two extra nmos which lead to slightly increase in area but had a better seu recovery.

III. Work and contribution

For this semester the focus was on studying the different behaviours that the pre existing cells possess, the parameters on which they are able to work and how much they are capable to avoid the uncertain situations. The aim for this semester was to focus on building the base for the motivation to build such designs which are very important in the aviation and under sea work of fields.

With this some practical simulations were also performed of the pre existing circuits and an attempt had been made to design a new topology containing 14T but more power optimized. The work is still going on and most probably will be taken as the thesis topic in the upcoming semester.

IV. Results and Discussion

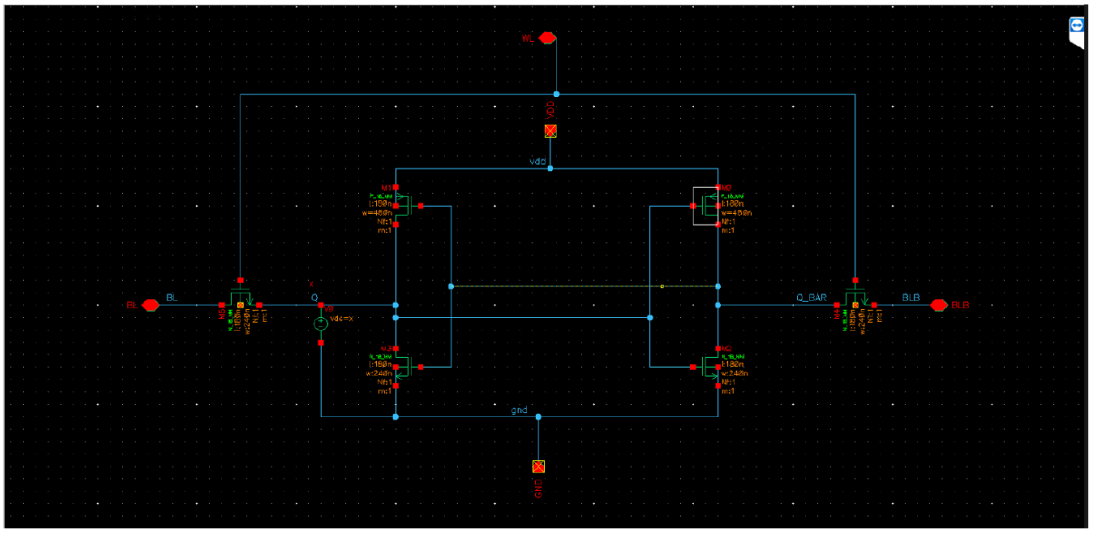

FIGURE 1. Basic 6T sram cell design

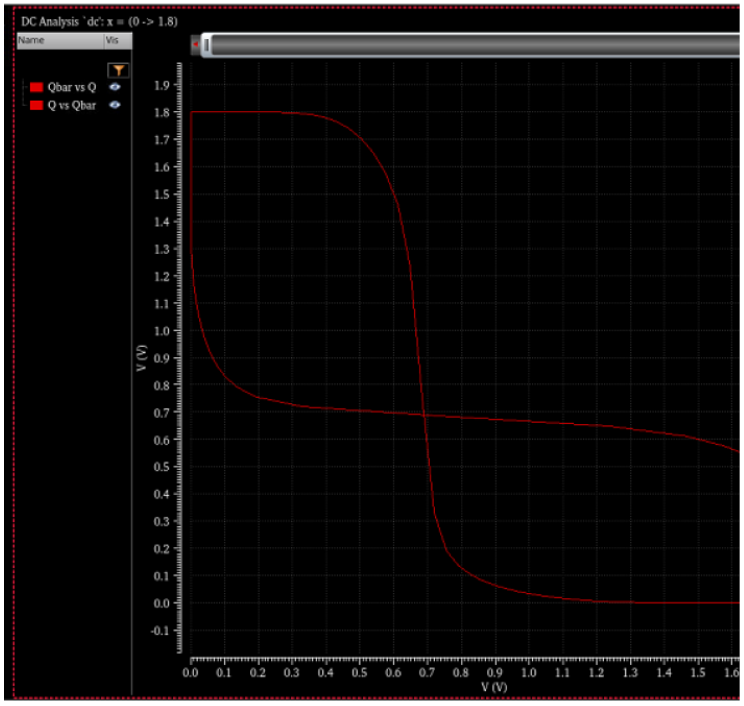

FIGURE 2. Q vs QB and QB vs Q

y axis – voltage

x axis – voltage

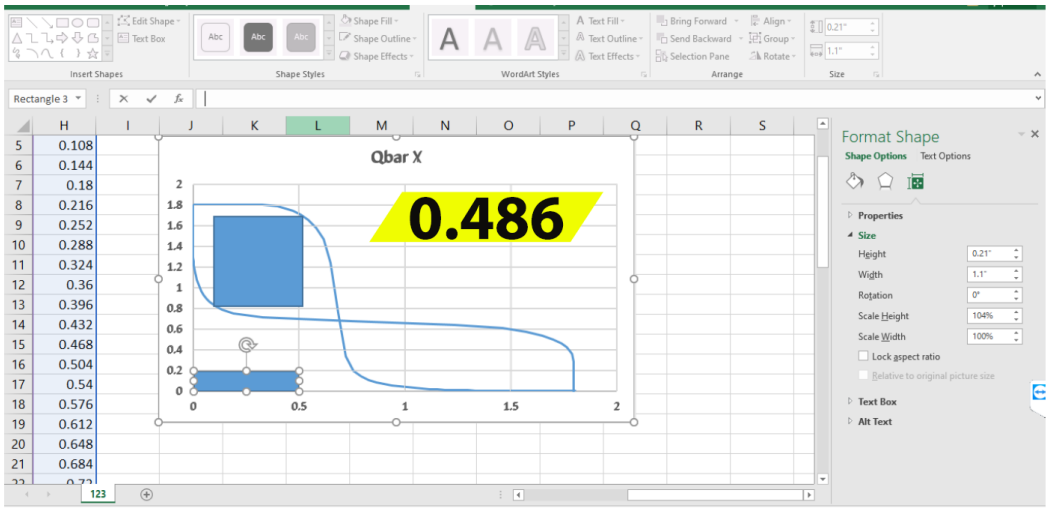

FIGURE 3. Calculation of graphical snm

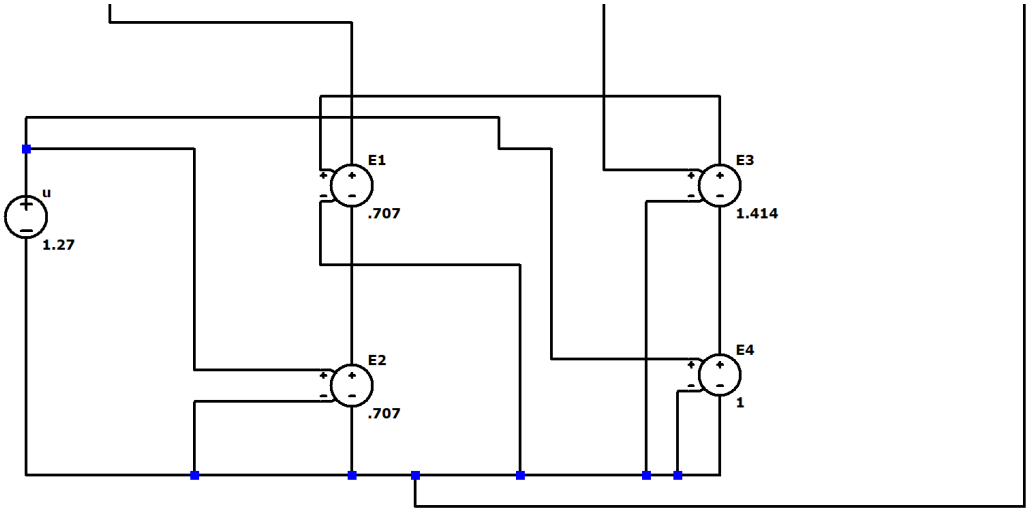

FIGURE 4. Transformation circuit for actual snm

FIGURE 5. Calculation for actual snm

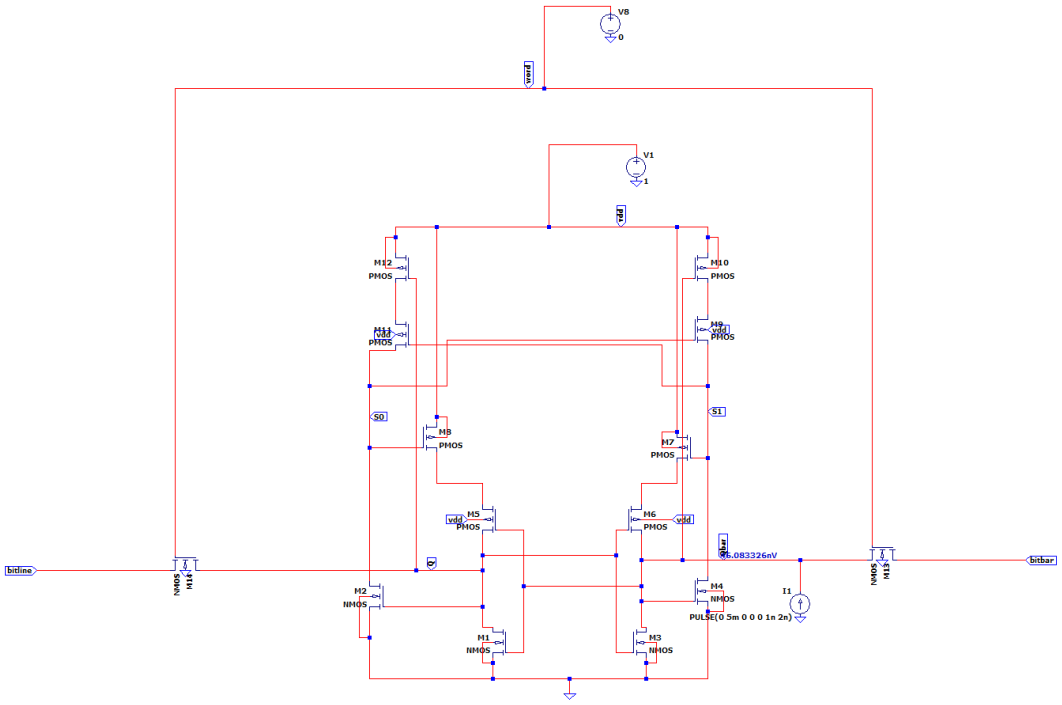

FIGURE 6. 14T cell design

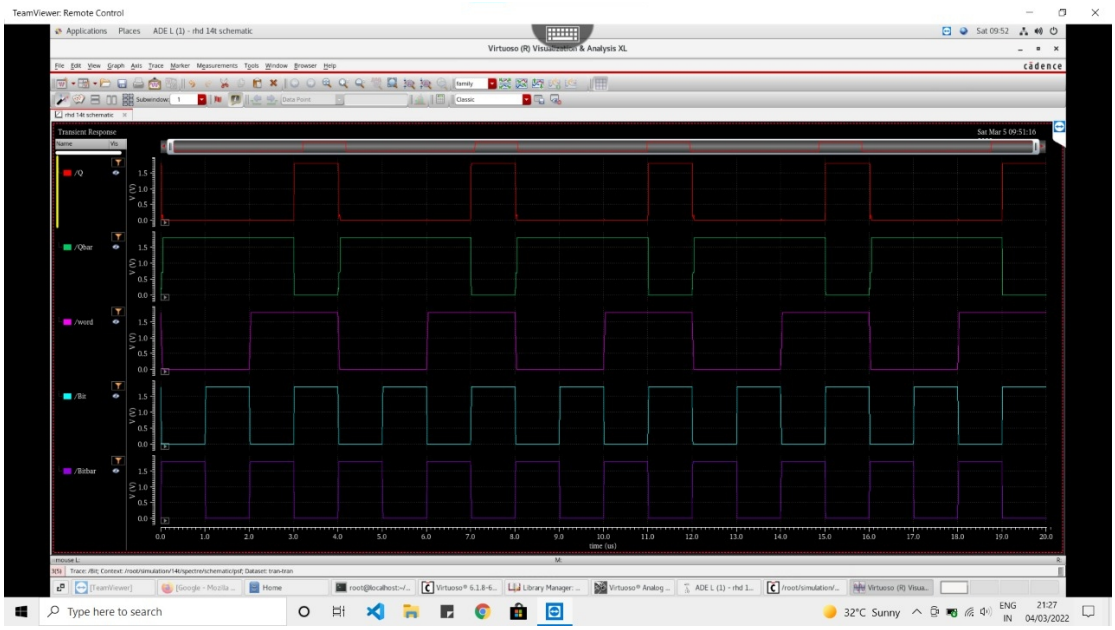

FIGURE 7. Read and write waveforms

y axis – Q, QB, BL, BLB, WORD (volts)

x axis – time (sec)

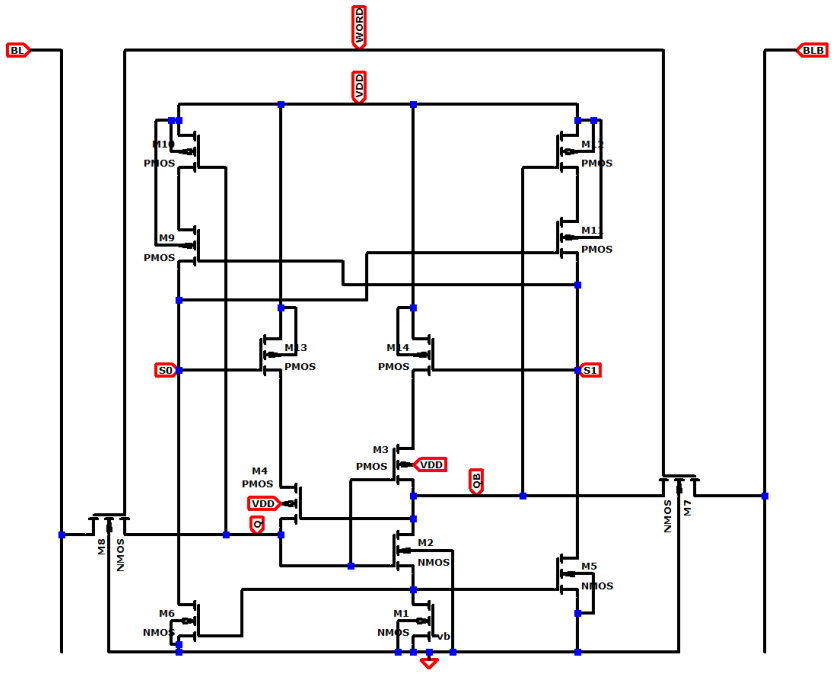

FIGURE 8. New 14T aimed for power optimized (ongoing work)

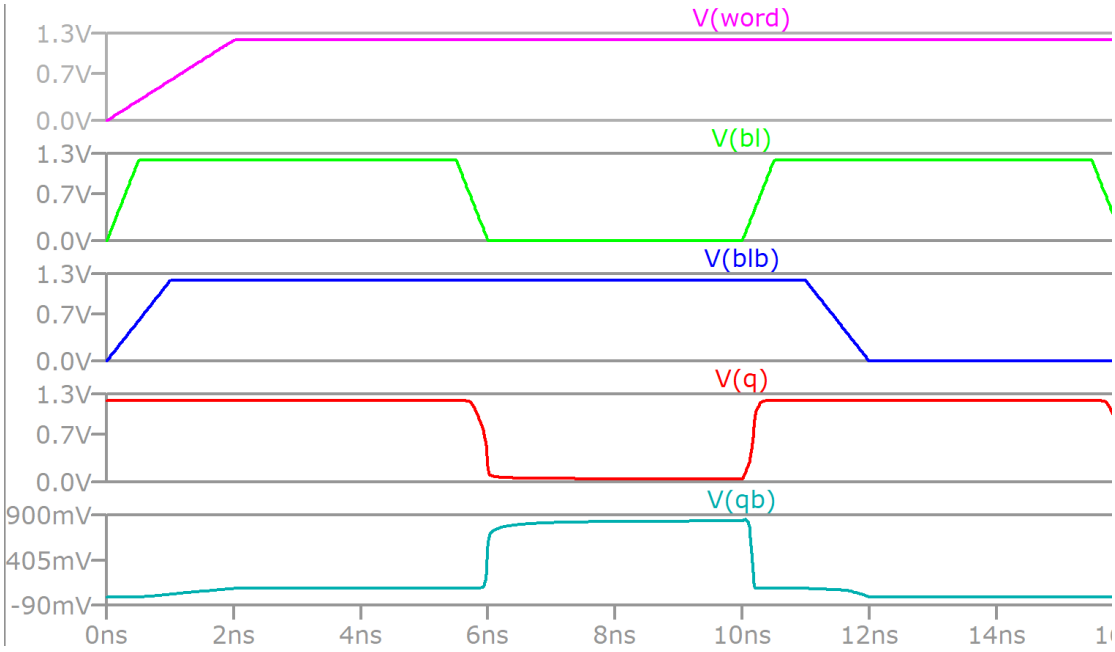

FIGURE 9. Read and write waveforms (ongoing work)

V. Conclusion

For seu the designs that are available are proposed by carefully studying what is the effect inside the cell at each nmos and pmos and will the circuit be able to recover from them and how fast. The limitation of my work is that its still under going but when optimized with proper ratios of w/l and slight change in topology (if required) will make solve the aim for what a seu sram cell design should be.

VI. Future scope

Such designs as mentioned previously are very much required in the military services since all the equipments had to work under hard conditions which are capable to malfunction any electronic devices. Hence, developing a proper protection circuitry is the urgent need.

References

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