C2 REVIEW ASSIGNMENT

VERILOG

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MEC2021015

MTECH

1ST SEM ECE

IIIT ALLAHABAD

Xilinx - ISE - B:\iiit-a\mux\mux.ise - [mux4.ngr]

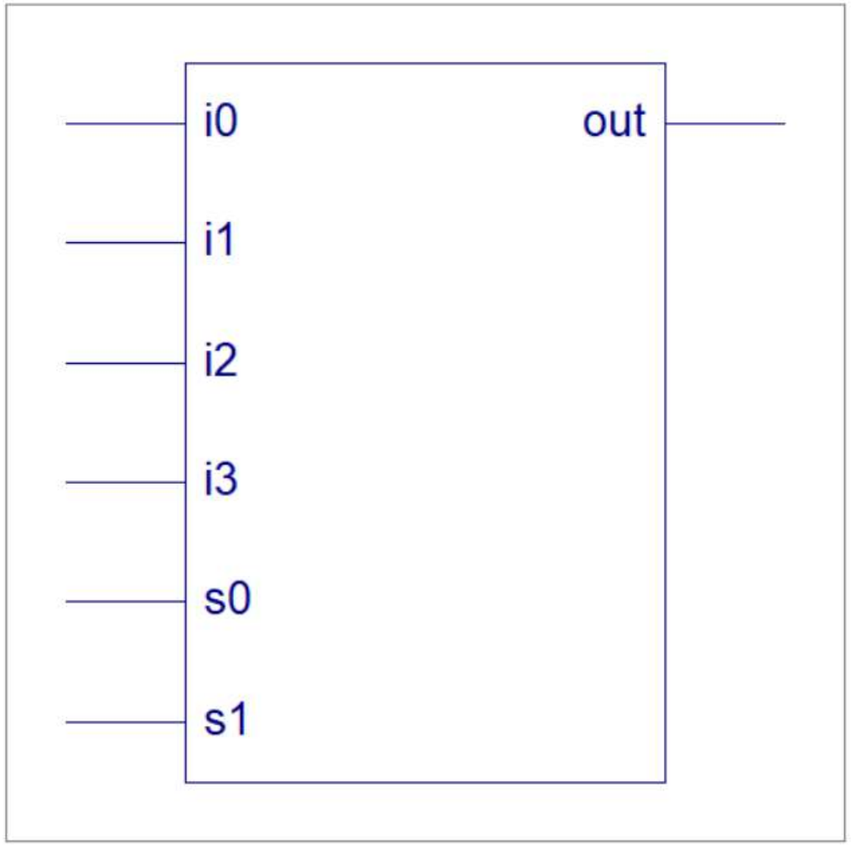
File Edit View Project Source Process Window Help

mux4
- m1
- m2
- m3

Snapshots | Libraries | Design

No flow available.

Processes



Design Summary | Synthesis Repor... | mux4 | dfecs

Design Objects of Top Level Symbol

Instances	Pins	Signals

Properties
No object is selected

Name	Value

Console | Errors | Warnings | Find in Files | View by Category | View by Name

[520,480]

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [mux4.ngr]

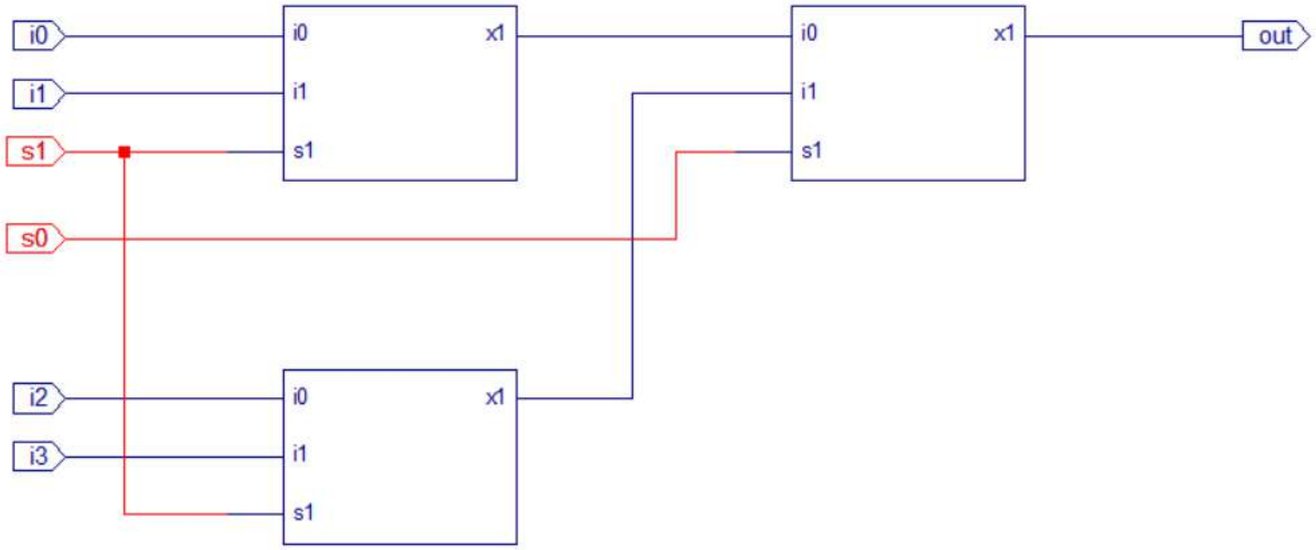
File Edit View Project Source Process Window Help

mux4
- m1
- m2
- m3

Snapshots Libraries Design

No flow available.

Processes



Design Summary | Synthesis Repor... | mux4 | dfecs

Design Objects of mux4

Instances	Pins	Signals
m1	s0	s0
m2	s1	s1

Properties
No object is selected

Name	Value

Console | Errors | Warnings | Find in Files | View by Category | View by Name

[1644,1020]

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [dfecs.v]

File Edit View Project Source Process Window Help

Sources for: Synthesis/Implementation

- mux
- xc3s50-5pq208
  - mux4 (dfecs.v)
    - m1 - mux2 (dfecs.v)
    - m2 - mux2 (dfecs.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- View Design Summary
- Design Utilities
- User Constraints
- Synthesize - XST
  - View Synthesis Report
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File

Processes

```
10  // Target Devices:
11  // Tool versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21  module mux2(x1,i0,i1,s1);
22  output reg x1;
23  input i0,i1,s1;
24  always @(i0,i1,s1)
25  begin
26  if(s1)
27  x1 = i1;
28  else
29  x1 = i0;
30  end
31  endmodule
32
33  module mux4(out,i0,i1,i2,i3,s1,s0);
34  output out;
35  input i0,i1,i2,i3,s1,s0;
36  wire x1,x2;
37  mux2 m1(x1,i0,i1,s1);
38  mux2 m2(x2,i2,i3,s1);
39  mux2 m3(out,x1,x2,s0);
40  endmodule
41
```

Design Summary | Synthesis Repor... | mux4 | dfecs

```
Started : "Launching RTL Schematic Viewer for mux4.ngr".

Started : "Launching ISE Text Editor to edit dfecs.v".
```

Console | Errors | Warnings | Find in Files

Ln 26 Col 7 | CAPS | NUM | SCRL | Verilog

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [fvscv.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- mux
- xc3s50-5pq208
  - tb_mux (fvscv.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator

Processes

```
23 ////////////////////////////////////////////////////////////////////////////////
24
25 module tb_mux;
26
27    // Inputs
28    reg i0;
29    reg i1;
30    reg i2;
31    reg i3;
32    reg s1;
33    reg s0;
34
35    // Outputs
36    wire out;
37
38    // Instantiate the Unit Under Test (UUT)
39    mux4 uut (
40       .out(out),
41       .i0(i0),
42       .i1(i1),
43       .i2(i2),
44       .i3(i3),
45       .s1(s1),
46       .s0(s0)
47    );
```

Design Summary | Synthesis Repor... | mux4 | dfecs | fvscv

```
Started : "Launching RTL Schematic Viewer for mux4.ngr".

Started : "Launching ISE Text Editor to edit dfecs.v".
```

Console | Errors | Warnings | Find in Files

Ready

Ln 25 Col 14 | CAPS | NUM | SCRL | Verilog

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [fvscv.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- mux
- xc3s50-5pq208
  - tb_mux (fvscv.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator

Processes

```
49      initial begin
50          // Initialize Inputs
51          i0 = 0;
52          i1 = 0;
53          i2 = 0;
54          i3 = 0;
55          s1 = 0;
56          s0 = 0;
57
58          // Wait 100 ns for global reset to finish
59          #100;
60
61          // Add stimulus here
62      i0 = 1'b1;
63      i1 = 1'b0;
64      i2 = 1'b1;
65      i3 = 1'b1;
66      s1 = 1'b0;
67      s0 = 1'b1;
68
69      #5
70      i0 = 1'b0;
71      i1 = 1'b1;
72      i2 = 1'b0;
73      i3 = 1'b0;
```

Design Summary | Synthesis Repor... | mux4 | dfecs | fvscv

```
Started : "Launching RTL Schematic Viewer for mux4.ngr".

Started : "Launching ISE Text Editor to edit dfecs.v".
```

Console | Errors | Warnings | Find in Files

Ready

Ln 25 Col 14 | CAPS | NUM | SCRL | Verilog

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [fvscv.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- mux
- xc3s50-5pq208
  - tb_mux (fvscv.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator

Processes

```
71  i1 = 1'b1;
72  i2 = 1'b0;
73  i3 = 1'b0;
74  s1 = 1'b0;
75  s0 = 1'b1;
76
77  #5
78  i0 = 1'b0;
79  i1 = 1'b0;
80  i2 = 1'b1;
81  i3 = 1'b0;
82  s1 = 1'b1;
83  s0 = 1'b1;
84
85  #5
86  i0 = 1'b0;
87  i1 = 1'b0;
88  i2 = 1'b0;
89  i3 = 1'b1;
90  s1 = 1'b1;
91  s0 = 1'b1;
92     end
93
94  endmodule
95
```

Design Summary | Synthesis Repor... | mux4 | dfecs | fvscv

```
Started : "Launching RTL Schematic Viewer for mux4.ngr".

Started : "Launching ISE Text Editor to edit dfecs.v".
```

Console | Errors | Warnings | Find in Files

Ready

Ln 25 Col 14 | CAPS | NUM | SCRL | Verilog

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Xilinx - ISE - B:\iiit-a\mux\mux.ise - [Simulation]

File Edit View Project Source Process Test Bench Simulation Window Help

Sources for: Behavioral Simulation

- mux
- xc3s50-5pq208
  - tb_mux (fvscv.v)

Sources | Snapshots | Libraries

Hierarchy of tb_mux:

- tb_mux tb_mux

Processes | Sim Hierarchy - tb_mux

Now: 115 ns

		99 ns	102	104 ns	107	110 ns	113
out	1						
s0	1						
s1	1						
i0	0						
i1	0						
i2	0						
i3	1						

Design Summary | Synthesis Repor... | mux4 | dfecs | fvscv | Simulation

```
Finished circuit initialization process.

1 >
```

Console | Errors | Warnings | Find in Files | Sim Console - tb_mux

Ready

Type here to search

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You have reached
end of this document

Thank you