C2 REVIEW ASSIGNMENT

VERILOG

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MEC2021015

MTECH

1ST SEM ECE

IIIT ALLAHABAD

Question 1
D FLIP FLOP

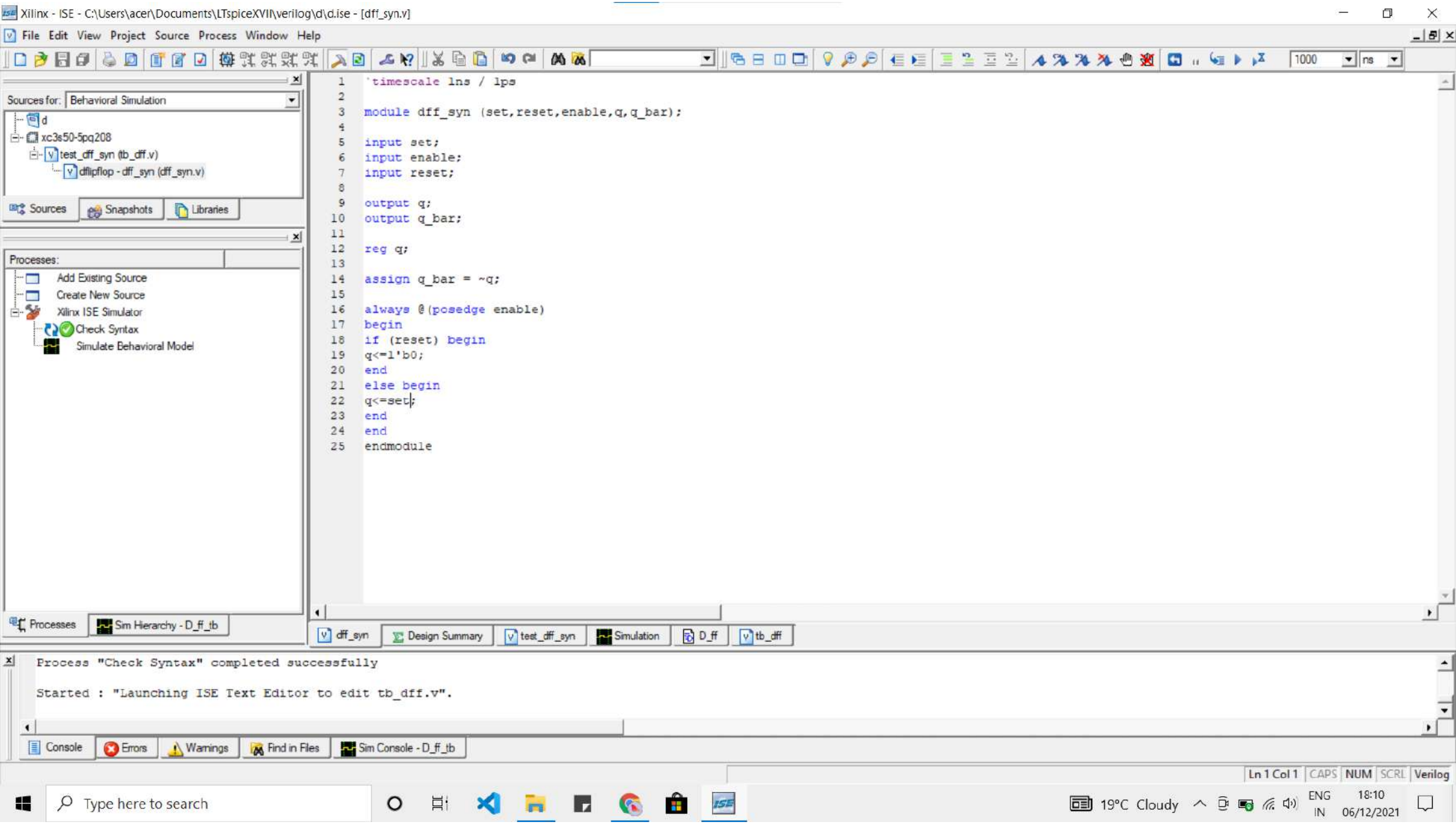
TRUTH TABLE

Que. 1

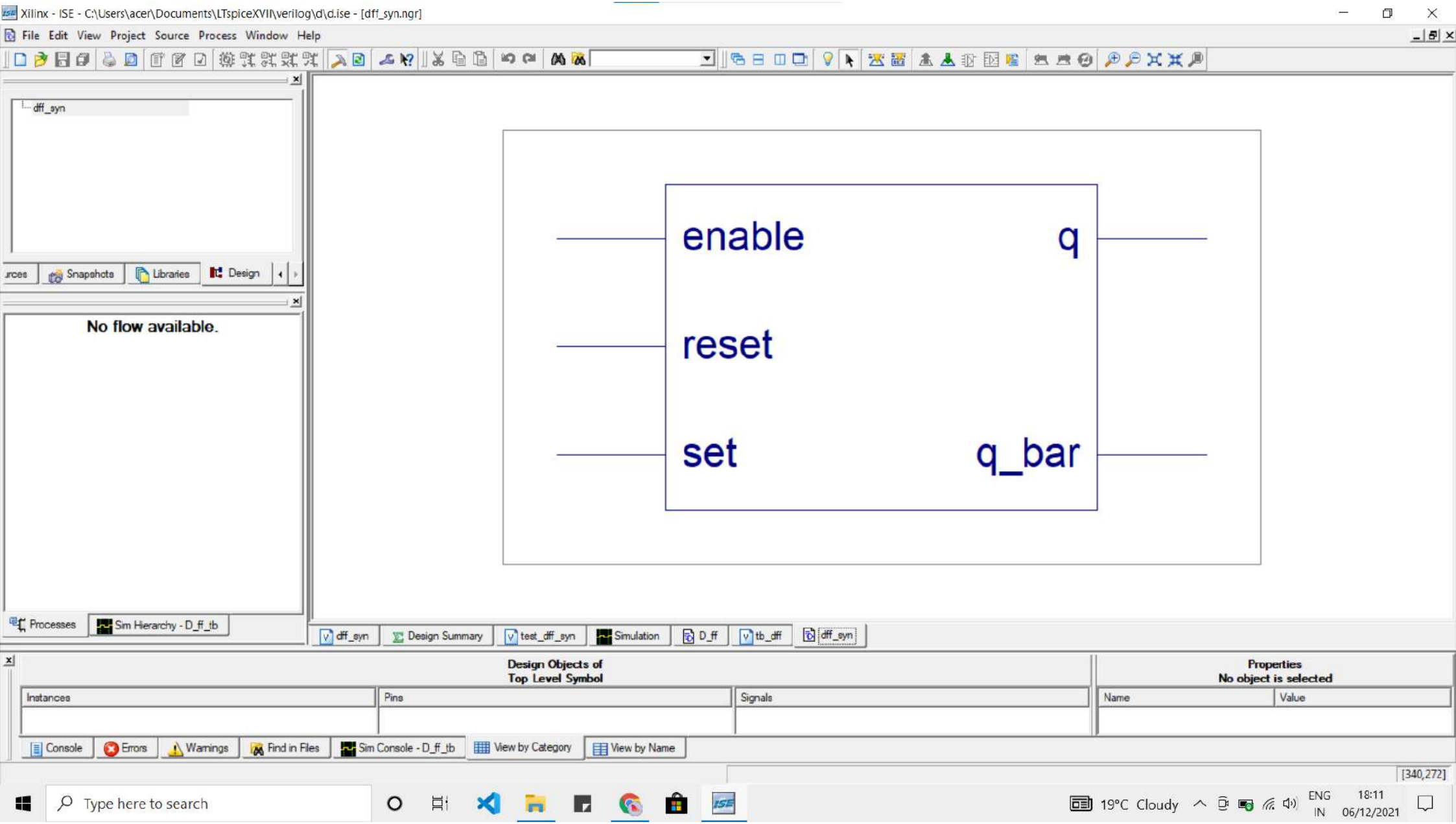
⇒ D-Flipflop Truth Table –

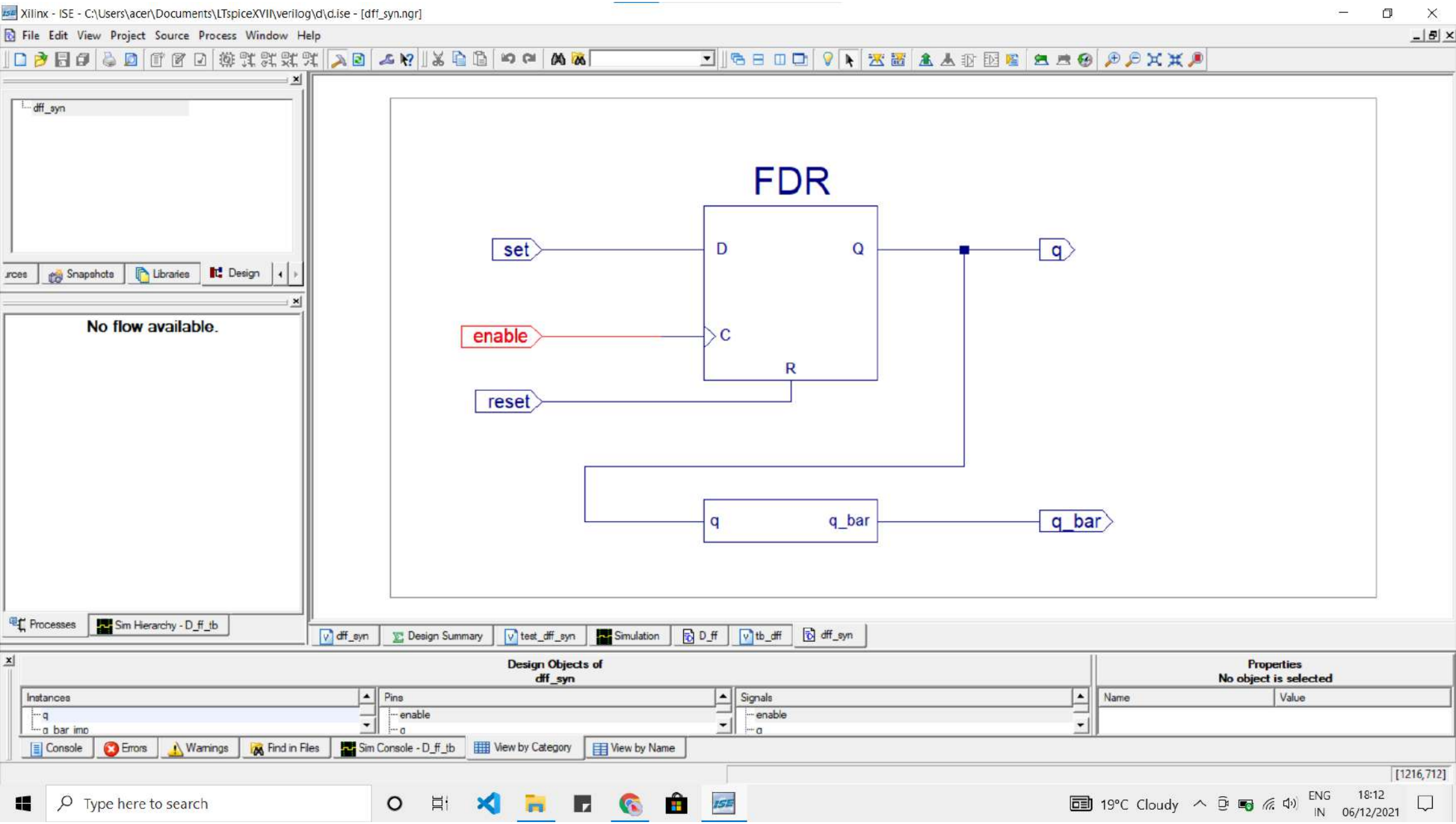
enable	set	q	q-bar
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

writing the module

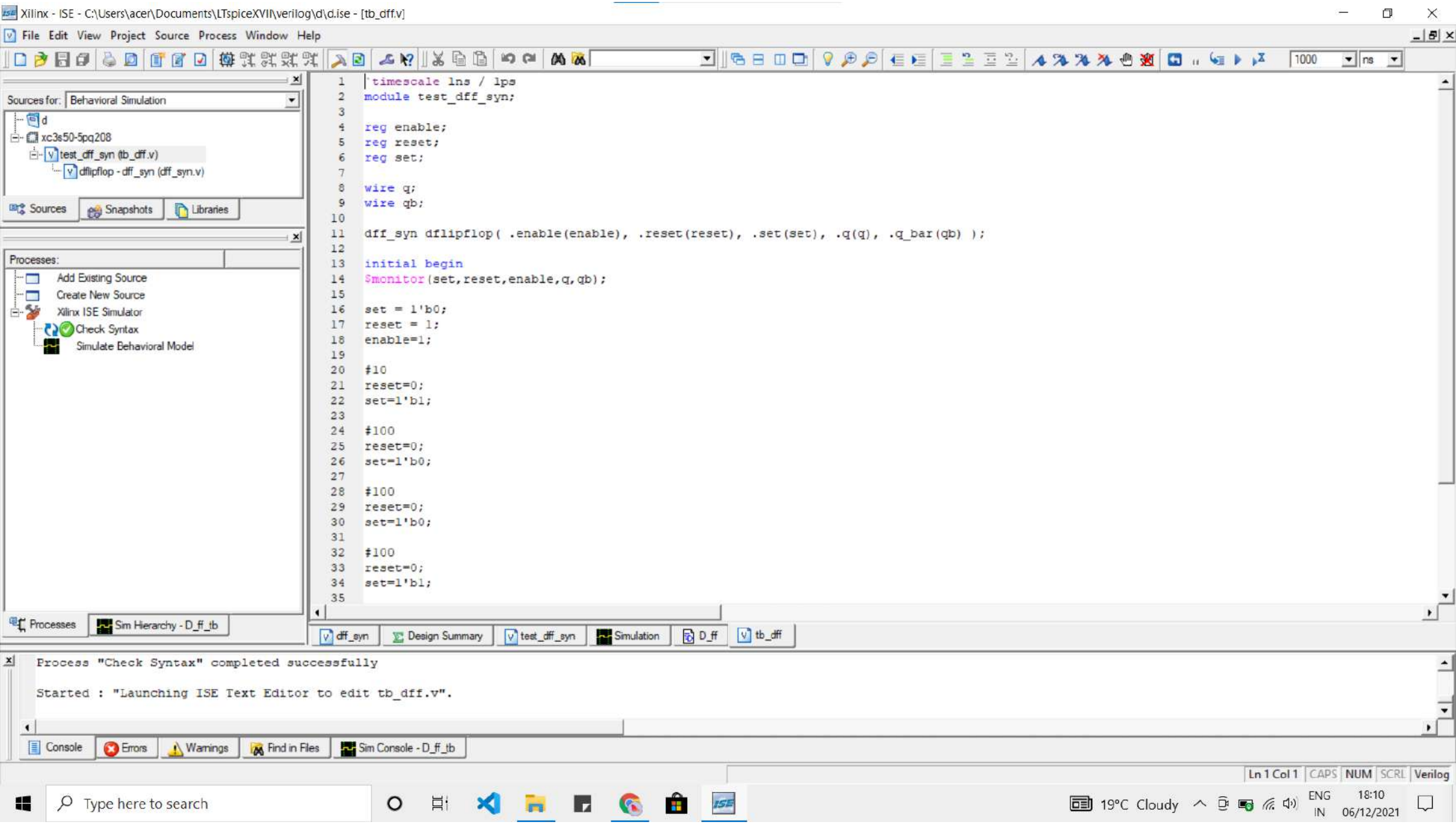

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [dff_syn.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
d
xc3s50-5pq208
test_dff_syn (tb_dff.v)
dflipflop - dff_syn (dff_syn.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Sim Hierarchy - D_ff_tb
1 `timescale 1ns / 1ps
2
3 module dff_syn (set,reset,enable,q,q_bar);
4
5 input set;
6 input enable;
7 input reset;
8
9 output q;
10 output q_bar;
11
12 reg q;
13
14 assign q_bar = ~q;
15
16 always @(posedge enable)
17 begin
18 if (reset) begin
19 q<=1'b0;
20 end
21 else begin
22 q<=set;
23 end
24 end
25 endmodule
dff_syn
Design Summary
test_dff_syn
Simulation
D_ff
tb_dff
Process "Check Syntax" completed successfully
Started : "Launching ISE Text Editor to edit tb_dff.v".
Console
Errors
Warnings
Find in Files
Sim Console - D_ff_tb
Ln 1 Col 1
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
18:10
06/12/2021

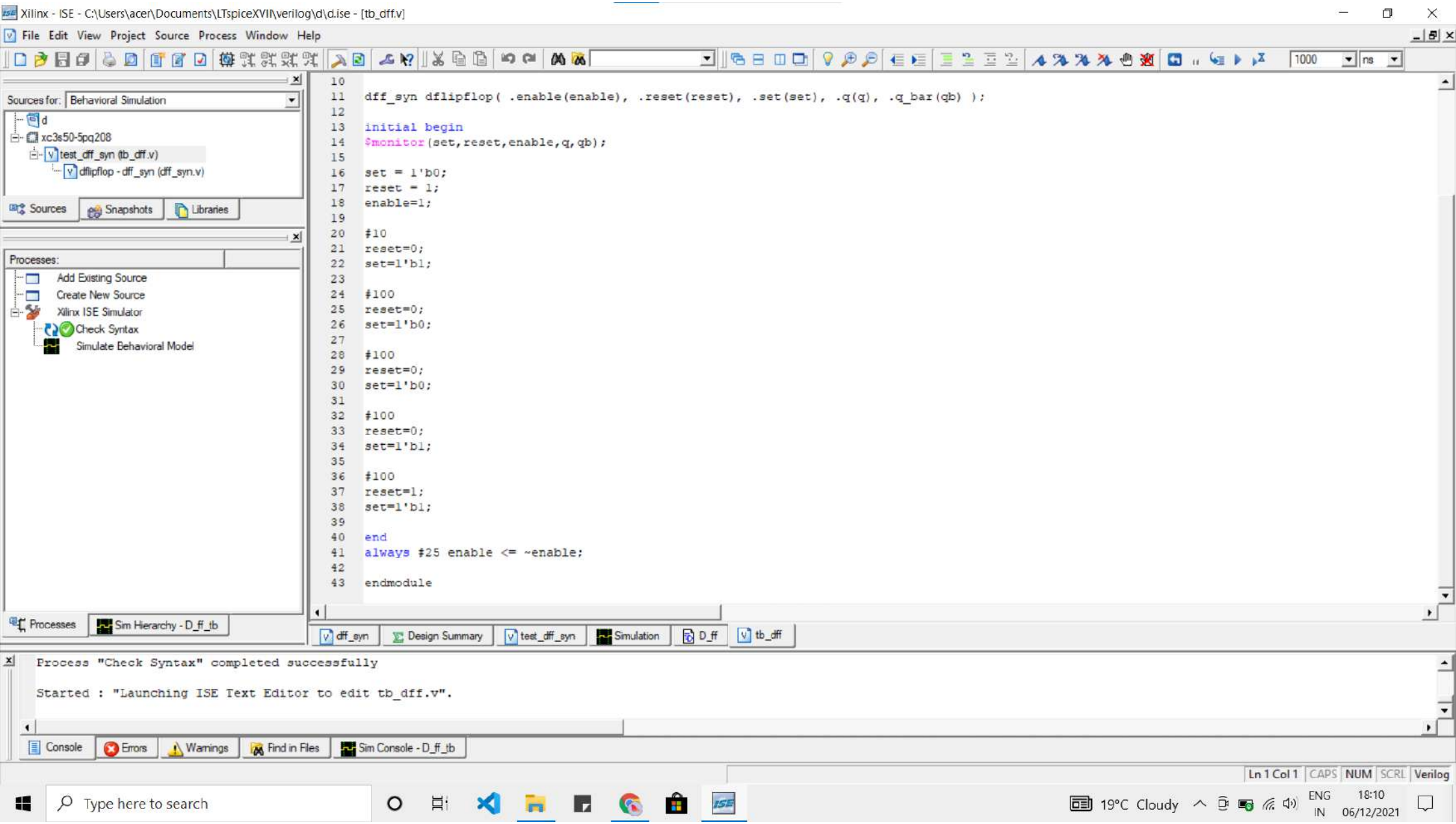
RTL schematic


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [dff_syn.ngr]
File Edit View Project Source Process Window Help
dff_syn
Snapshots
Libraries
Design
No flow available.
Processes
Sim Hierarchy - D_ff_tb
enable
reset
set
q
q_bar
dff_syn
Design Summary
test_dff_syn
Simulation
D_ff
tb_dff
dff_syn
Design Objects of
Top Level Symbol
Instances
Pins
Signals
Properties
No object is selected
Name
Value
Console
Errors
Warnings
Find in Files
Sim Console - D_ff_tb
View by Category
View by Name
[340,272]
Type here to search
19°C Cloudy
ENG
IN
18:11
06/12/2021

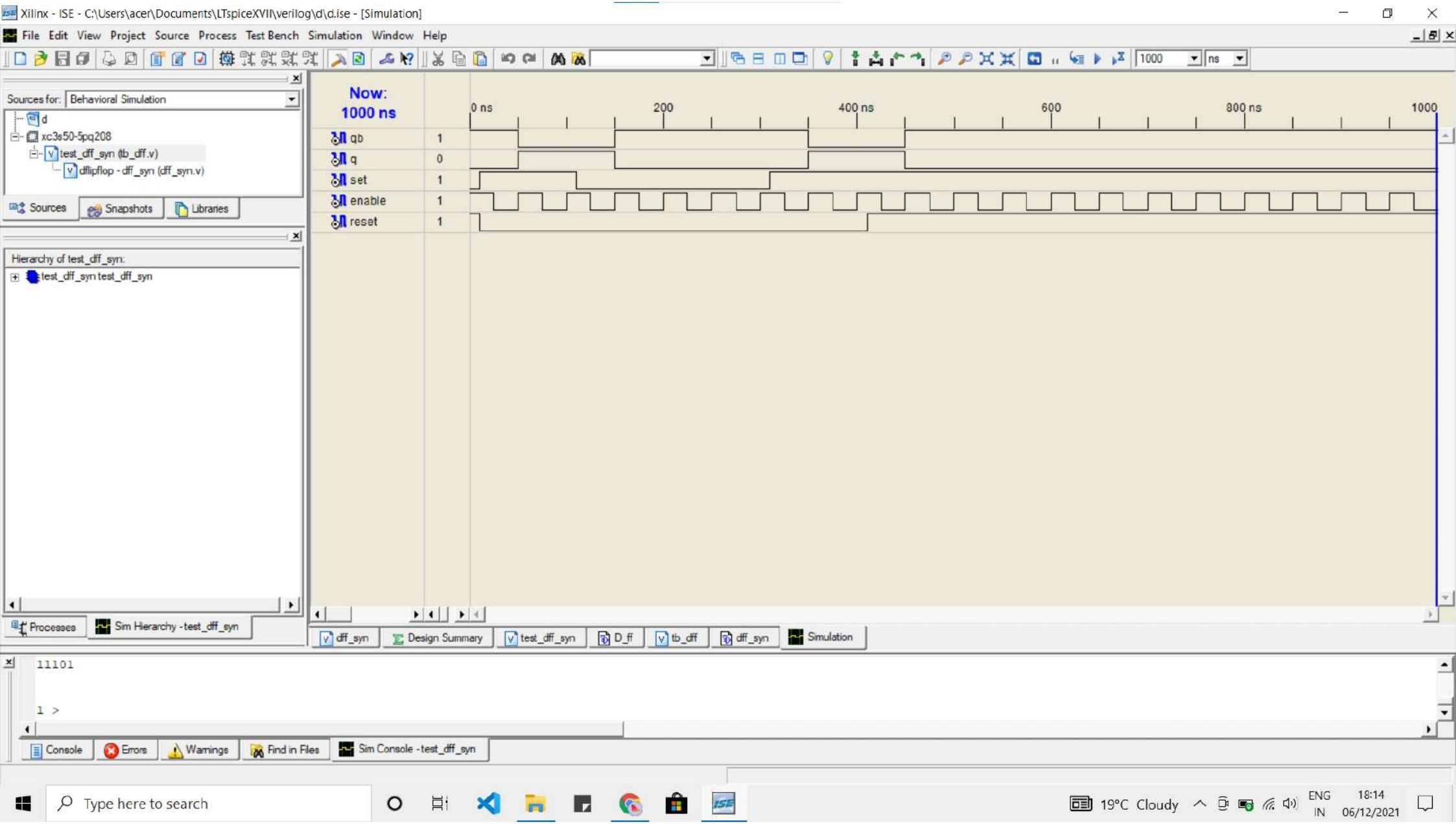

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [dff_syn.ngr]
File Edit View Project Source Process Window Help
dff_syn
Snapshots
Libraries
Design
No flow available.
Processes
Sim Hierarchy - D_ff_tb
FDR
set
D
Q
q
enable
C
R
reset
q
q_bar
q_bar
dff_syn
Design Summary
test_dff_syn
Simulation
D_ff
tb_dff
dff_syn
Design Objects of
dff_syn
Instances
Pins
Signals
Properties
No object is selected
Name
Value
Console
Errors
Warnings
Find in Files
Sim Console - D_ff_tb
View by Category
View by Name
[1216,712]
Type here to search
19°C Cloudy
ENG
IN
18:12
06/12/2021

writing the test bench


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [tb_dff.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
d
xc3s50-5pq208
test_dff_syn (tb_dff.v)
dflipflop - dff_syn (dff_syn.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Sim Hierarchy - D_ff_tb
1 `timescale 1ns / 1ps
2 module test_dff_syn;
3
4 reg enable;
5 reg reset;
6 reg set;
7
8 wire q;
9 wire qb;
10
11 dff_syn dflipflop(.enable(enable), .reset(reset), .set(set), .q(q), .q_bar(qb));
12
13 initial begin
14 $monitor(set,reset,enable,q,qb);
15
16 set = 1'b0;
17 reset = 1;
18 enable=1;
19
20 #10
21 reset=0;
22 set=1'b1;
23
24 #100
25 reset=0;
26 set=1'b0;
27
28 #100
29 reset=0;
30 set=1'b0;
31
32 #100
33 reset=0;
34 set=1'b1;
35
dff_syn
Design Summary
test_dff_syn
Simulation
D_ff
tb_dff
Process "Check Syntax" completed successfully
Started : "Launching ISE Text Editor to edit tb_dff.v".
Console
Errors
Warnings
Find in Files
Sim Console - D_ff_tb
Ln 1 Col 1
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
18:10
06/12/2021


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [tb_dff.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
d
xc3s50-5pq208
test_dff_syn (tb_dff.v)
dflipflop - dff_syn (dff_syn.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Sim Hierarchy - D_ff_tb
10
11 dff_syn dflipflop(.enable(enable), .reset(reset), .set(set), .q(q), .q_bar(qb));
12
13 initial begin
14 $monitor(set,reset,enable,q,qb);
15
16 set = 1'b0;
17 reset = 1;
18 enable=1;
19
20 #10
21 reset=0;
22 set=1'b1;
23
24 #100
25 reset=0;
26 set=1'b0;
27
28 #100
29 reset=0;
30 set=1'b0;
31
32 #100
33 reset=0;
34 set=1'b1;
35
36 #100
37 reset=1;
38 set=1'b1;
39
40 end
41 always #25 enable <= ~enable;
42
43 endmodule
dff_syn
Design Summary
test_dff_syn
Simulation
D_ff
tb_dff
Process "Check Syntax" completed successfully
Started : "Launching ISE Text Editor to edit tb_dff.v".
Console
Errors
Warnings
Find in Files
Sim Console - D_ff_tb
Ln 1 Col 1
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
18:10
06/12/2021

Simulations


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\d\d.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
d
xc3s50-5pq208
test_dff_syn (tb_dff.v)
dflipflop - dff_syn (dff_syn.v)
Sources
Snapshots
Libraries
Hierarchy of test_dff_syn:
test_dff_syn test_dff_syn
Processes
Sim Hierarchy - test_dff_syn
Now:
1000 ns
0 ns
200
400 ns
600
800 ns
1000
qb
q
set
enable
reset
1
0
dff_syn
Design Summary
test_dff_syn
D_ff
tb_dff
dff_syn
Simulation
11101
1 >
Console
Errors
Warnings
Find in Files
Sim Console - test_dff_syn
Type here to search
19°C Cloudy
ENG
IN
18:14
06/12/2021

Question 2
SR FLIP FLOP

TRUTH TABLE

Que. 2

⇒ SR flip-flop –

↳ Truth Table –

set	Reset	q	q-bar
0	0	0	1
0	1	0	1
1	0	1	0
1	1	invalid	invalid

writing the module

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [sr_flip.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- m
- xc3s50-5pq208
  - test_SR_flip (tb.v)
    - srflipflop - SR_flip (s.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator
  - Check Syntax
  - Simulate Behavioral Model

Processes

```
1  `timescale 1ns / 1ps
2
3  module SR_flip(s,r,clk,reset,q,q_bar);
4
5  input s,r,clk,reset;
6
7  output q,q_bar;
8
9  wire s,r,clk;
10 reg q,q_bar;
11
12 always @(posedge clk) begin
13
14 if (reset) begin
15 q=1'b0;
16 q_bar=1'b1;
17
18 end else begin
19
20 case({s,r})
21 {1'b0,1'b0}: begin q=q;q_bar=q_bar; end
22 {1'b0,1'b1}: begin q=1'b0;q_bar=1'b1; end
23 {1'b1,1'b0}: begin q=1'b1;q_bar=1'b0; end
24 {1'b1,1'b1}: begin q=1'bx; q_bar=1'bx; end
25 endcase
26
27 end
28
29 end
30 endmodule
```

Design Summary | sr_flip | SR_flip | SR_flip | test_sr_flip

```
Running ISim simulation engine ...

Started : "Launching ISE Text Editor to edit tb.v".
```

Console | Errors | Warnings | Find in Files

Ln 42 Col 8 | CAPS | NUM | SCRL | Verilog

Type here to search

19°C Cloudy

ENG IN 17:51 06/12/2021

RTL schematic

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [SR_flip.ngr]

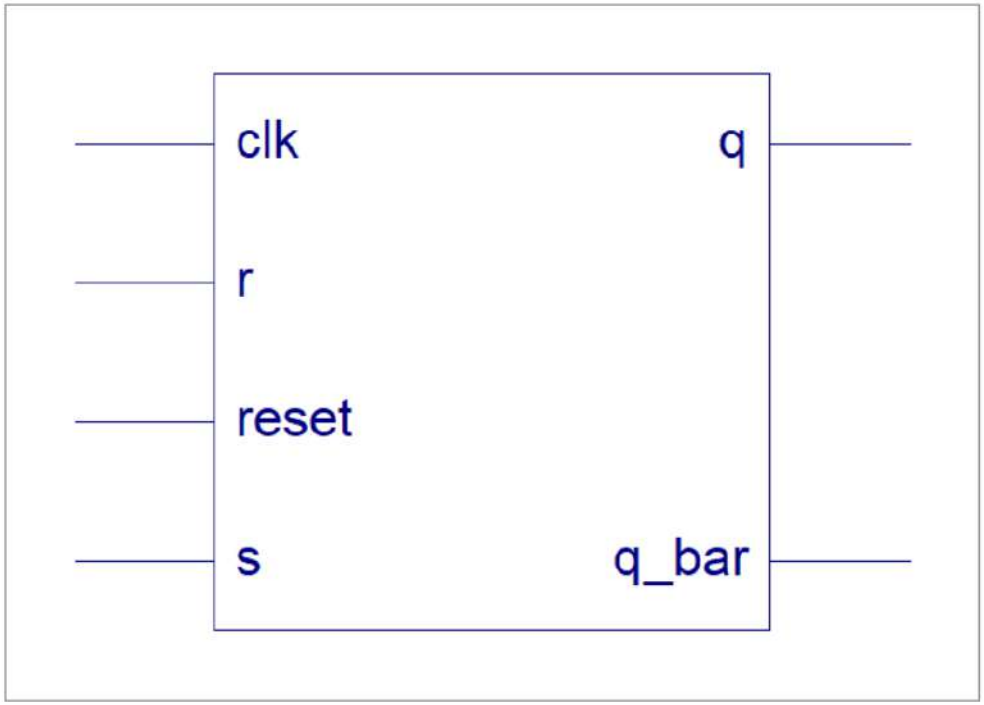
File Edit View Project Source Process Window Help

SR_flip

Snapshots Libraries Design

No flow available.

Processes



Design Summary | sr_flip | SR_flip | SR_flip | test_sr_flip

Design Objects of Top Level Symbol

Instances	Pins	Signals

Properties
No object is selected

Name	Value

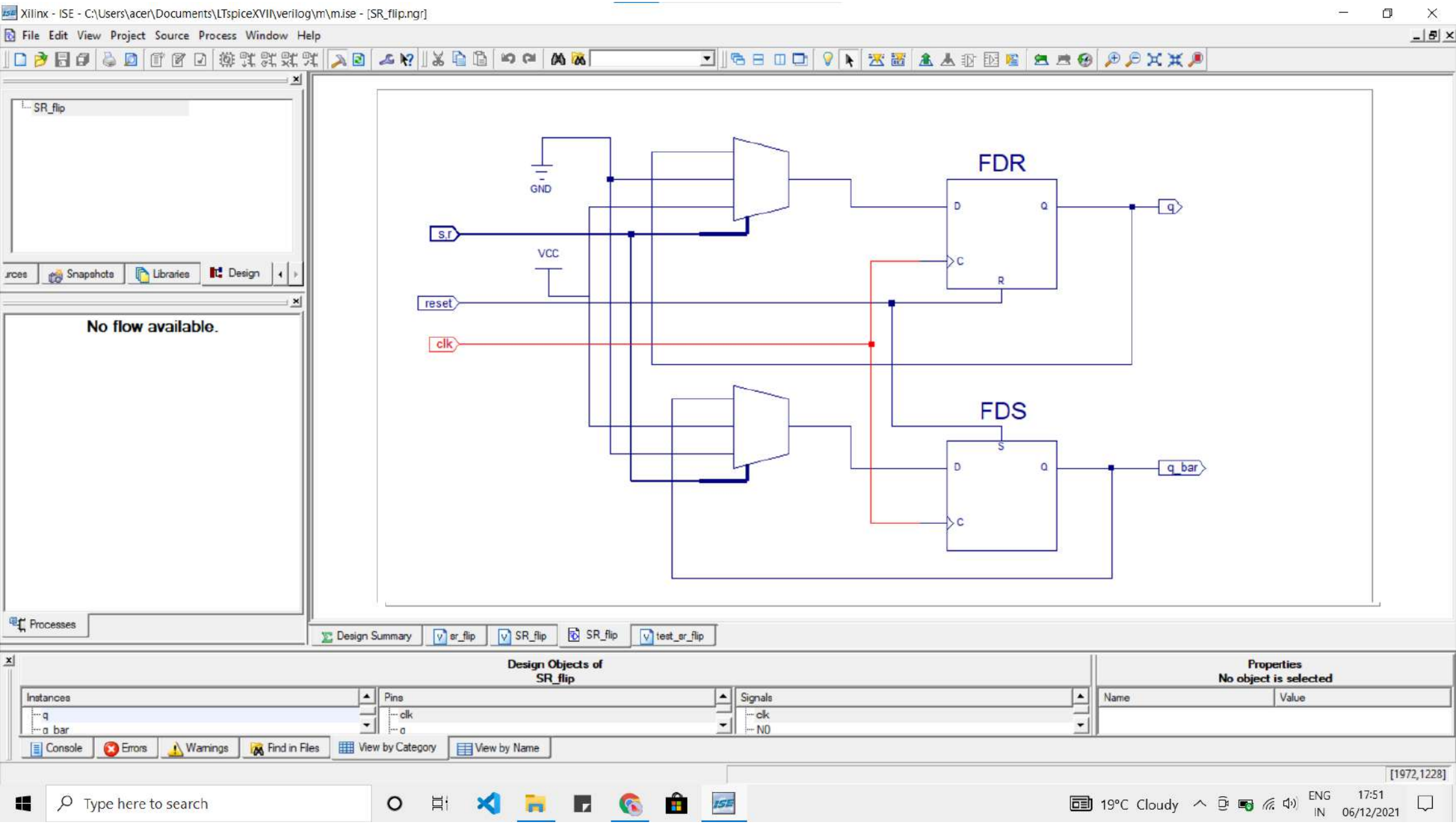
Console | Errors | Warnings | Find in Files | View by Category | View by Name

[432,296]

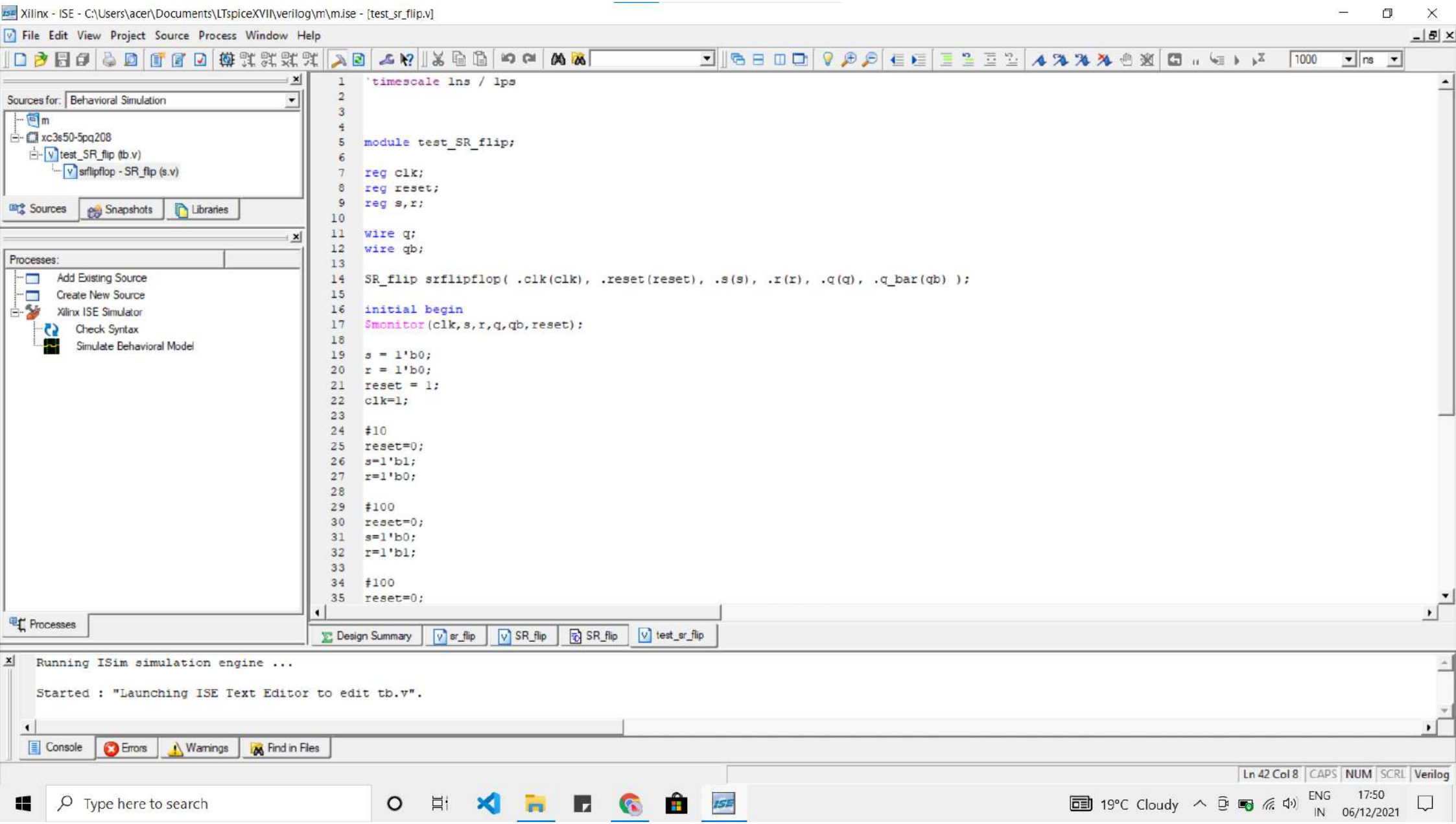
Type here to search

19°C Cloudy

ENG IN 17:51 06/12/2021


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [SR_flip.ngr]
File Edit View Project Source Process Window Help
SR_flip
Snapshots
Libraries
Design
No flow available.
Processes
GND
VCC
s_r
reset
clk
FDR
D
Q
C
R
q
FDS
S
D
Q
C
q_bar
Design Summary
sr_flip
SR_flip
SR_flip
test_sr_flip
Design Objects of SR_flip
Instances
q
q_bar
Pins
clk
q
Signals
clk
N0
Properties
No object is selected
Name
Value
Console
Errors
Warnings
Find in Files
View by Category
View by Name
[1972,1228]
Type here to search
19°C Cloudy
ENG
IN
17:51
06/12/2021

writing the test bench


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [test_sr_flip.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
m
xc3s50-5pq208
test_SR_flip (tb.v)
srflipflop - SR_flip (s.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
1 `timescale 1ns / 1ps
2
3
4 module test_SR_flip;
5
6 reg clk;
7 reg reset;
8 reg s,r;
9
10 wire q;
11 wire qb;
12
13 SR_flip srflipflop(.clk(clk), .reset(reset), .s(s), .r(r), .q(q), .q_bar(qb));
14
15 initial begin
16 $monitor(clk,s,r,q,qb,reset);
17
18 s = 1'b0;
19 r = 1'b0;
20 reset = 1;
21 clk=1;
22
23 #10
24 reset=0;
25 s=1'b1;
26 r=1'b0;
27
28 #100
29 reset=0;
30 s=1'b0;
31 r=1'b1;
32
33 #100
34 reset=0;
35
Design Summary
sr_flip
SR_flip
SR_flip
test_sr_flip
Running ISim simulation engine ...
Started : "Launching ISE Text Editor to edit tb.v".
Console
Errors
Warnings
Find in Files
Ln 42 Col 8
CAPS
NUM
SCRL
Verilog
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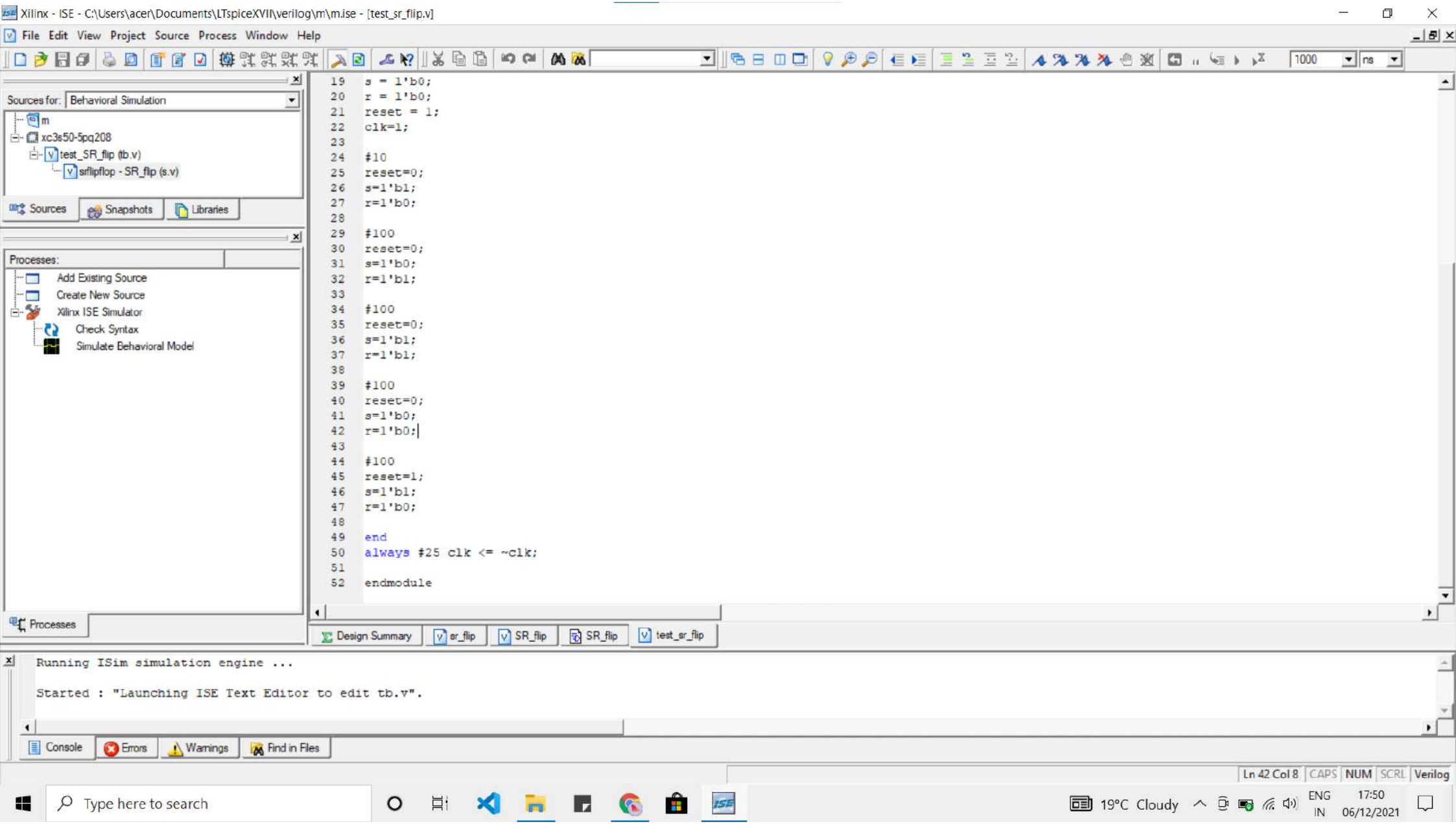
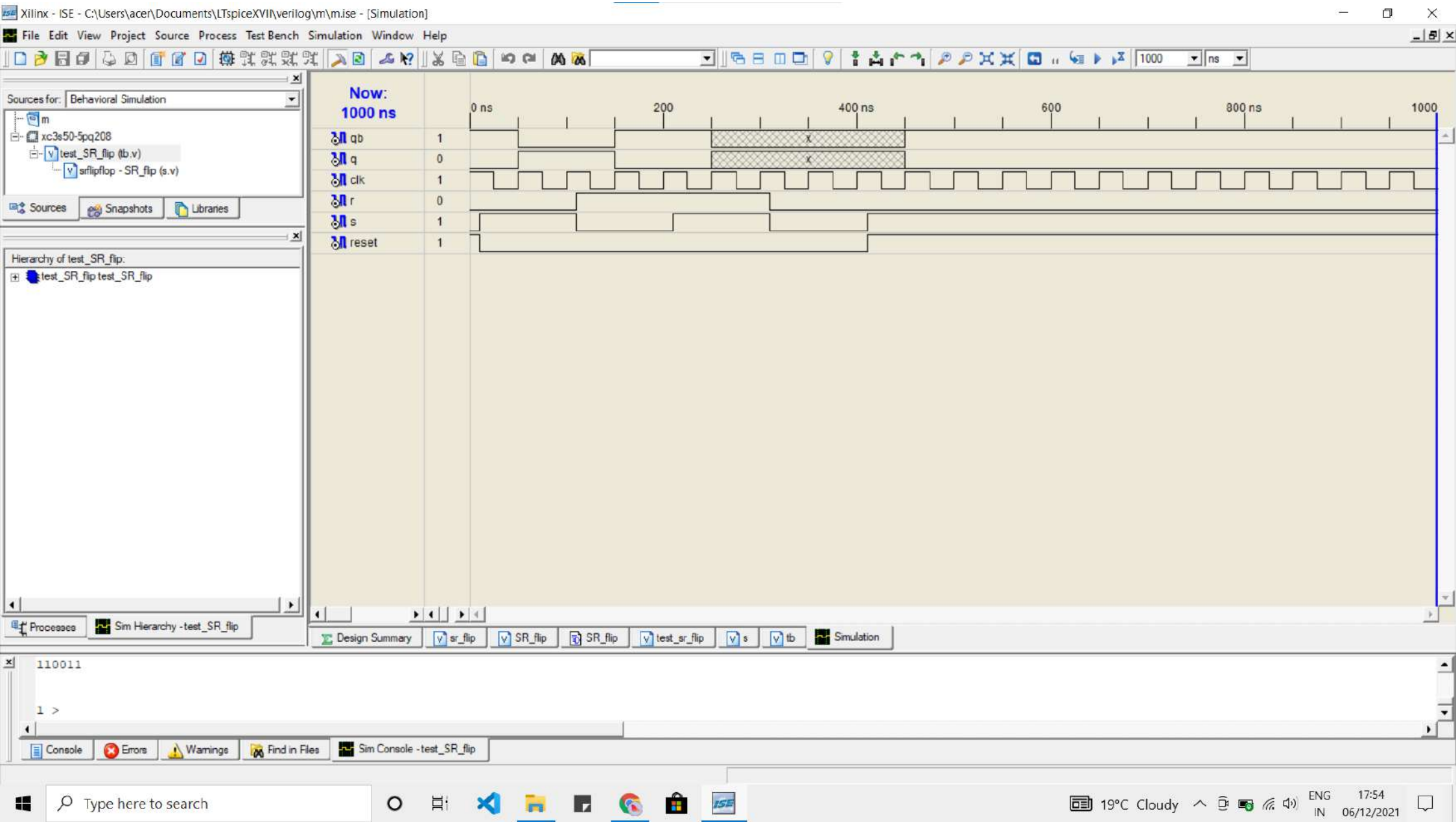
19°C Cloudy
ENG
IN
17:50
06/12/2021


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [test_sr_flip.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
m
xc3s50-5pq208
test_SR_flip (tb.v)
srflipflop - SR_flip (s.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
19 s = 1'b0;
20 r = 1'b0;
21 reset = 1;
22 clk=1;
23
24 #10
25 reset=0;
26 s=1'b1;
27 r=1'b0;
28
29 #100
30 reset=0;
31 s=1'b0;
32 r=1'b1;
33
34 #100
35 reset=0;
36 s=1'b1;
37 r=1'b1;
38
39 #100
40 reset=0;
41 s=1'b0;
42 r=1'b0;
43
44 #100
45 reset=1;
46 s=1'b1;
47 r=1'b0;
48
49 end
50 always #25 clk <= ~clk;
51
52 endmodule
Design Summary
sr_flip
SR_flip
SR_flip
test_sr_flip
Running ISim simulation engine ...
Started : "Launching ISE Text Editor to edit tb.v".
Console
Errors
Warnings
Find in Files
Ln 42 Col 8
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
17:50
06/12/2021

Simulations


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\m\m.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
m
xc3s50-5pq208
test_SR_flip (tb.v)
srflipflop - SR_flip (s.v)
Sources
Snapshots
Libraries
Hierarchy of test_SR_flip:
test_SR_flip test_SR_flip
Processes
Sim Hierarchy - test_SR_flip
Now:
1000 ns
0 ns
200
400 ns
600
800 ns
1000
qb
q
clk
r
s
reset
Design Summary
sr_flip
SR_flip
SR_flip
test_sr_flip
s
tb
Simulation
110011
1 >
Console
Errors
Warnings
Find in Files
Sim Console - test_SR_flip
Type here to search
19°C Cloudy
ENG
IN
17:54
06/12/2021

Question 3
SR_to_JK
FLIP FLOP

TRUTH TABLE

Que. 3

⇒ SR_to_JK flipflop –

(*) for this conversion we used two and gates at the input of our Que.2 SR flip-flop

↳ Truth-Table –

J	K	q	q-bar
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	0

writing the module

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [sr_to_jk.v*]

File Edit View Project Source Process Window Help

Sources for: Synthesis/Implementation

- jk
- xc3s50-5pq208
  - sr_to_jk (sr_to_jk.v)
    - sr - SR_flip (sr_to_jk.v)

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- View Design Summary
- Design Utilities
- User Constraints
- Synthesize - XST
  - View Synthesis Report
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File

Processes | Sim Hierarchy - tt_v

```
1  `timescale 1ns / 1ps
2  module SR_flip(s,r,clk,reset,q,q_bar);
3  input s,r,clk,reset;
4  output q,q_bar;
5
6  reg q,q_bar;
7
8  always @(posedge clk) begin
9  if (reset) begin
10 q=1'b0;
11 q_bar=1'b1;
12 end else begin
13 case({s,r})
14 {1'b0,1'b0}: begin q=q;q_bar=q_bar; end
15 {1'b0,1'b1}: begin q=1'b0;q_bar=1'b1; end
16 {1'b1,1'b0}: begin q=1'b1;q_bar=1'b0; end
17 {1'b1,1'b1}: begin q=1'bx; q_bar=1'bx; end
18 endcase
19 end
20 end
21 endmodule
22
23
24 module sr_to_jk(k,j,clk,reset,q,q_bar);
25 input k,j,clk,reset;
26 output q,q_bar;
27
28
29 SR_flip sr(s,r,clk,reset,q,q_bar);
30
31 and gate2(r,k,q);
32 and gate3(s,j,q_bar);
33
34
35 endmodule
```

Design Summary | sr_to_jk | Synthesis Repor... | sr_to_jk | test_sr_to_jk | Simulation | test_sr_to_jk

```
Process "Check Syntax" completed successfully
```

Console | Errors | Warnings | Find in Files | Sim Console - tt_v

Ln 28 Col 1 | CAPS | NUM | SCRL | Verilog

Type here to search

19°C Cloudy

ENG IN 22:55 07/12/2021

RTL schematic

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [sr_to_jk.ngr]

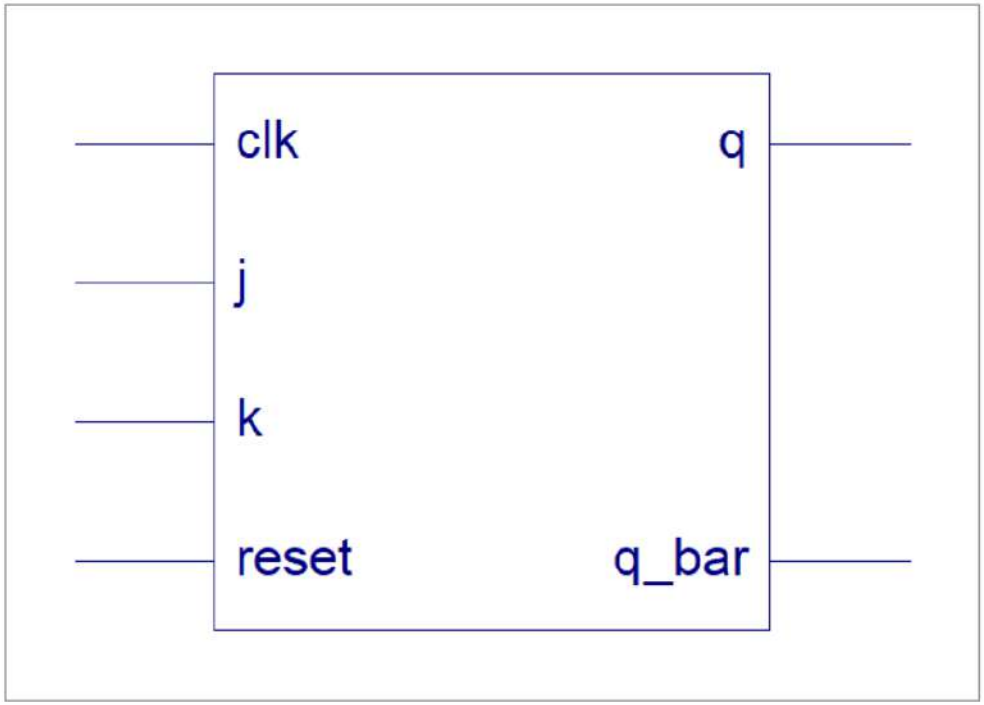
File Edit View Project Source Process Window Help

sr_to_jk
sr

Snapshots Libraries Design

Hierarchy of tt_v:
tt_v tt_v

Processes Sim Hierarchy - tt_v



Design Summary sr_to_jk Synthesis Repor... sr_to_jk test_sr_to_jk Simulation

Design Objects of Top Level Symbol

Instances	Pins	Signals

Properties
No object is selected

Name	Value

Console Errors Warnings Find in Files Sim Console - tt_v View by Category View by Name

[456,352]

Type here to search

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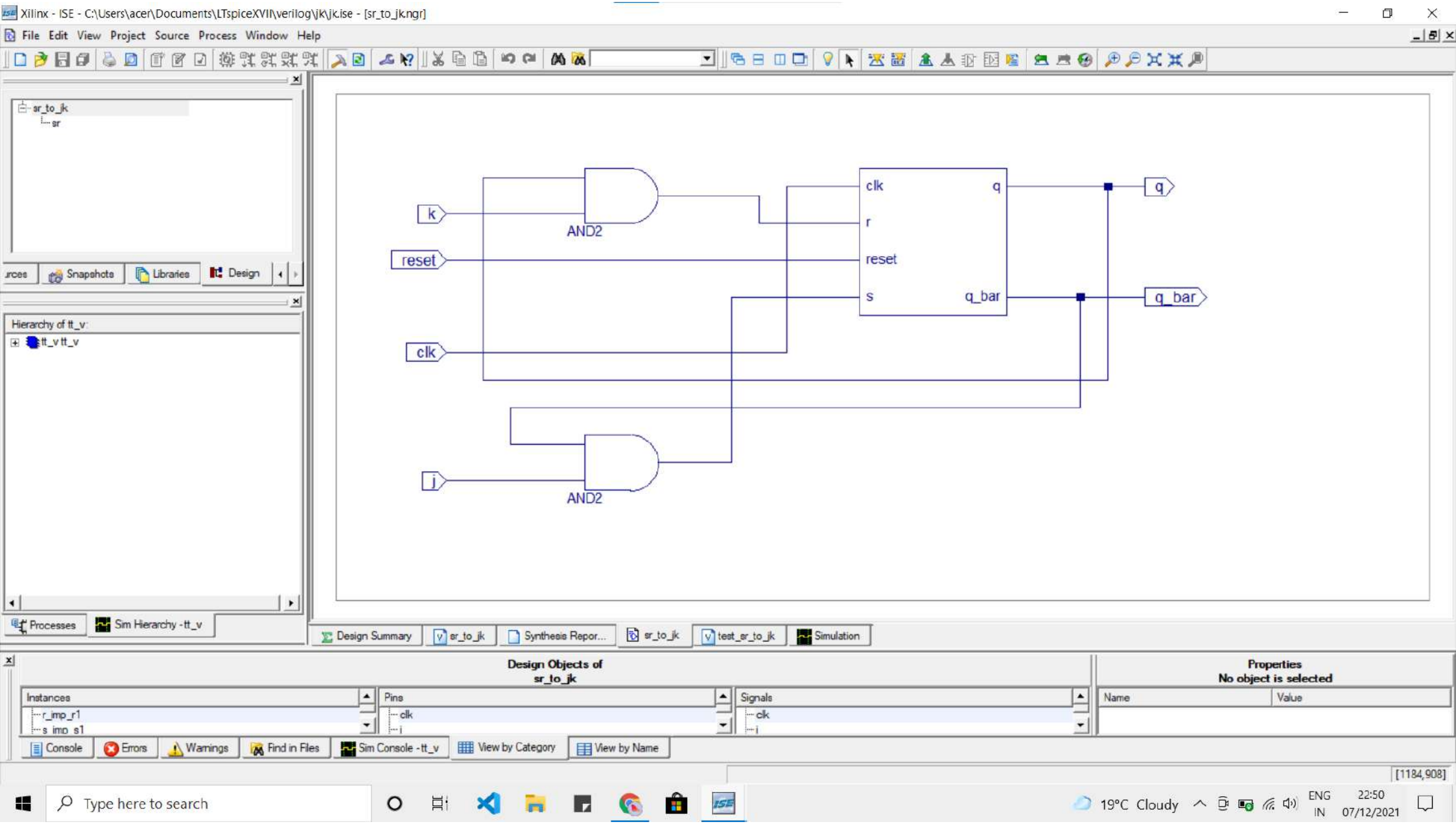
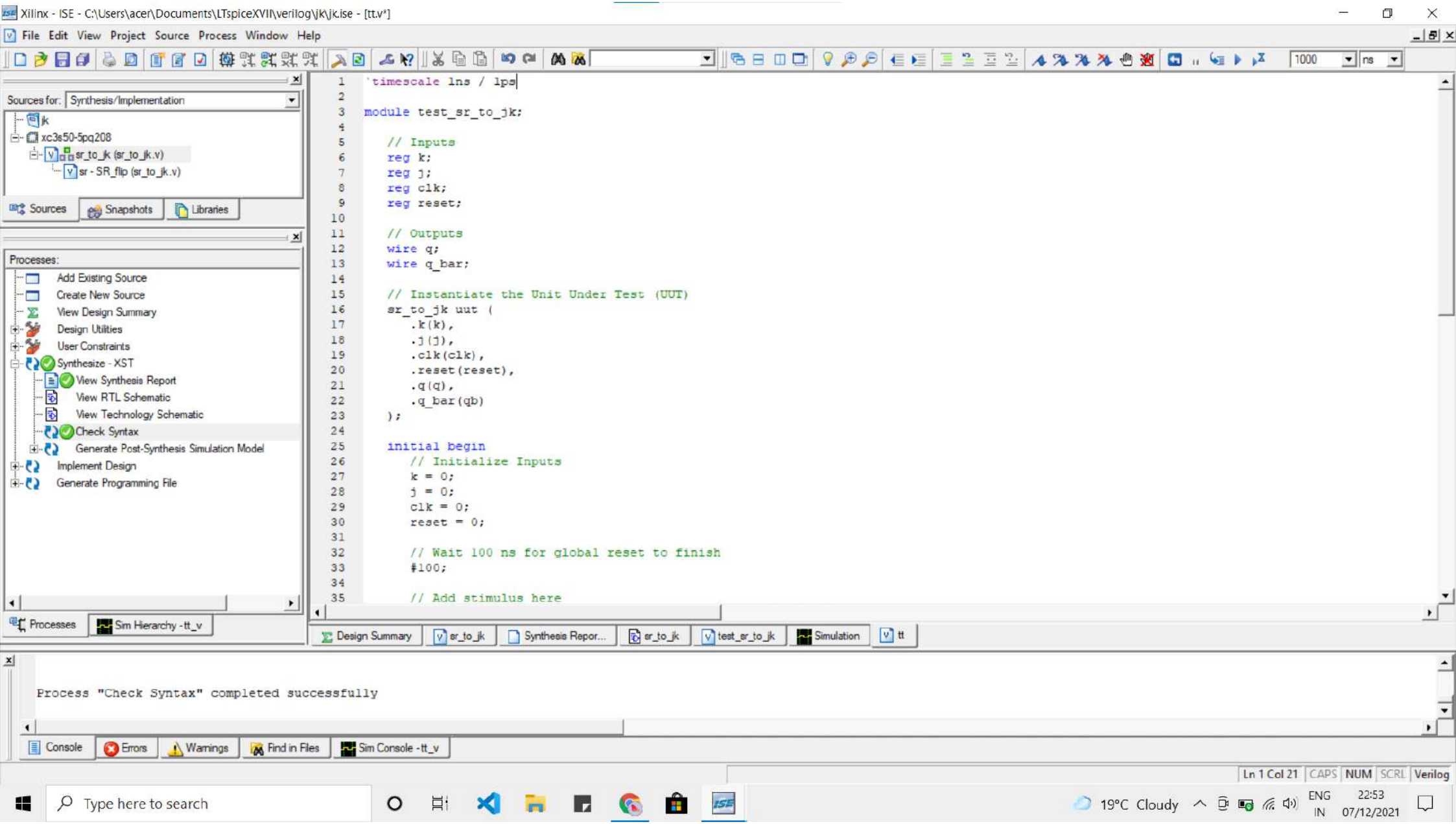
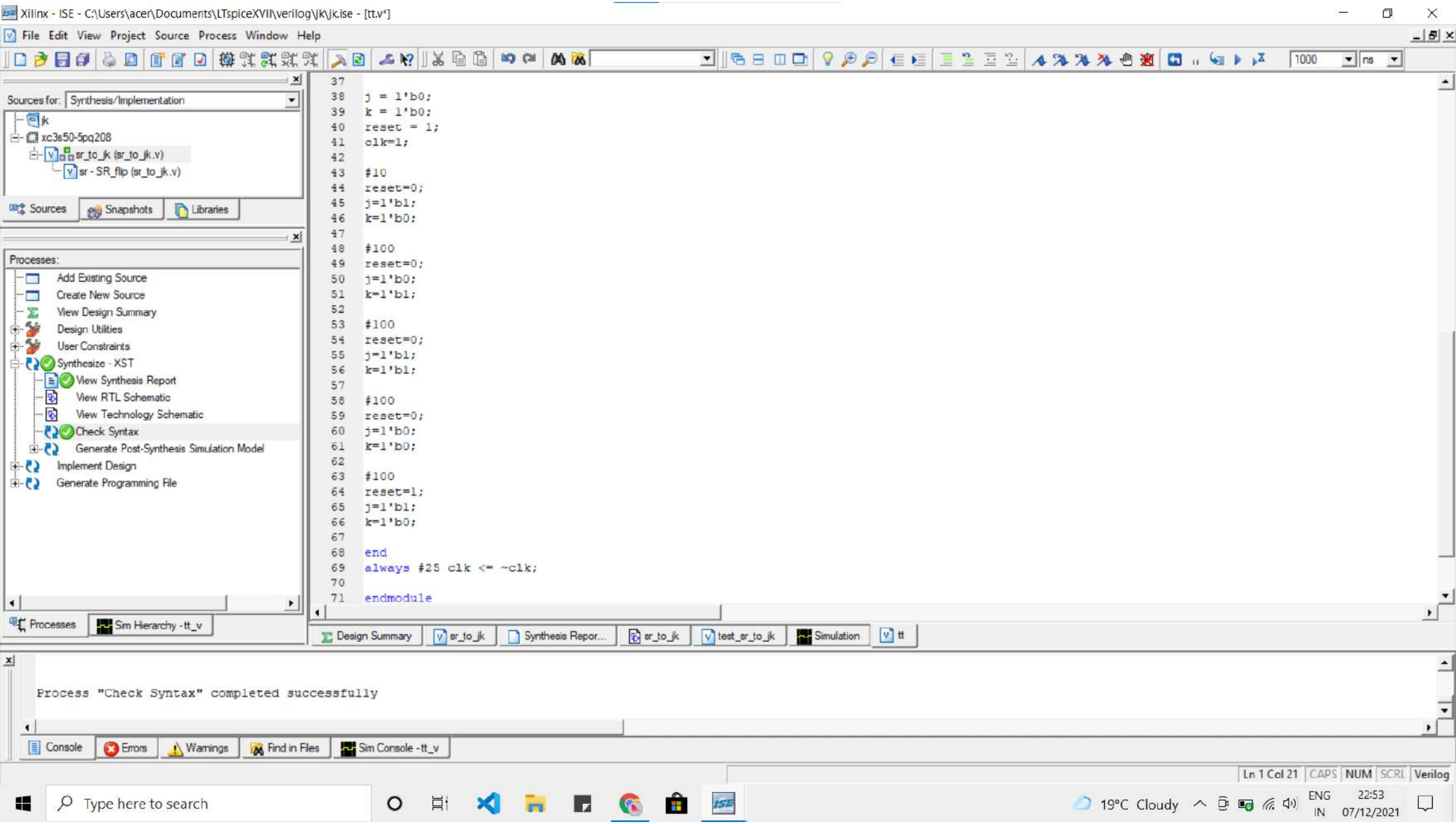
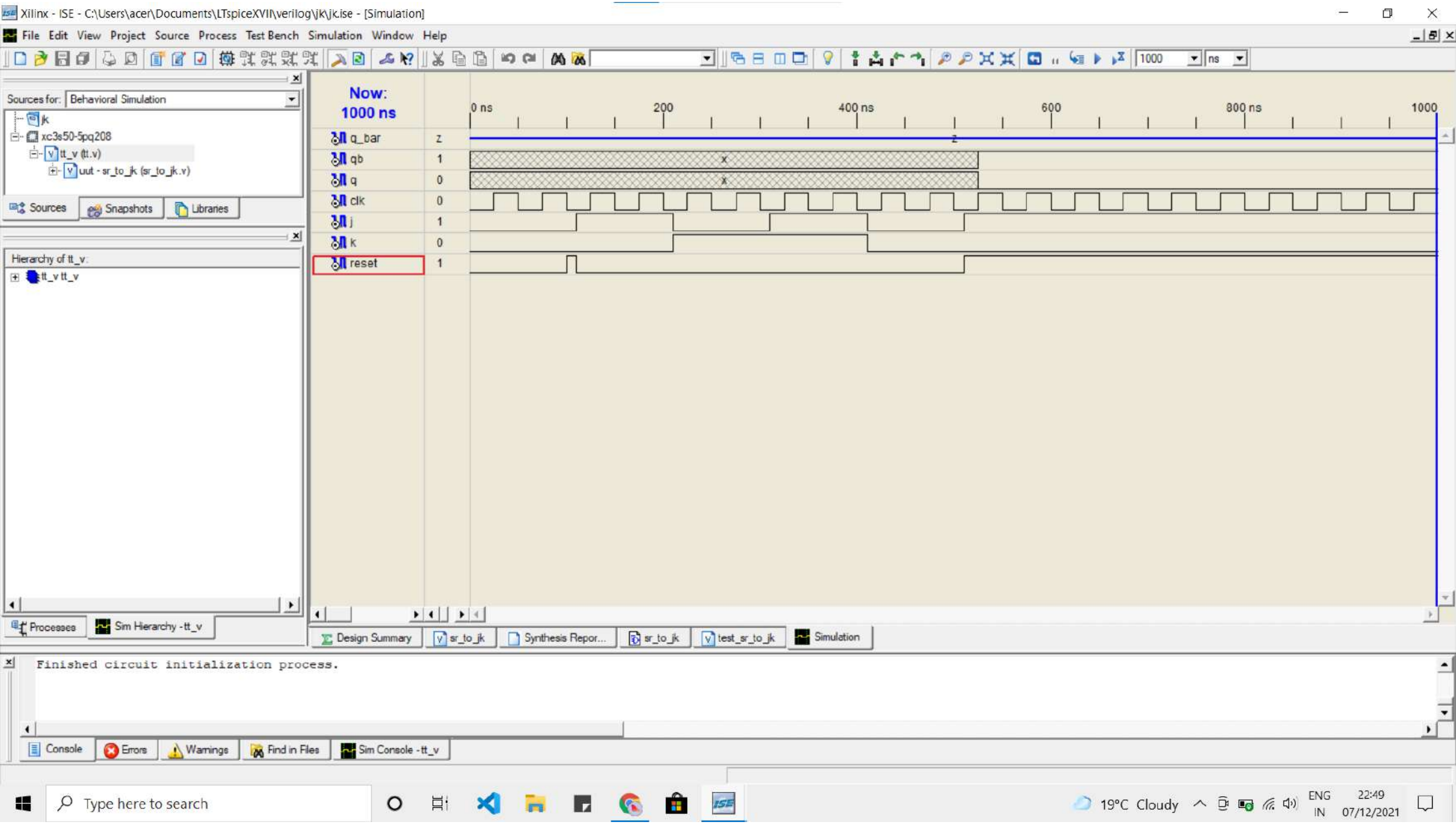

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [sr_to_jk.ngr]
File Edit View Project Source Process Window Help
sr_to_jk
sr
Snapshots
Libraries
Design
Hierarchy of tt_v:
tt_v tt_v
Processes
Sim Hierarchy - tt_v
k
reset
clk
j
AND2
AND2
clk
r
reset
s
q
q_bar
q
q_bar
Design Summary
sr_to_jk
Synthesis Repor...
sr_to_jk
test_sr_to_jk
Simulation
Design Objects of sr_to_jk
Instances
r_imp_r1
s_imp_s1
Pins
clk
j
Signals
clk
j
Properties
No object is selected
Name
Value
Console
Errors
Warnings
Find in Files
Sim Console - tt_v
View by Category
View by Name
[1184,908]
Type here to search
19°C Cloudy
ENG
IN
22:50
07/12/2021

writing the test bench


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [tt.v*]
File Edit View Project Source Process Window Help
Sources for: Synthesis/Implementation
jk
xc3s50-5pq208
sr_to_jk (sr_to_jk.v)
sr - SR_flip (sr_to_jk.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
View Synthesis Report
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Implement Design
Generate Programming File
Processes
Sim Hierarchy - tt_v
1 `timescale 1ns / 1ps
2
3 module test_sr_to_jk;
4
5 // Inputs
6 reg k;
7 reg j;
8 reg clk;
9 reg reset;
10
11 // Outputs
12 wire q;
13 wire q_bar;
14
15 // Instantiate the Unit Under Test (UUT)
16 sr_to_jk uut (
17 .k(k),
18 .j(j),
19 .clk(clk),
20 .reset(reset),
21 .q(q),
22 .q_bar(qb)
23);
24
25 initial begin
26 // Initialize Inputs
27 k = 0;
28 j = 0;
29 clk = 0;
30 reset = 0;
31
32 // Wait 100 ns for global reset to finish
33 #100;
34
35 // Add stimulus here
Design Summary
sr_to_jk
Synthesis Repor...
sr_to_jk
test_sr_to_jk
Simulation
tt
Process "Check Syntax" completed successfully
Console
Errors
Warnings
Find in Files
Sim Console - tt_v
Ln 1 Col 21
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
22:53
07/12/2021


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [tt.v*]
File Edit View Project Source Process Window Help
Sources for: Synthesis/Implementation
jk
xc3s50-5pq208
sr_to_jk (sr_to_jk.v)
sr - SR_flip (sr_to_jk.v)
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
View Synthesis Report
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Implement Design
Generate Programming File
Processes
Sim Hierarchy - tt_v
37
38 j = 1'b0;
39 k = 1'b0;
40 reset = 1;
41 clk=1;
42
43 #10
44 reset=0;
45 j=1'b1;
46 k=1'b0;
47
48 #100
49 reset=0;
50 j=1'b0;
51 k=1'b1;
52
53 #100
54 reset=0;
55 j=1'b1;
56 k=1'b1;
57
58 #100
59 reset=0;
60 j=1'b0;
61 k=1'b0;
62
63 #100
64 reset=1;
65 j=1'b1;
66 k=1'b0;
67
68 end
69 always #25 clk <= ~clk;
70
71 endmodule
Design Summary
sr_to_jk
Synthesis Repor...
sr_to_jk
test_sr_to_jk
Simulation
tt
Process "Check Syntax" completed successfully
Console
Errors
Warnings
Find in Files
Sim Console - tt_v
Ln 1 Col 21
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
22:53
07/12/2021

Simulations


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\jk\jk.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
jk
xc3s50-5pq208
tt_v (tt.v)
uut - sr_to_jk (sr_to_jk.v)
Sources
Snapshots
Libraries
Hierarchy of tt_v:
tt_v tt_v
Processes
Sim Hierarchy - tt_v
Now:
1000 ns
0 ns
200
400 ns
600
800 ns
1000
q_bar
qb
q
clk
j
k
reset
Design Summary
sr_to_jk
Synthesis Repor...
sr_to_jk
test_sr_to_jk
Simulation
Finished circuit initialization process.
Console
Errors
Warnings
Find in Files
Sim Console - tt_v
Type here to search
19°C Cloudy
ENG
IN
22:49
07/12/2021

Question 4
UP_DOWN_WITH SR_to_JK FLIP FLOP

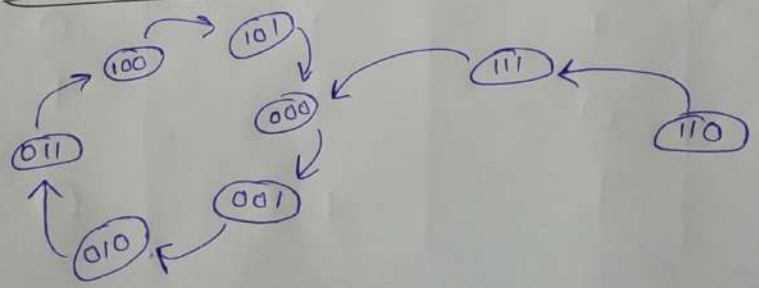
TRUTH TABLE

Que. 4

⇒ Synchronous Mod-6 up-down counter from SR_to_JK flip flop.

Present			Next			Inputs					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J	K
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1

↳ state diagram —



writing the module

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [UP_DOWN_with_sr_to_jk.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- ccc
- xc3s50-5pq208
  - test_UP_DOWN_WITH_sr_to_jk_v (test_UP_DOWN

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator
  - Check Syntax
  - Simulate Behavioral Model

Processes | Sim Hierarchy - test_UP_DOWN_W

```
1  `timescale 1ns / 1ps
2  module UP_DOWN_WITH_sr_to_jk(j,k,clk,reset,q3,q3_b);
3  output q3,q3_b;
4  input j,k,clk,reset;
5
6  sr_to_jk g1(j,k,clk,reset,q,q_bar);
7  and a1(j2,q,q3_b);
8
9  sr_to_jk g2(j2,q,clk,reset,q2,q2_b);
10 and a2(j3,q2,q);
11
12
13 sr_to_jk g3(j3,q,clk,reset,q3,q3_b);
14 endmodule
15
16 module SR_ff(s,r,clk,reset,q,q_bar);
17 input s,r,clk,reset;
18 output q,q_bar;
19
20 reg q,q_bar;
21
22 always @(posedge clk) begin
23 if (reset) begin
24 q=1'b0;
25 q_bar=1'b1;
26 end else begin
27 case({s,r})
28 {1'b0,1'b0}: begin q=q;q_bar=q_bar; end
29 {1'b0,1'b1}: begin q=1'b0;q_bar=1'b1; end
30 {1'b1,1'b0}: begin q=1'b1;q_bar=1'b0; end
31 {1'b1,1'b1}: begin q=1'bx; q_bar=1'bx; end
32 endcase
33 end
34 end
35 endmodule
```

Design Summary | test_UP_DOWN_WI... | UP_DOWN_with_sr... | Simulation | Synthesis Repor... | UP_DOWN_WITH_sr...

```
Parsing C:/Xilinx/verilog/src/glbl.v: 0.01

Process "Check Syntax" completed successfully
```

Console | Errors | Warnings | Find in Files | Sim Console - test_UP_DOWN_WITH_sr_to_jk_v

[1376,1396] CAPS NUM SCRL Verilog

Type here to search

19°C Cloudy

ENG IN 22:19 09/12/2021

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [UP_DOWN_with_sr_to_jk.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- ccc
- xc3s50-5pq208
  - test_UP_DOWN_WITH_sr_to_jk_v (test_UP_DOWN

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator
  - Check Syntax
  - Simulate Behavioral Model

Processes | Sim Hierarchy - test_UP_DOWN_W

```
20  reg q,q_bar;
21
22  always @(posedge clk) begin
23  if (reset) begin
24  q=1'b0;
25  q_bar=1'b1;
26  end else begin
27  case({s,r})
28  {1'b0,1'b0}: begin q=q;q_bar=q_bar; end
29  {1'b0,1'b1}: begin q=1'b0;q_bar=1'b1; end
30  {1'b1,1'b0}: begin q=1'b1;q_bar=1'b0; end
31  {1'b1,1'b1}: begin q=1'bx; q_bar=1'bx; end
32  endcase
33  end
34  end
35  endmodule
36
37
38  module sr_to_jk(k,j,clk,reset,q,q_bar);
39  input k,j,clk,reset;
40  output q,q_bar;
41
42
43
44  SR_ff sr(s,r,clk,reset,q,q_bar);
45
46  and gate2(r,k,q);
47  and gate3(s,j,q_bar);
48
49  endmodule
50
51
52
53
```

Design Summary | test_UP_DOWN_WI... | UP_DOWN_with_sr... | Simulation | Synthesis Repor... | UP_DOWN_WITH_sr...

```
Parsing C:/Xilinx/verilog/src/glbl.v: 0.01

Process "Check Syntax" completed successfully
```

Console | Errors | Warnings | Find in Files | Sim Console - test_UP_DOWN_WITH_sr_to_jk_v

[1376,1396] CAPS NUM SCRL Verilog

Type here to search

19°C Cloudy

ENG IN 22:19 09/12/2021

RTL schematic

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [UP_DOWN_WITH_sr_to_jk.ngr]

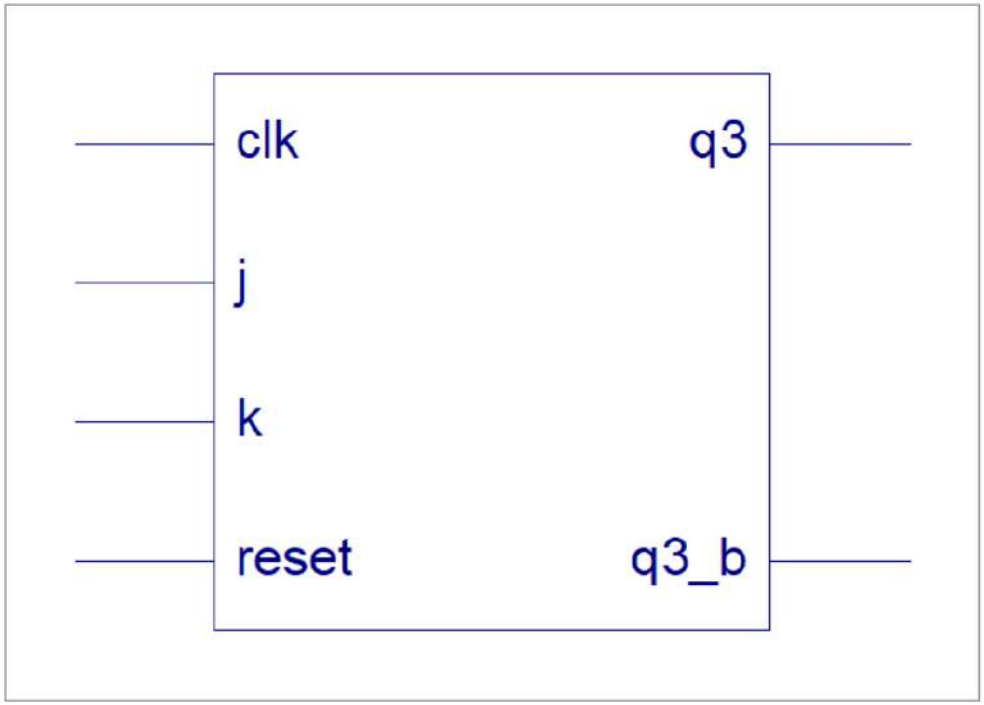
File Edit View Project Source Process Window Help

UP_DOWN_WITH_sr_to_jk
- g1
- g2
- g3

Snapshots | Libraries | Design

No flow available.

Processes | Sim Hierarchy - test_UP_DOWN_W...



Design Summary | test_UP_DOWN_WI... | UP_DOWN_with_sr... | Simulation | Synthesis Repor... | UP_DOWN_WITH_sr...

Design Objects of Top Level Symbol

Instances	Pins	Signals

Properties
No object is selected

Name	Value

Console | Errors | Warnings | Find in Files | Sim Console - test_UP_DOWN_WITH_sr_to_jk_v | View by Category | View by Name

[360,348]

Type here to search

19°C Cloudy

ENG IN 22:17 09/12/2021

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [UP_DOWN_WITH_sr_to_jk.ngr]

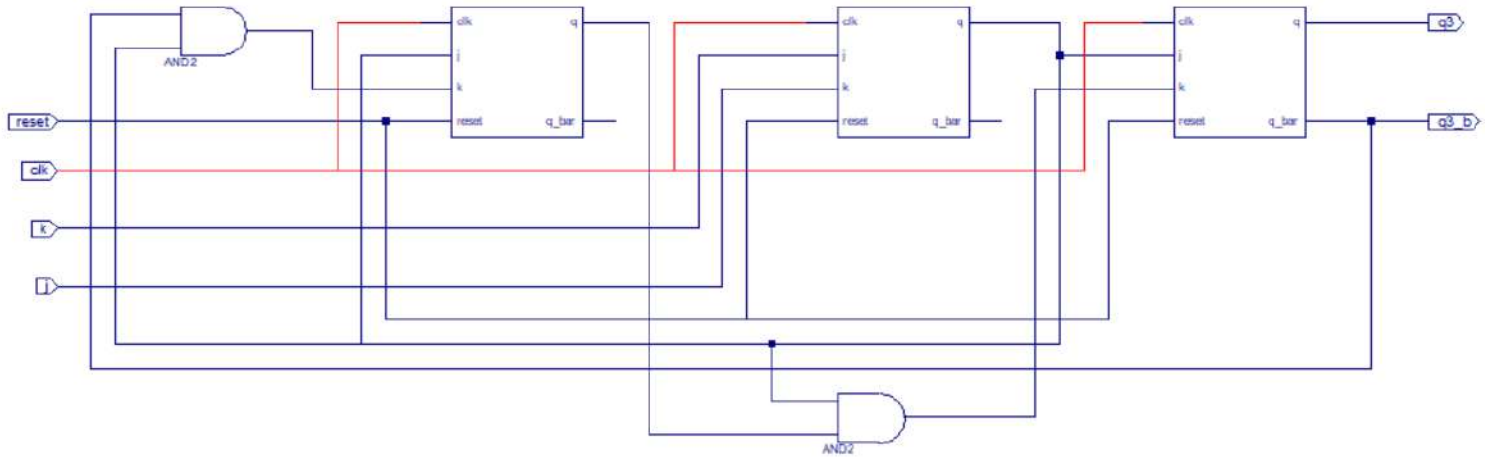
File Edit View Project Source Process Window Help

UP_DOWN_WITH_sr_to_jk
- g1
- g2
- g3

Snapshots | Libraries | Design

No flow available.

Processes | Sim Hierarchy - test_UP_DOWN_W...



Design Summary | test_UP_DOWN_WI... | UP_DOWN_with_sr... | Simulation | Synthesis Repor... | UP_DOWN_WITH_sr...

Design Objects of UP_DOWN_WITH_sr_to_jk

Instances	Pins	Signals
g1	clk	clk
g2	i	i

Properties of Signal clk

Name	Value
Name	clk
PortName	clk

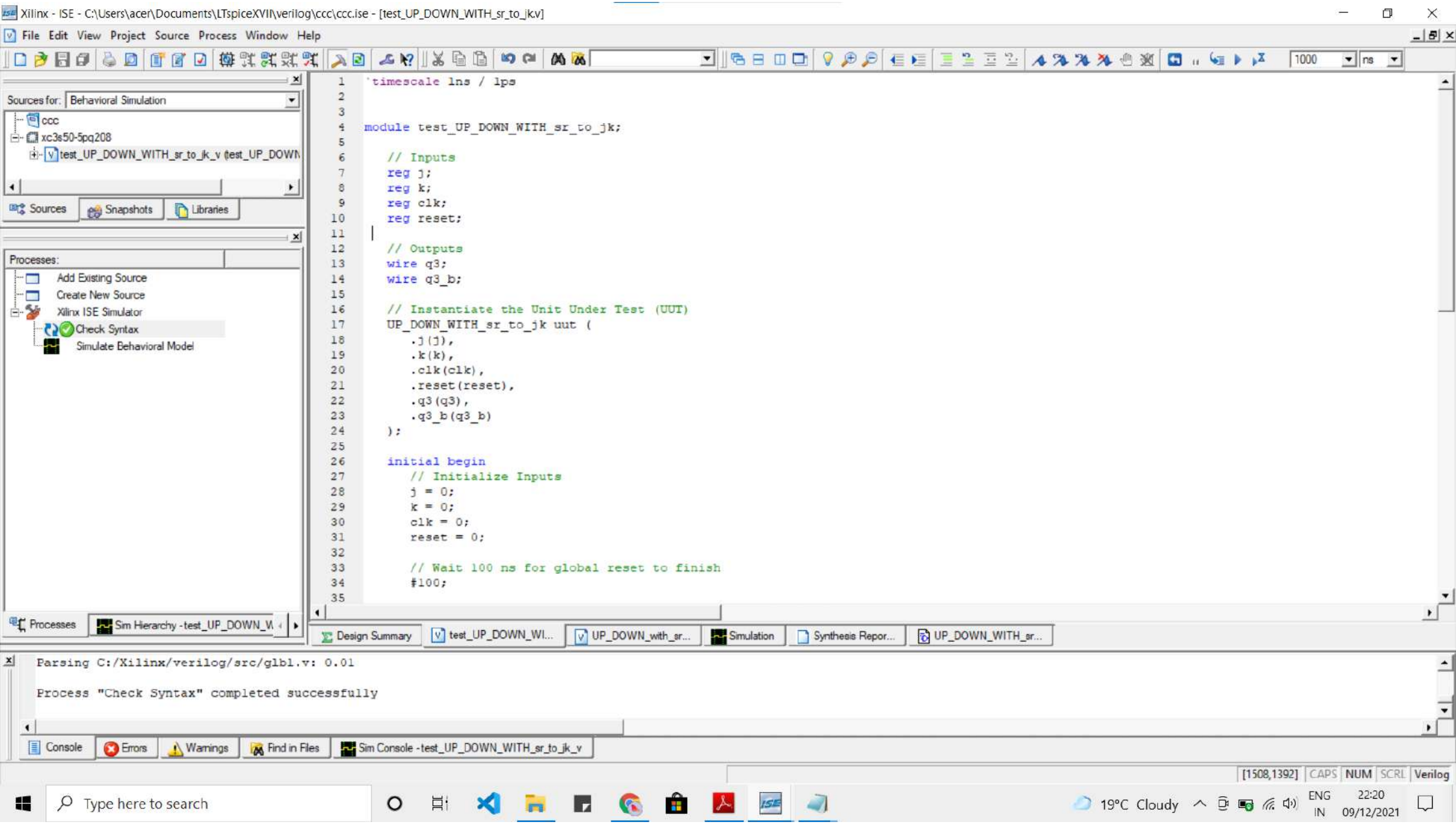
Console | Errors | Warnings | Find in Files | Sim Console - test_UP_DOWN_WITH_sr_to_jk_v | View by Category | View by Name

[1988,1388]

Type here to search

19°C Cloudy ENG IN 22:18 09/12/2021

writing the test bench


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [test_UP_DOWN_WITH_sr_to_jk.v]
File Edit View Project Source Process Window Help
Sources for: Behavioral Simulation
ccc
xc3s50-5pq208
test_UP_DOWN_WITH_sr_to_jk_v (test_UP_DOWN
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Sim Hierarchy - test_UP_DOWN_W
1000
ns
1 `timescale 1ns / 1ps
2
3
4 module test_UP_DOWN_WITH_sr_to_jk;
5
6 // Inputs
7 reg j;
8 reg k;
9 reg clk;
10 reg reset;
11
12 // Outputs
13 wire q3;
14 wire q3_b;
15
16 // Instantiate the Unit Under Test (UUT)
17 UP_DOWN_WITH_sr_to_jk uut (
18 .j(j),
19 .k(k),
20 .clk(clk),
21 .reset(reset),
22 .q3(q3),
23 .q3_b(q3_b)
24);
25
26 initial begin
27 // Initialize Inputs
28 j = 0;
29 k = 0;
30 clk = 0;
31 reset = 0;
32
33 // Wait 100 ns for global reset to finish
34 #100;
35
Design Summary
test_UP_DOWN_WI...
UP_DOWN_with_sr...
Simulation
Synthesis Repor...
UP_DOWN_WITH_sr...
Parsing C:/Xilinx/verilog/src/glbl.v: 0.01
Process "Check Syntax" completed successfully
Console
Errors
Warnings
Find in Files
Sim Console - test_UP_DOWN_WITH_sr_to_jk_v
[1508,1392]
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
22:20
09/12/2021

Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [test_UP_DOWN_WITH_sr_to_jk.v]

File Edit View Project Source Process Window Help

Sources for: Behavioral Simulation

- ccc
- xc3s50-5pq208
- test_UP_DOWN_WITH_sr_to_jk_v (test_UP_DOWN

Sources | Snapshots | Libraries

Processes:

- Add Existing Source
- Create New Source
- Xilinx ISE Simulator
  - Check Syntax
  - Simulate Behavioral Model

Processes | Sim Hierarchy - test_UP_DOWN_W

```
36        // Add stimulus here
37
38    j = 1'b0;
39    k = 1'b0;
40    reset = 1;
41    clk=1;
42
43    #10
44    reset=0;
45    j=1'b1;
46    k=1'b0;
47
48    #100
49    reset=0;
50    j=1'b0;
51    k=1'b1;
52
53    #100
54    reset=0;
55    j=1'b1;
56    k=1'b1;
57
58    #100
59    reset=0;
60    j=1'b0;
61    k=1'b0;
62
63    #100
64    reset=1;
65    j=1'b1;
66    k=1'b0;
67
68    end
69    always #25 clk <= ~clk;
70    endmodule
```

Design Summary | test_UP_DOWN_WI... | UP_DOWN_with_sr... | Simulation | Synthesis Repor... | UP_DOWN_WITH_sr...

```
Parsing C:/Xilinx/verilog/src/glbl.v: 0.01

Process "Check Syntax" completed successfully
```

Console | Errors | Warnings | Find in Files | Sim Console - test_UP_DOWN_WITH_sr_to_jk_v

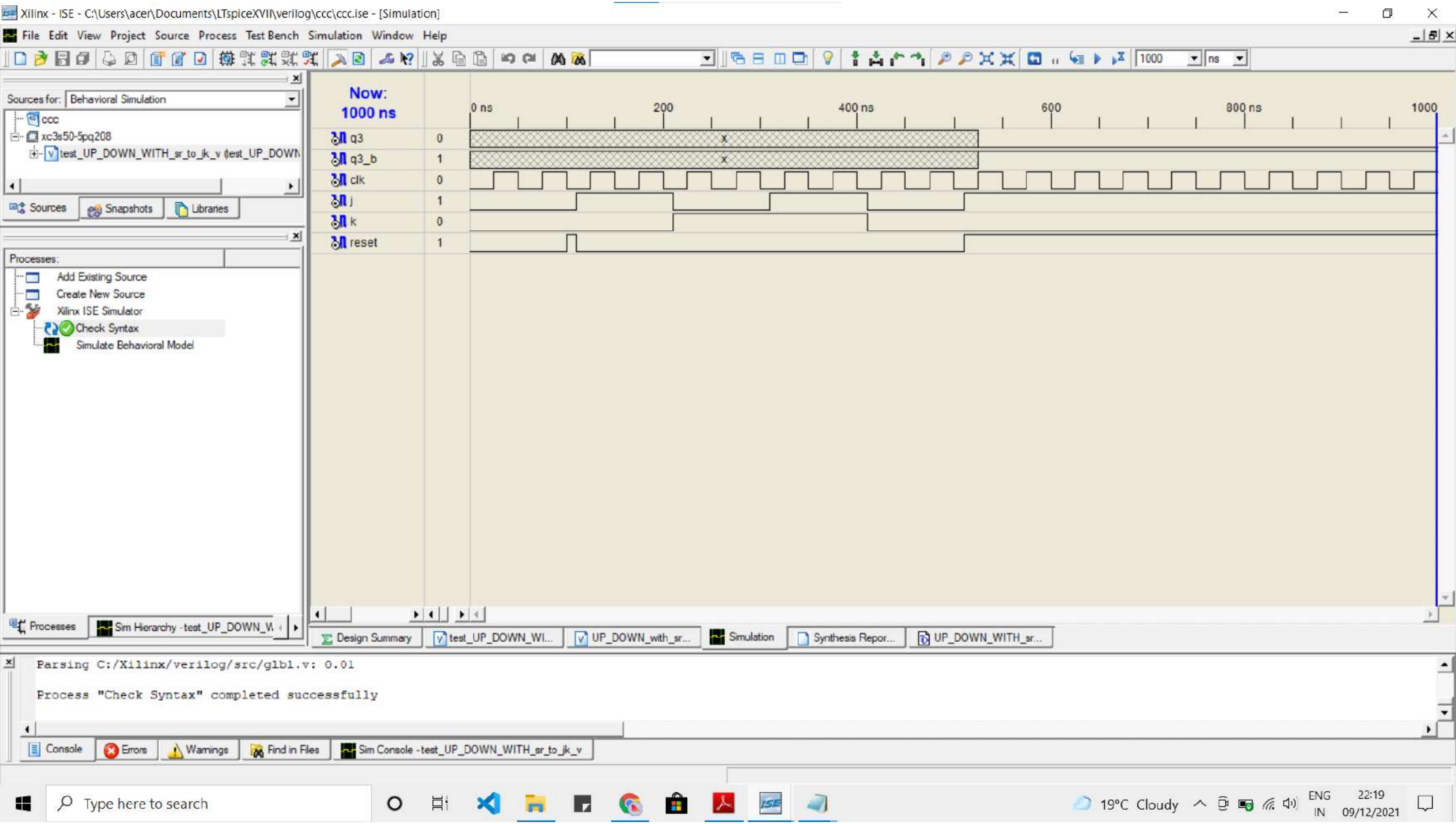
Ln 69 Col 24 | CAPS | NUM | SCRL | Verilog

Type here to search

19°C Cloudy

ENG IN 22:21 09/12/2021

Simulations


Xilinx - ISE - C:\Users\acer\Documents\LTspiceXVII\verilog\ccc\ccc.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
ccc
xc3s50-5pq208
test_UP_DOWN_WITH_sr_to_jk_v (test_UP_DOWN
Sources
Snapshots
Libraries
Processes:
Add Existing Source
Create New Source
Xilinx ISE Simulator
Check Syntax
Simulate Behavioral Model
Processes
Sim Hierarchy - test_UP_DOWN_W
Now:
1000 ns
0 ns
200
400 ns
600
800 ns
1000
q3
q3_b
clk
j
k
reset
Design Summary
test_UP_DOWN_WI...
UP_DOWN_with_sr...
Simulation
Synthesis Repor...
UP_DOWN_WITH_sr...
Parsing C:/Xilinx/verilog/src/glbl.v: 0.01
Process "Check Syntax" completed successfully
Console
Errors
Warnings
Find in Files
Sim Console - test_UP_DOWN_WITH_sr_to_jk_v
Type here to search
19°C Cloudy
ENG
IN
22:19
09/12/2021

Question 5
32-bit Multiplier

Que. 5

⇒ Floating Point Representation —

We have 3 elements in a 32-bit floating point representation —

(a) Sign = It is the first bit of the binary representation.
1 ⇒ negative number
0 ⇒ positive number

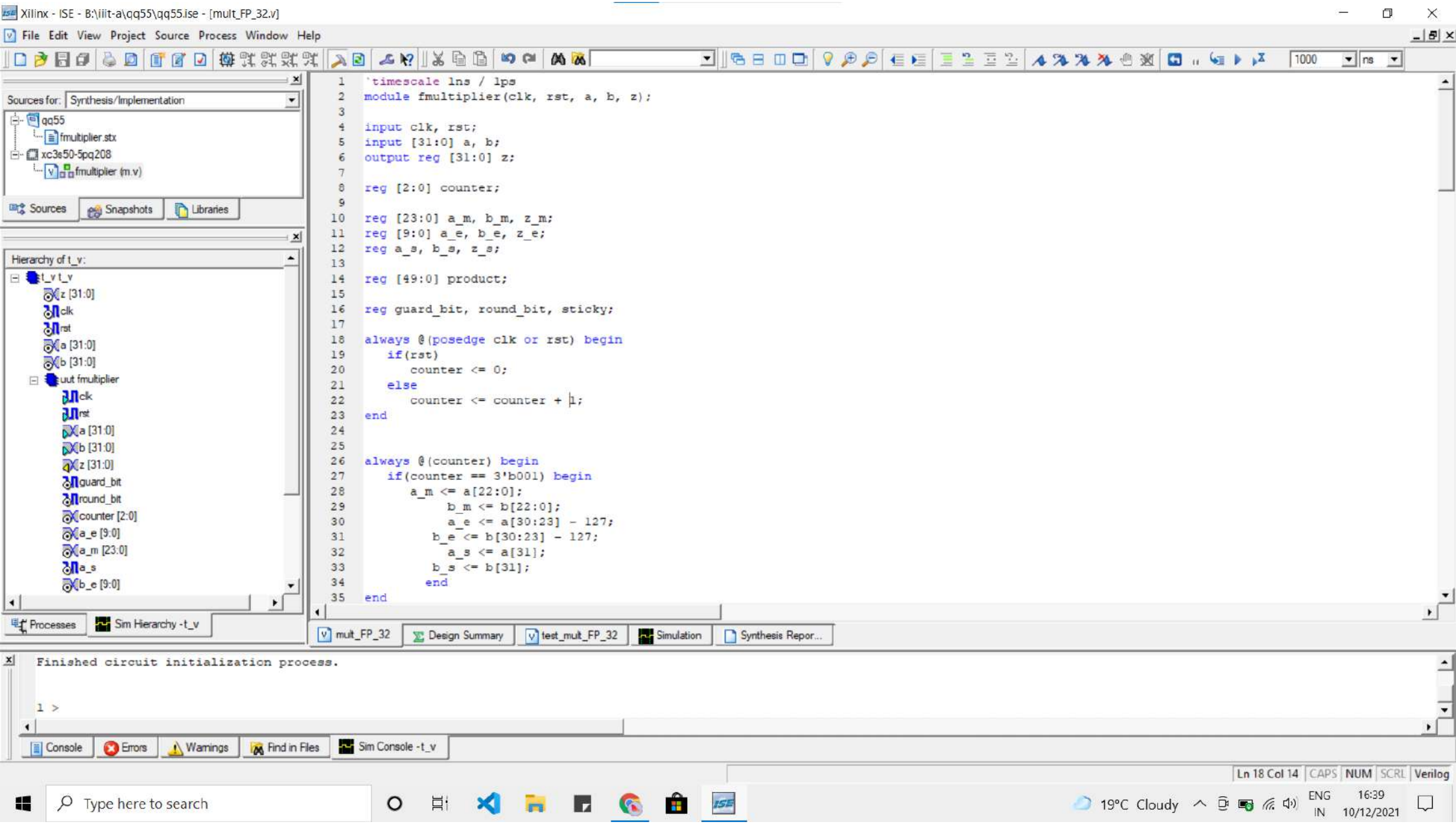
(b) Exponent = It is decided by the next 8 bits of binary representation. 127 is the unique number of 32 bit floating point representation. It is known as bias. It is determined by $2^{k-1} - 1$ where "k" is the number of bits in the exponent field.
There are 3 exponent bits in 8-bit representation and 8 exponent bits in 32-bit representation.

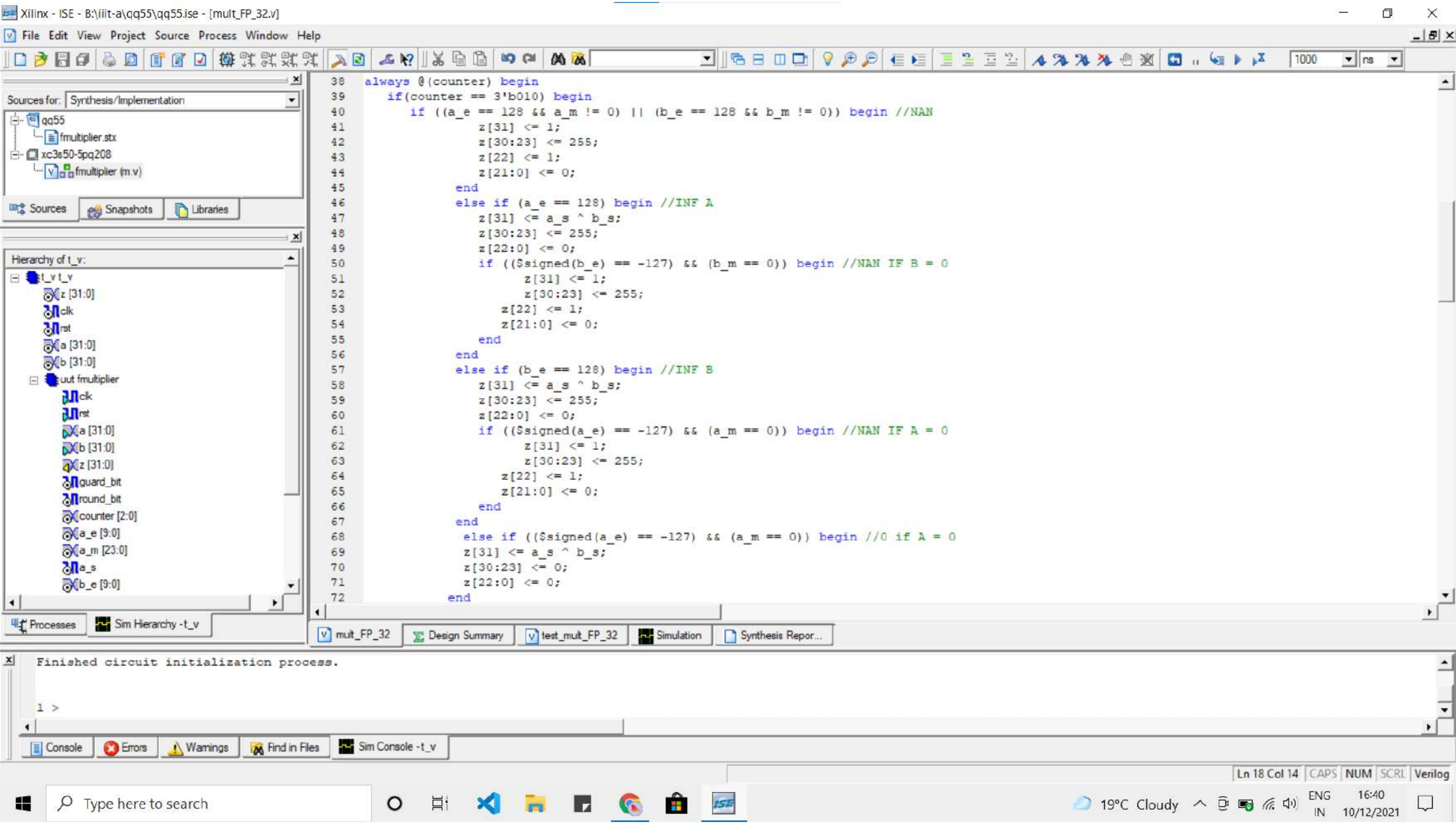
© Mantissa — It is calculated from the remaining 23 bits of the binary representation. It consits of 1 and a fractional part which is determined as so required.

(*)

↳ Here instead of giving 5 simulations we give random number assignments and generated more number of results.

writing the module


Xilinx - ISE - B:\iiit-a\qq55\qq55.ise - [mult_FP_32.v]
File Edit View Project Source Process Window Help
Sources for: Synthesis/Implementation
qq55
fmultiplier.stx
xc3s50-5pq208
fmultiplier (m.v)
Sources
Snapshots
Libraries
Hierarchy of t_v:
t_v t_v
z [31:0]
clk
rst
a [31:0]
b [31:0]
uut fmultiplier
clk
rst
a [31:0]
b [31:0]
z [31:0]
guard_bit
round_bit
counter [2:0]
a_e [9:0]
a_m [23:0]
a_s
b_e [9:0]
Processes
Sim Hierarchy -t_v
1 `timescale 1ns / 1ps
2 module fmultiplier(clk, rst, a, b, z);
3
4 input clk, rst;
5 input [31:0] a, b;
6 output reg [31:0] z;
7
8 reg [2:0] counter;
9
10 reg [23:0] a_m, b_m, z_m;
11 reg [9:0] a_e, b_e, z_e;
12 reg a_s, b_s, z_s;
13
14 reg [49:0] product;
15
16 reg guard_bit, round_bit, sticky;
17
18 always @(posedge clk or rst) begin
19 if(rst)
20 counter <= 0;
21 else
22 counter <= counter + 1;
23 end
24
25
26 always @(counter) begin
27 if(counter == 3'b001) begin
28 a_m <= a[22:0];
29 b_m <= b[22:0];
30 a_e <= a[30:23] - 127;
31 b_e <= b[30:23] - 127;
32 a_s <= a[31];
33 b_s <= b[31];
34 end
35 end
mult_FP_32
Design Summary
test_mult_FP_32
Simulation
Synthesis Repor...
Finished circuit initialization process.
1 >
Console
Errors
Warnings
Find in Files
Sim Console -t_v
Ln 18 Col 14
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
16:39
10/12/2021


Xilinx - ISE - B:\iiit-a\qq55\qq55.ise - [mult_FP_32.v]
File Edit View Project Source Process Window Help
Sources for: Synthesis/Implementation
qq55
fmultiplier.stx
xc3s50-5pq208
fmultiplier (m.v)
Sources
Snapshots
Libraries
Hierarchy of t_v:
t_v t_v
z [31:0]
clk
rst
a [31:0]
b [31:0]
uut fmultiplier
clk
rst
a [31:0]
b [31:0]
z [31:0]
guard_bit
round_bit
counter [2:0]
a_e [9:0]
a_m [23:0]
a_s
b_e [9:0]
Processes
Sim Hierarchy -t_v
38 always @(counter) begin
39 if(counter == 3'b010) begin
40 if ((a_e == 128 && a_m != 0) || (b_e == 128 && b_m != 0)) begin //NAN
41 z[31] <= 1;
42 z[30:23] <= 255;
43 z[22] <= 1;
44 z[21:0] <= 0;
45 end
46 else if (a_e == 128) begin //INF A
47 z[31] <= a_s ^ b_s;
48 z[30:23] <= 255;
49 z[22:0] <= 0;
50 if (($signed(b_e) == -127) && (b_m == 0)) begin //NAN IF B = 0
51 z[31] <= 1;
52 z[30:23] <= 255;
53 z[22] <= 1;
54 z[21:0] <= 0;
55 end
56 end
57 else if (b_e == 128) begin //INF B
58 z[31] <= a_s ^ b_s;
59 z[30:23] <= 255;
60 z[22:0] <= 0;
61 if (($signed(a_e) == -127) && (a_m == 0)) begin //NAN IF A = 0
62 z[31] <= 1;
63 z[30:23] <= 255;
64 z[22] <= 1;
65 z[21:0] <= 0;
66 end
67 end
68 else if (($signed(a_e) == -127) && (a_m == 0)) begin //0 if A = 0
69 z[31] <= a_s ^ b_s;
70 z[30:23] <= 0;
71 z[22:0] <= 0;
72 end
mult_FP_32
Design Summary
test_mult_FP_32
Simulation
Synthesis Repor...
Finished circuit initialization process.
1 >
Console
Errors
Warnings
Find in Files
Sim Console -t_v
Ln 18 Col 14
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
16:40
10/12/2021

Xilinx - ISE - B:\iiit-a\qq55\qq55.ise - [mult_FP_32.v]

File Edit View Project Source Process Window Help

Sources for: Synthesis/Implementation

- qq55
  - fmultiplier.stx
- xc3s50-5pq208
  - fmultiplier (m.v)

Sources | Snapshots | Libraries

Hierarchy of t_v:

- t_v t_v
  - z [31:0]
  - clk
  - rst
  - a [31:0]
  - b [31:0]
  - uut fmultiplier
    - clk
    - rst
    - a [31:0]
    - b [31:0]
    - z [31:0]
    - guard_bit
    - round_bit
    - counter [2:0]
    - a_e [9:0]
    - a_m [23:0]
    - a_s
    - b_e [9:0]

Processes | Sim Hierarchy -t_v

```
73            else if (($signed(b_e) == -127) && (b_m == 0)) begin //0 if B = 0
74              z[31] <= a_s ^ b_s;
75              z[30:23] <= 0;
76              z[22:0] <= 0;
77            end
78            else begin
79             if ($signed(a_e) == -127)
80                   a_e <= -126;
81             else
82                   a_m[23] <= 1;
83
84                if ($signed(b_e) == -127)
85                   b_e <= -126;
86             else
87                   b_m[23] <= 1;
88            end
89          end
90  end
91
92
93  always @(counter) begin
94     if(counter == 3'b011) begin
95        if (~a_m[23]) begin
96              a_m <= a_m << 1;
97              a_e <= a_e - 1;
98            end
99            if (~b_m[23]) begin
100             b_m <= b_m << 1;
101             b_e <= b_e - 1;
102           end
103    end
104 end
105
106
107 always @(counter) begin
```

mult_FP_32 | Design Summary | test_mult_FP_32 | Simulation | Synthesis Repor...

```
Finished circuit initialization process.


1 >
```

Console | Errors | Warnings | Find in Files | Sim Console -t_v

Ln 18 Col 14 | CAPS | NUM | SCRL | Verilog

Type here to search

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ENG IN 16:40 10/12/2021

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    - rst
    - a [31:0]
    - b [31:0]
    - z [31:0]
    - guard_bit
    - round_bit
    - counter [2:0]
    - a_e [9:0]
    - a_m [23:0]
    - a_s
    - b_e [9:0]

Processes | Sim Hierarchy -t_v

```
108     if(counter == 3'b100) begin
109        z_s <= a_s ^ b_s;
110           z_e <= a_e + b_e + 1;
111         product <= a_m * b_m * 4;
112     end
113  end
114
115
116  always @(counter) begin
117     if(counter == 3'b101) begin
118        z_m <= product[49:26];
119           guard_bit <= product[25];
120              round_bit <= product[24];
121              sticky <= (product[23:0] != 0);
122     end
123  end
124
125  always @(counter) begin
126     if(counter == 3'b110) begin
127        if ($signed(z_e) < -126) begin
128              z_e <= z_e + (-126 -$signed(z_e));
129              z_m <= z_m >> (-126 -$signed(z_e));
130              guard_bit <= z_m[0];
131              round_bit <= guard_bit;
132              sticky <= sticky | round_bit;
133           end
134        else if (z_m[23] == 0) begin
135              z_e <= z_e - 1;
136              z_m <= z_m << 1;
137              z_m[0] <= guard_bit;
138              guard_bit <= round_bit;
139              round_bit <= 0;
140           end
141             else if (guard_bit && (round_bit | sticky | z_m[0])) begin
142              z_m <= z_m + 1;
```

mult_FP_32 | Design Summary | test_mult_FP_32 | Simulation | Synthesis Repor...

```
Finished circuit initialization process.


1 >
```

Console | Errors | Warnings | Find in Files | Sim Console -t_v

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    - clk
    - rst
    - a [31:0]
    - b [31:0]
    - z [31:0]
    - guard_bit
    - round_bit
    - counter [2:0]
    - a_e [9:0]
    - a_m [23:0]
    - a_s
    - b_e [9:0]

Processes | Sim Hierarchy -t_v

```
133             end
134         else if (z_m[23] == 0) begin
135               z_e <= z_e - 1;
136               z_m <= z_m << 1;
137               z_m[0] <= guard_bit;
138               guard_bit <= round_bit;
139               round_bit <= 0;
140             end
141               else if (guard_bit && (round_bit | sticky | z_m[0])) begin
142               z_m <= z_m + 1;
143                  if (z_m == 24'hffffff)
144                        z_e <=z_e + 1;
145             end
146            end
147   end
148
149   always @(counter) begin
150      if(counter == 3'b111) begin
151         z[22:0] <= z_m[22:0];
152            z[30:23] <= z_e[7:0] + 127;
153            z[31] <= z_s;
154            if ($signed(z_e) == -126 && z_m[23] == 0)
155                  z[30:23] <= 0;
156            if ($signed(z_e) > 127) begin
157                  z[22:0] <= 0;
158                  z[30:23] <= 255;
159                  z[31] <= z_s;
160            end
161      end
162   end
163
164
165   endmodule
166
```

mult_FP_32 | Design Summary | test_mult_FP_32 | Simulation | Synthesis Repor...

```
Finished circuit initialization process.


1 >
```

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Ln 18 Col 14 | CAPS | NUM | SCRL | Verilog

Type here to search

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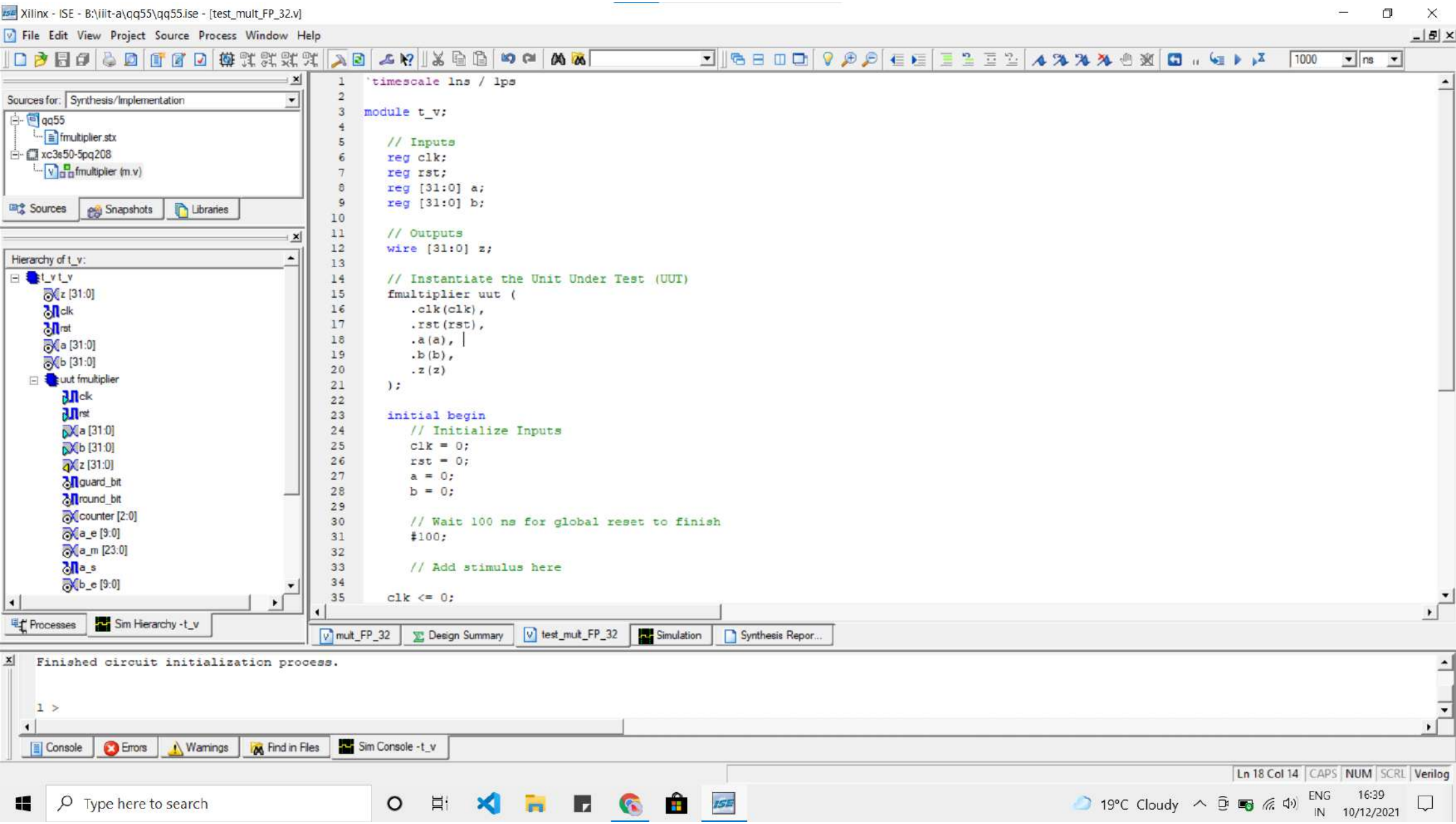
writing the test bench


Xilinx - ISE - B:\iiit-a\qq55\qq55.ise - [test_mult_FP_32.v]
File Edit View Project Source Process Window Help
Sources for: Synthesis/Implementation
qq55
fmultiplier.stx
xc3s50-5pq208
fmultiplier (m.v)
Sources
Snapshots
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Hierarchy of t_v:
t_v t_v
z [31:0]
clk
rst
a [31:0]
b [31:0]
uut fmultiplier
clk
rst
a [31:0]
b [31:0]
z [31:0]
guard_bit
round_bit
counter [2:0]
a_e [9:0]
a_m [23:0]
a_s
b_e [9:0]
Processes
Sim Hierarchy -t_v
1 `timescale 1ns / 1ps
2
3 module t_v;
4
5 // Inputs
6 reg clk;
7 reg rst;
8 reg [31:0] a;
9 reg [31:0] b;
10
11 // Outputs
12 wire [31:0] z;
13
14 // Instantiate the Unit Under Test (UUT)
15 fmultiplier uut (
16 .clk(clk),
17 .rst(rst),
18 .a(a),
19 .b(b),
20 .z(z)
21);
22
23 initial begin
24 // Initialize Inputs
25 clk = 0;
26 rst = 0;
27 a = 0;
28 b = 0;
29
30 // Wait 100 ns for global reset to finish
31 #100;
32
33 // Add stimulus here
34
35 clk <= 0;
mult_FP_32
Design Summary
test_mult_FP_32
Simulation
Synthesis Repor...
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Console
Errors
Warnings
Find in Files
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SCRL
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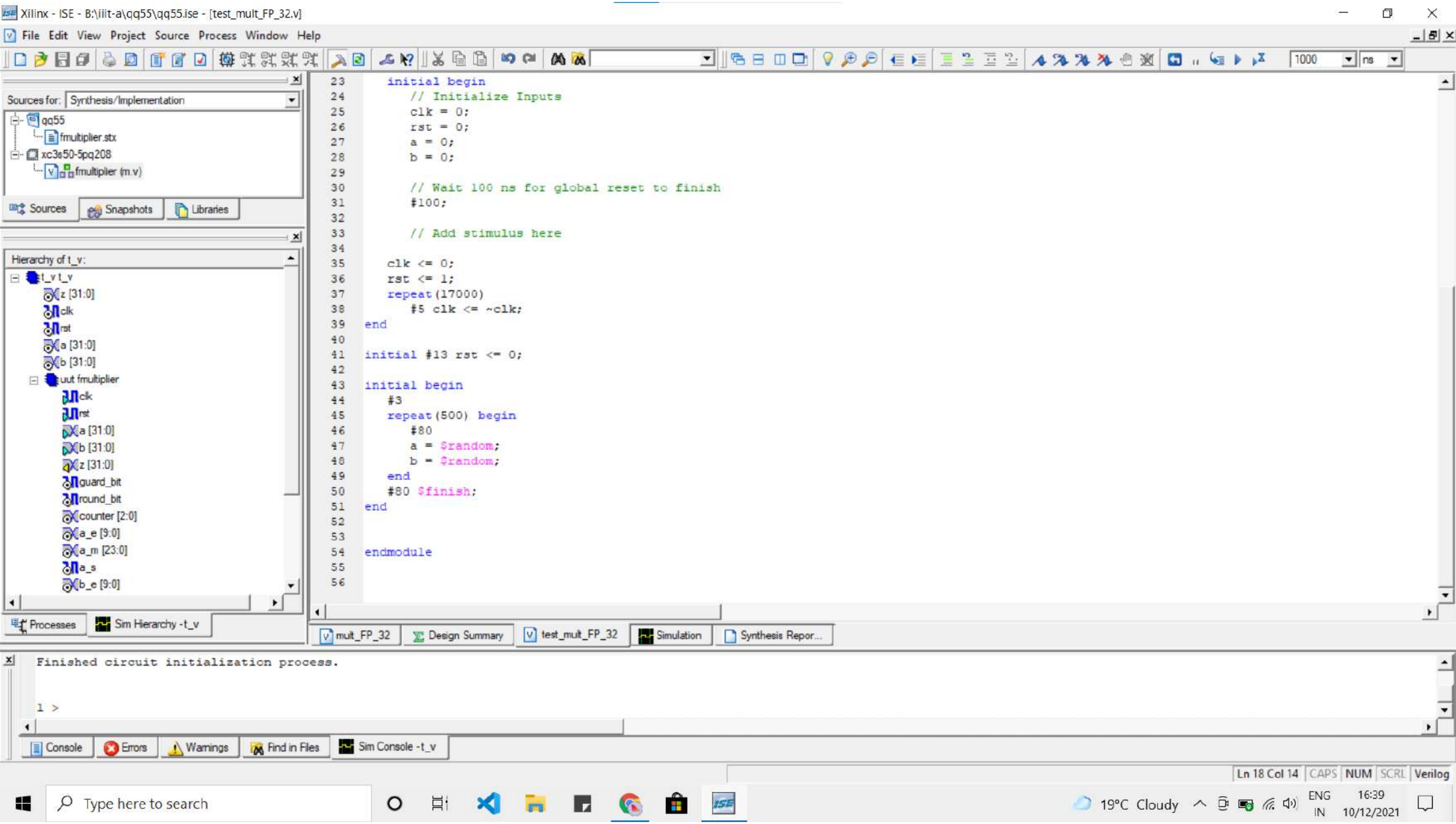
ENG
IN
16:39
10/12/2021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File Edit View Project Source Process Window Help
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rst
a [31:0]
b [31:0]
uut fmultiplier
clk
rst
a [31:0]
b [31:0]
z [31:0]
guard_bit
round_bit
counter [2:0]
a_e [9:0]
a_m [23:0]
a_s
b_e [9:0]
Processes
Sim Hierarchy -t_v
23 initial begin
24 // Initialize Inputs
25 clk = 0;
26 rst = 0;
27 a = 0;
28 b = 0;
29
30 // Wait 100 ns for global reset to finish
31 #100;
32
33 // Add stimulus here
34
35 clk <= 0;
36 rst <= 1;
37 repeat(17000)
38 #5 clk <= ~clk;
39 end
40
41 initial #13 rst <= 0;
42
43 initial begin
44 #3
45 repeat(500) begin
46 #80
47 a = $random;
48 b = $random;
49 end
50 #80 $finish;
51 end
52
53
54 endmodule
55
56
mult_FP_32
Design Summary
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Simulation
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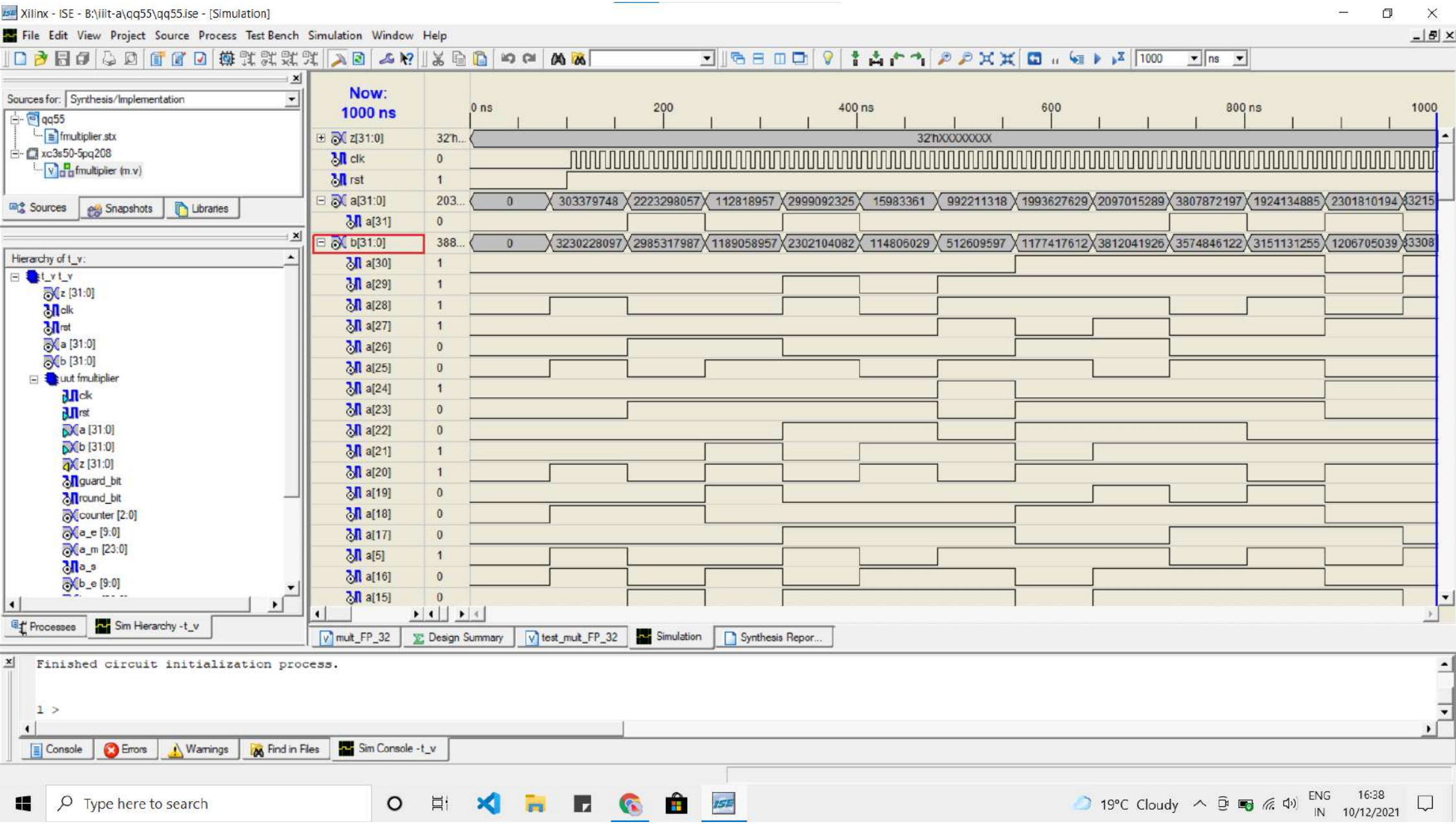
Console
Errors
Warnings
Find in Files
Sim Console -t_v
Ln 18 Col 14
CAPS
NUM
SCRL
Verilog
Type here to search
19°C Cloudy
ENG
IN
16:39
10/12/2021

Simulations


Xilinx - ISE - B:\iiit-a\qq55\qq55.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
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qq55
fmultiplier.stx
xc3s50-5pq208
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Snapshots
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rst
a [31:0]
b [31:0]
uut fmultiplier
clk
rst
a [31:0]
b [31:0]
z [31:0]
guard_bit
round_bit
counter [2:0]
a_e [9:0]
a_m [23:0]
a_s
b_e [9:0]
Processes
Sim Hierarchy -t_v
Now:
1000 ns
0 ns
200
400 ns
600
800 ns
1000
z[31:0]
32'h...
32'hXXXXXXXX
clk
0
rst
1
a[31:0]
203...
0
303379748
2223298057
112818957
2999092325
15983361
992211318
1993627629
2097015289
3807872197
1924134885
2301810194
3215
a[31]
0
b[31:0]
388...
0
3230228097
2985317987
1189058957
2302104082
114806029
512609597
1177417612
3812041926
3574846122
3151131255
1206705039
3308
a[30]
1
a[29]
1
a[28]
1
a[27]
1
a[26]
0
a[25]
0
a[24]
1
a[23]
0
a[22]
0
a[21]
1
a[20]
1
a[19]
0
a[18]
0
a[17]
0
a[5]
1
a[16]
0
a[15]
0
mult_FP_32
Design Summary
test_mult_FP_32
Simulation
Synthesis Repor...
Finished circuit initialization process.
1 >
Console
Errors
Warnings
Find in Files
Sim Console -t_v
Type here to search
19°C Cloudy
ENG
IN
16:38
10/12/2021

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