INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, ALLAHABAD

Online Assignment

Subject: Programming for Engg. Applications

Assignment Topic: Verilog HDL

Course Coordinator: Dr. Sunny Sharma

(M.Tech. ECE, 1st Sem)

Total Marks: 20 Last date of Submission: 10-12-2021

Marks may be rescaled later

Submission Guidelines:

i. You are advised to submit the code of design and test bench in .v format along with result waveforms screenshot wherever required

ii. Needed paperwork for solving the set of problems, should be submitted separately with a scanned document .pdf format file.

iii. Stuff related to the Question should be enclosed by the folder of the name "Q#.#"

iv. Set of Folders "Q#.#" should be enclosed by the folder of the name of your enrollment.

v. All .v files should have either a high level module of the hierarchy of the design or name of the test bench module of the design.

vi. All pages of the pdf file should be numbered from 1 to N.

Problems:

1. Write the verilog module of a D flip-flop (module name should be dff_syn) with synchronous set, reset and enable pin? Simulate (testbench name should be test_dff_syn) the design to verify the truth table of the proposed design. (3)
2. Write the verilog module of a S-R flip-flop (module name should be SR_FLIP) and verify the truth table of the design through simulation (testbench name should be test_SR_FLIP). (3)
3. Use previously designed S-R flip flop (in Que. 2) and write the verilog module (module name should be SR_to_JK) to convert the flip-flop to J-K flip flop? Simulate (test bench name should be test_SR_to_JK) the converted J-K flip-flop to verify the truth table of J-K flip-flop. (3)
4. Use the above converted J-K flip-flop (in Que. 3) to design the verilog module of a mod-10 up and down counter (module name should be UP_DOWN_WITH_SR_to_JK) and verify the Design through simulation (test bench name should be (test_UP_DOWN_WITH_SR_to_JK). (3)
5. What do you mean by floating point representation in a number system? Elaborate, the digital design could be used for the multiplication of two floating point numbers represented in 32 bit IEEE Standard 754 floating point format ? Write a verilog module of the name mult_FP32 that multiplies the two 32-bit floating point numbers, ranging from -1 to 1. Simulate at least 05 distinct multiplication problems with the designed multiplier with a testbench named "test_mult_FP32" ? (8)