

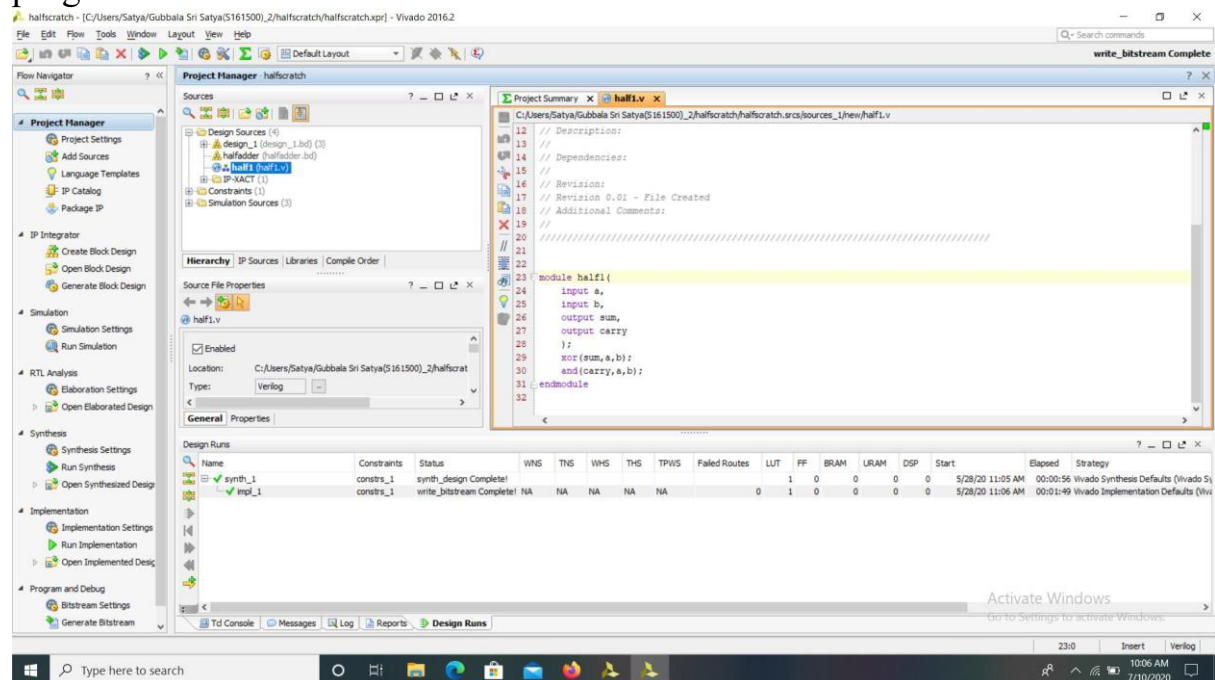
IP Creation for 8-Bit Adder

Main steps:

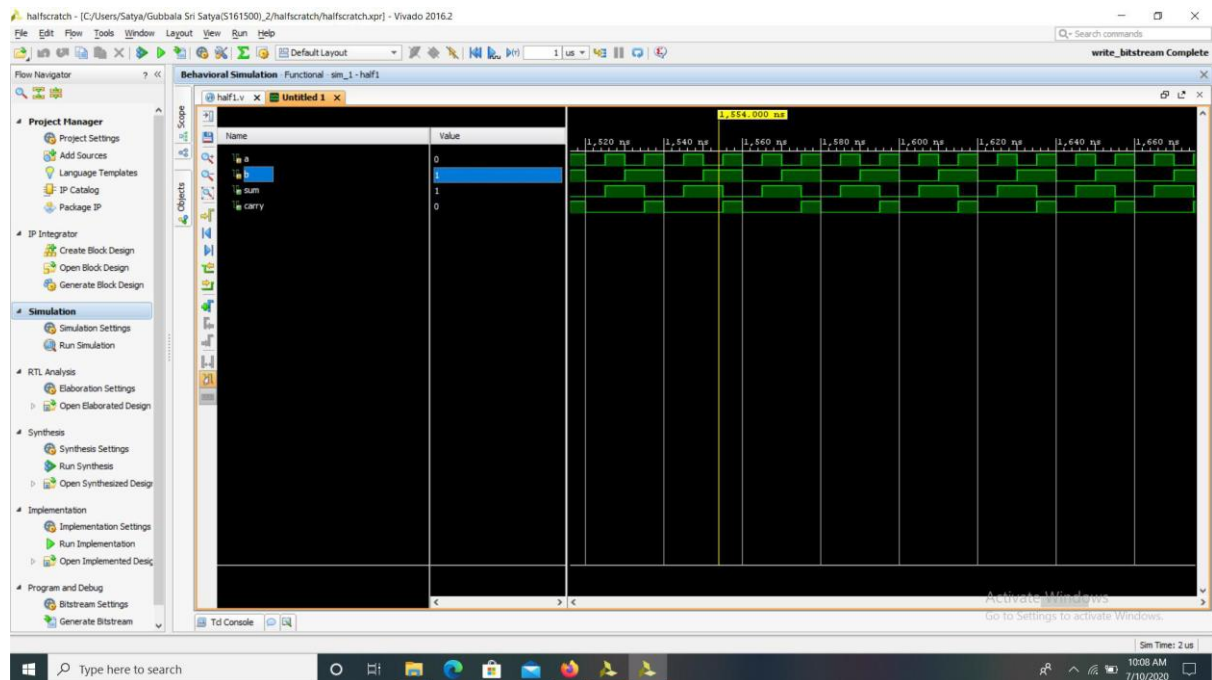
- Write program for full adder
- Run Synthesis
- Run Implementation
- Generate Bit Stream
- Create IP
- Cascade 8 IPs to create 8 bit adder.

Detailed Steps:

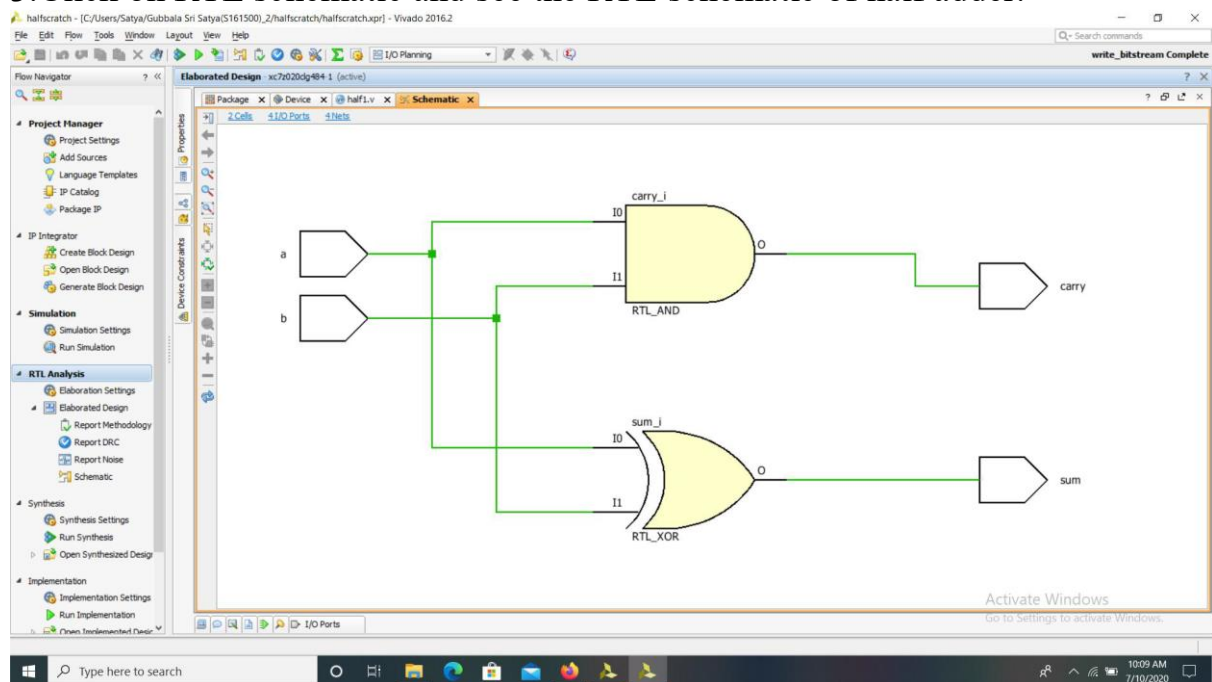
1.Create new project as told in the previous project. Add sources and write the program for half adder in that source file.



2.Click on Run Simulation. Give values by clicking on force clock. And see the output.



3. Click on RTL schematic and see the RTL schematic of half adder.



4. Click on scalar ports and assign the package pins. And then click on Run synthesis. After completion of Synthesis Click on Run Implementation. And then Generate Bit Stream.

halfscratch - [C:/Users/Satya/Gubbala Sri Satya(S161500)_2/halfscratch/halfscratch.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
 - Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design

Elaborated Design - xc7020dgp4k-1 (active)

I/O Ports

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type
All ports (1)													
Scalar ports (4)													
a	IN				G19	✓	35	LVCMOS25*	2.500			NONE	
b	IN				F19	✓	35	LVCMOS25*	2.500			NONE	
carry	OUT				E15	✓	35	LVCMOS25*	2.500	12	SLOW	NONE	
sum	OUT				W17	✓	33	LVCMOS25*	2.500	12	SLOW	NONE	

Activate Windows
Go to Settings to activate Windows.

halfscratch - [C:/Users/Satya/Gubbala Sri Satya(S161500)_2/halfscratch/halfscratch.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Flow Navigator

- IP Catalog
- Package IP
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Elaborated Design - xc7020dgp4k-1 (active)

Device Constraints

Internal VREF

- 0.6V
- 0.675V
- 0.75V
- 0.9V
- NONE (4)
 - I/O Bank 13
 - I/O Bank 33
 - I/O Bank 34
 - I/O Bank 35

Sources: RTL Netlist, Device Constraints

Properties

Select an object to see properties

Properties: Clock Regions

Package: xc7020dgp4k-1

Device: xc7020dgp4k-1

half1.v

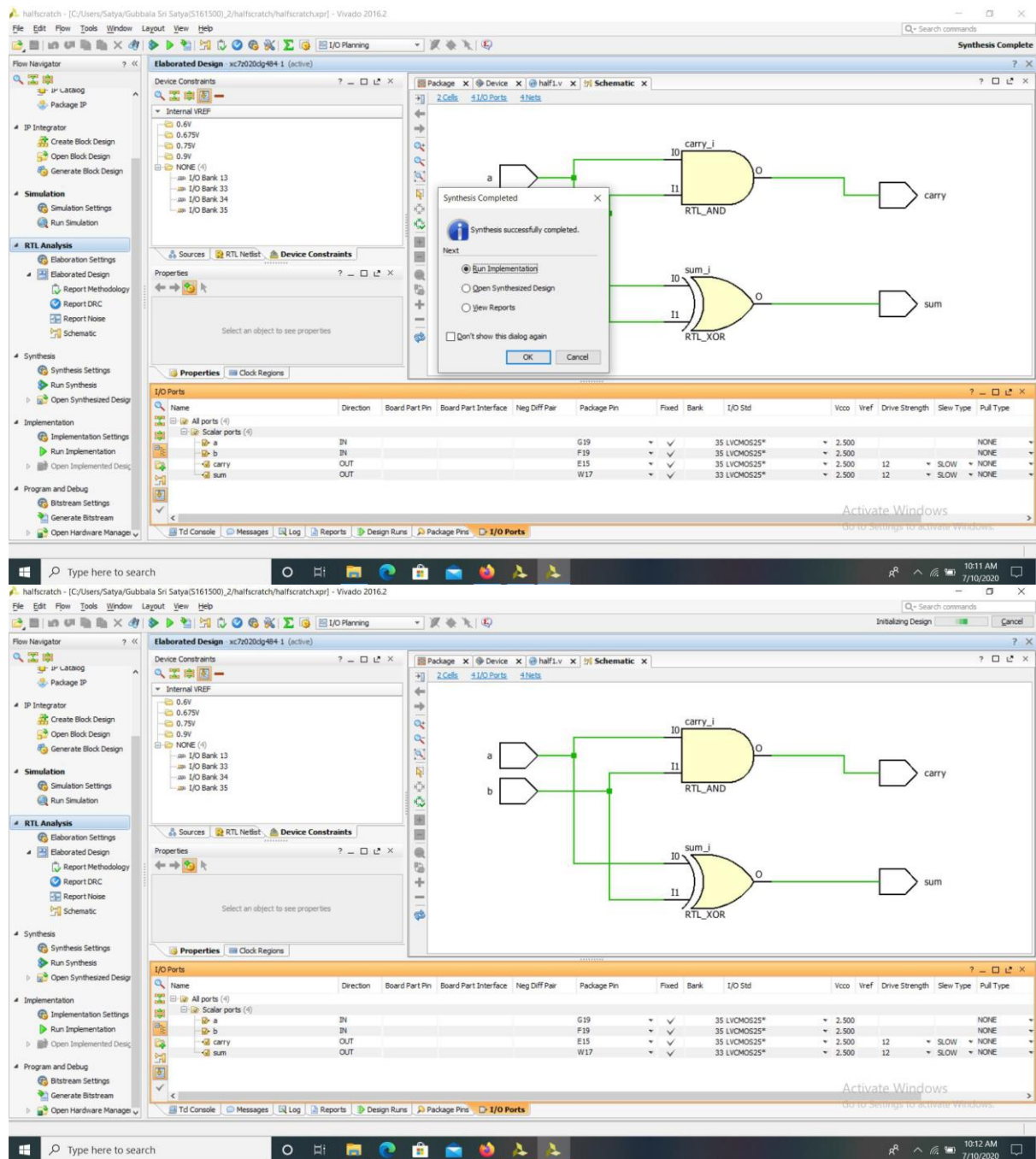
Schematic

2 Cells, 4 I/O Ports, 4 Nets

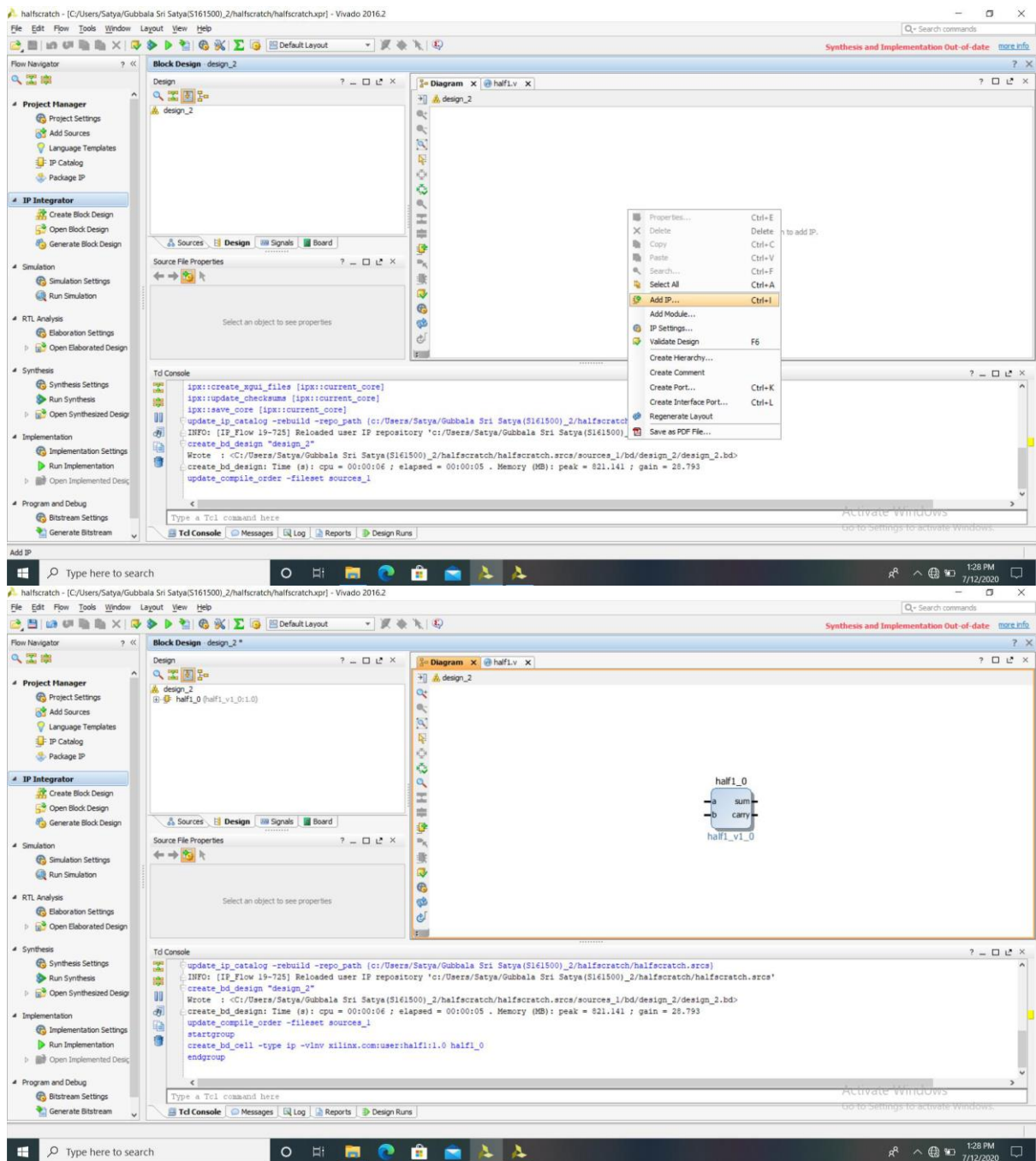
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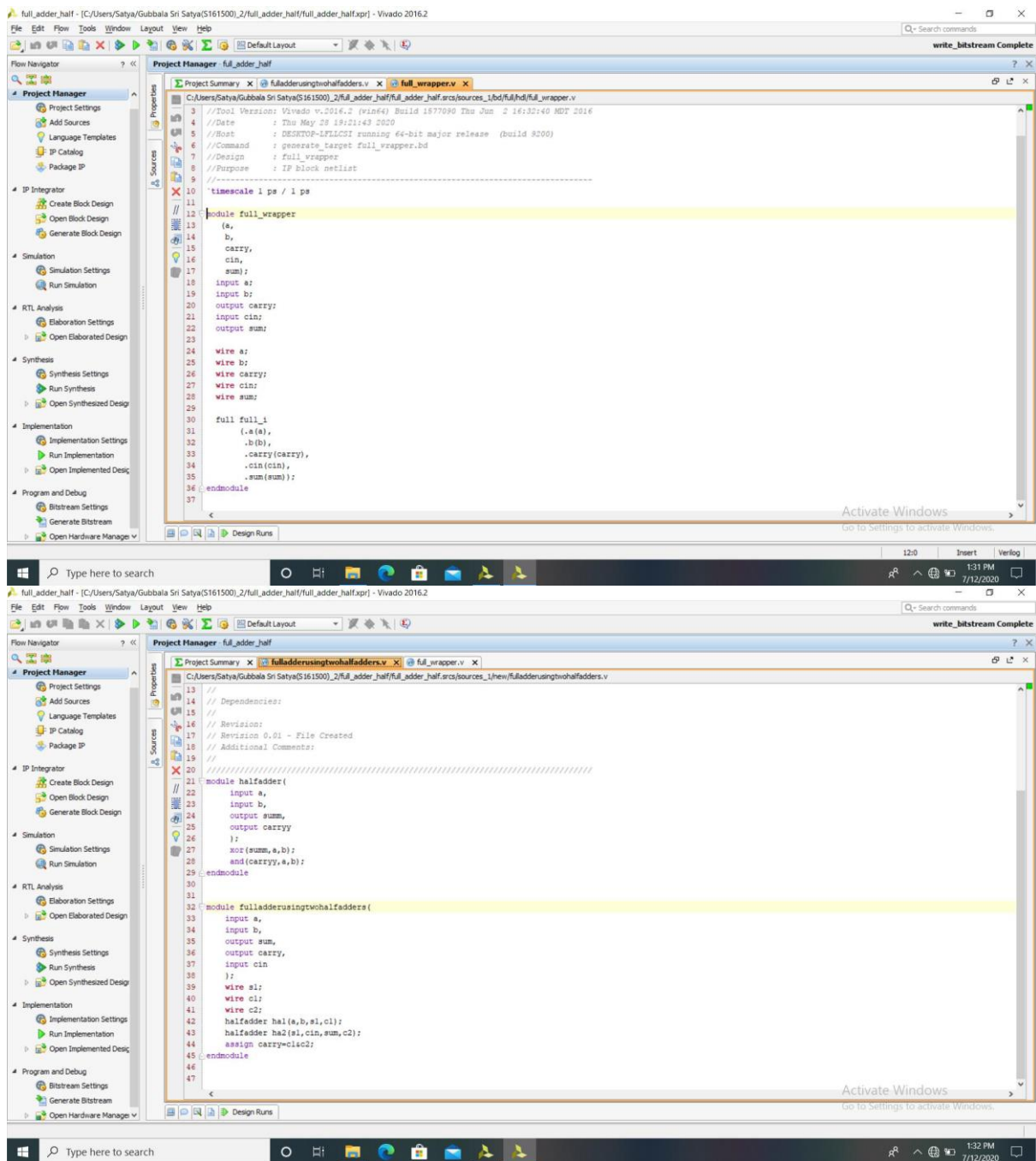
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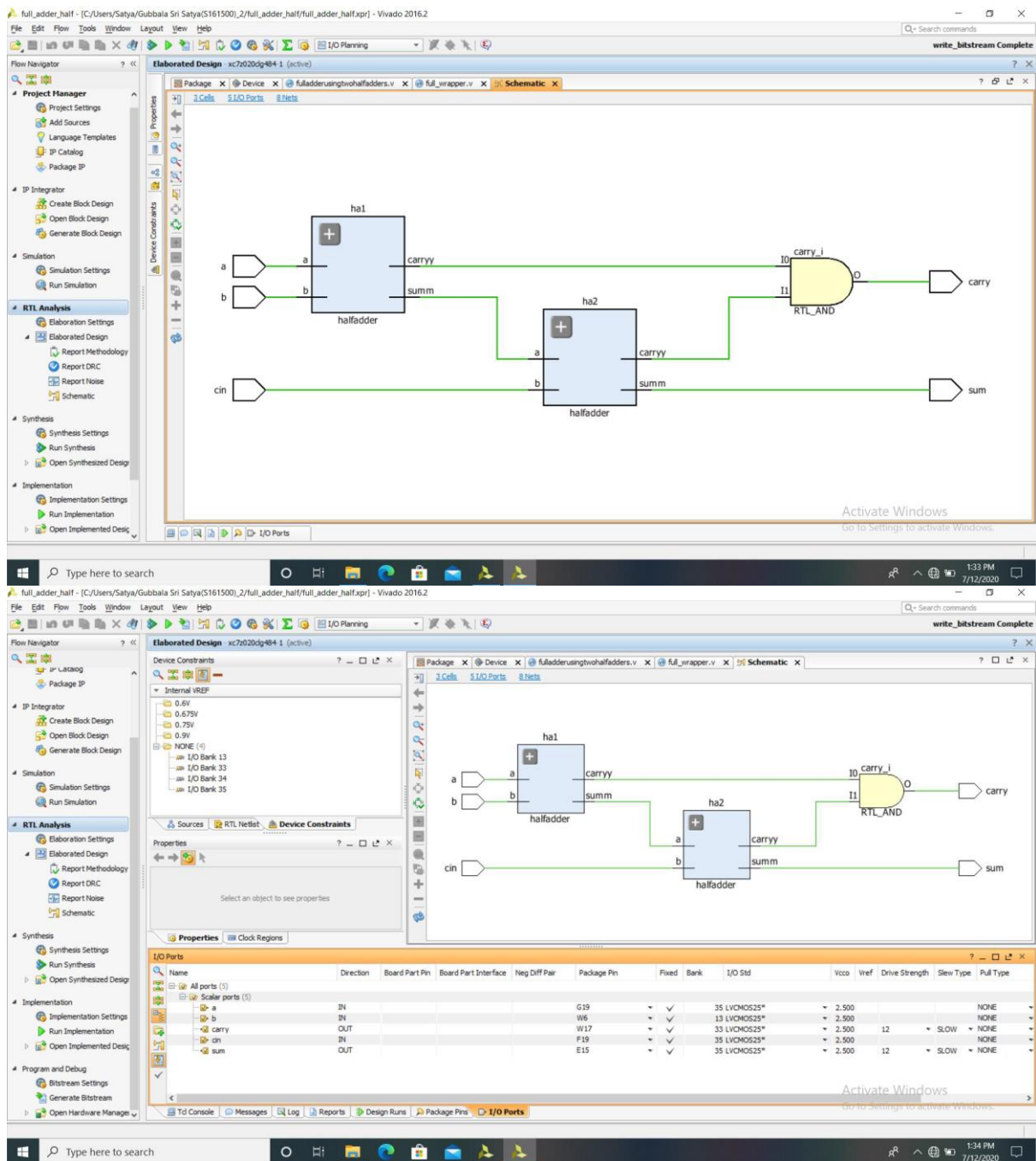
5. After completion of Bit Stream generation, Go to Tools click on Create and Package IP and select Package your current project. Create an IP for half adder. Thus the IP is created.



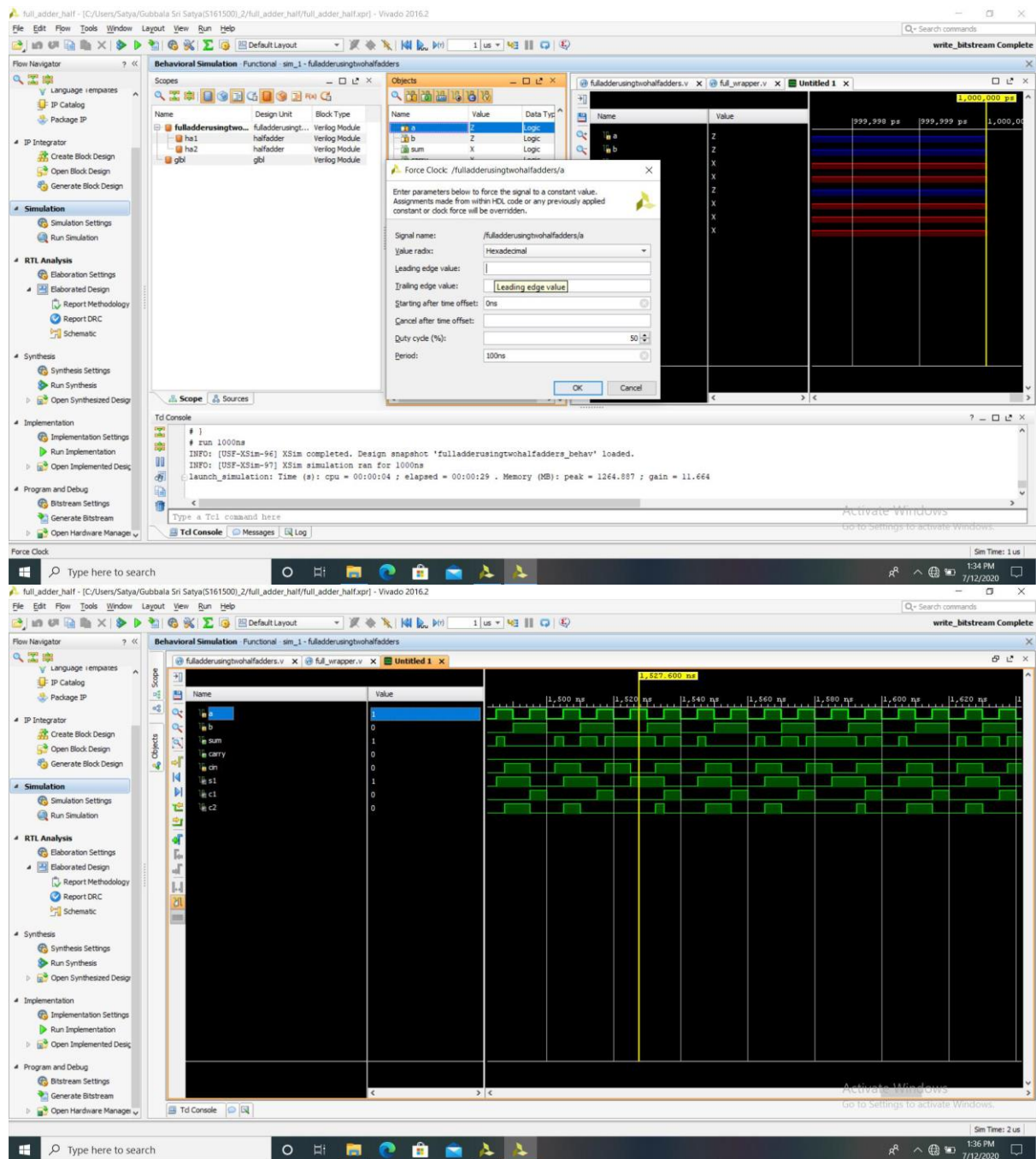
6. Now you have to write code for full adder. You can instantiate half adder two times for doing full adder. Below two pictures are the codes for main program and test bench.



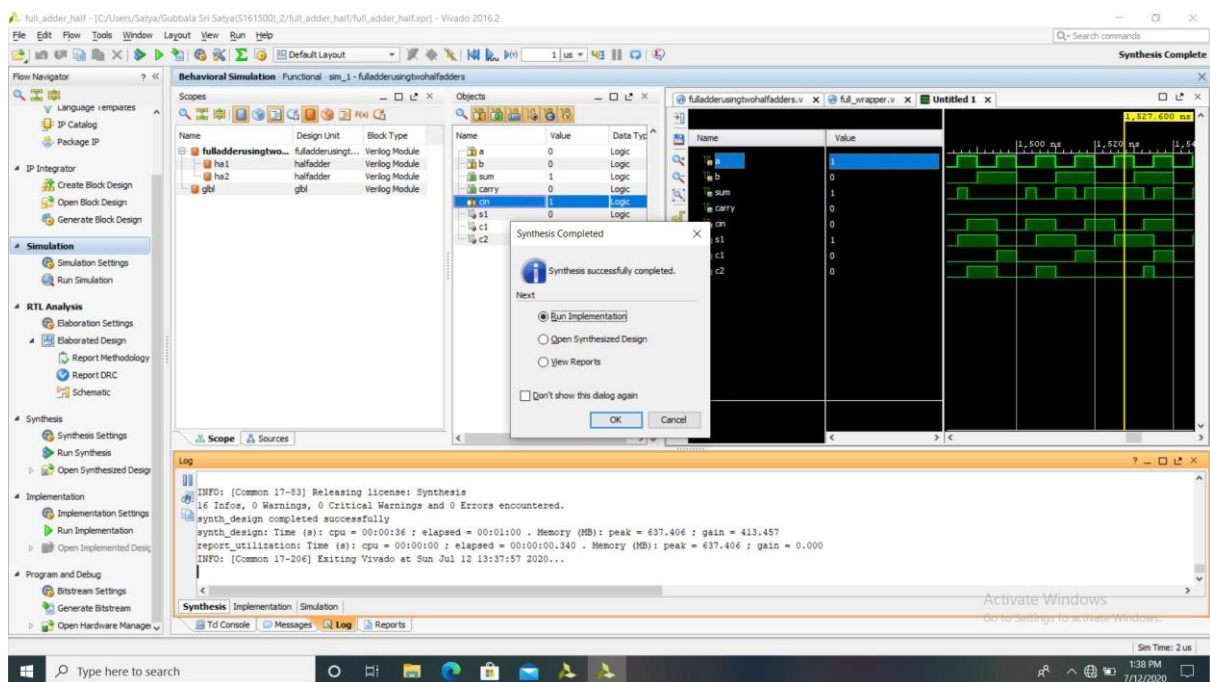
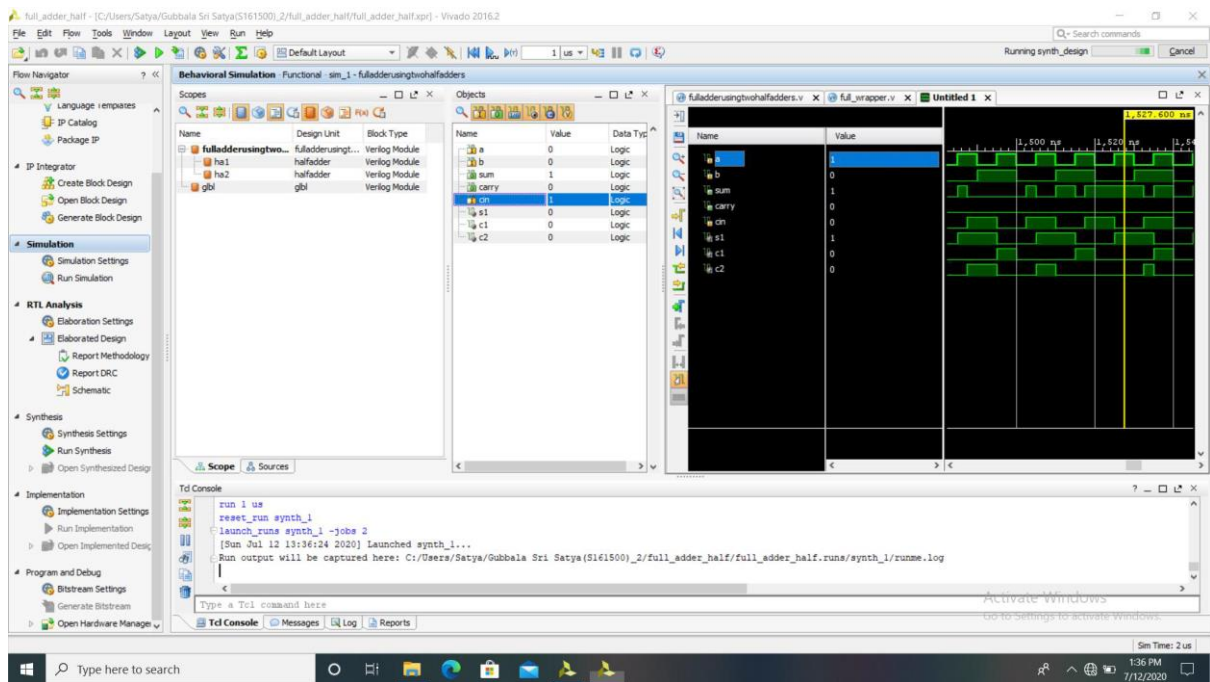
7. Then save the file and click on RTL Schematic. Assign the Package pins in the Scalar ports menu.



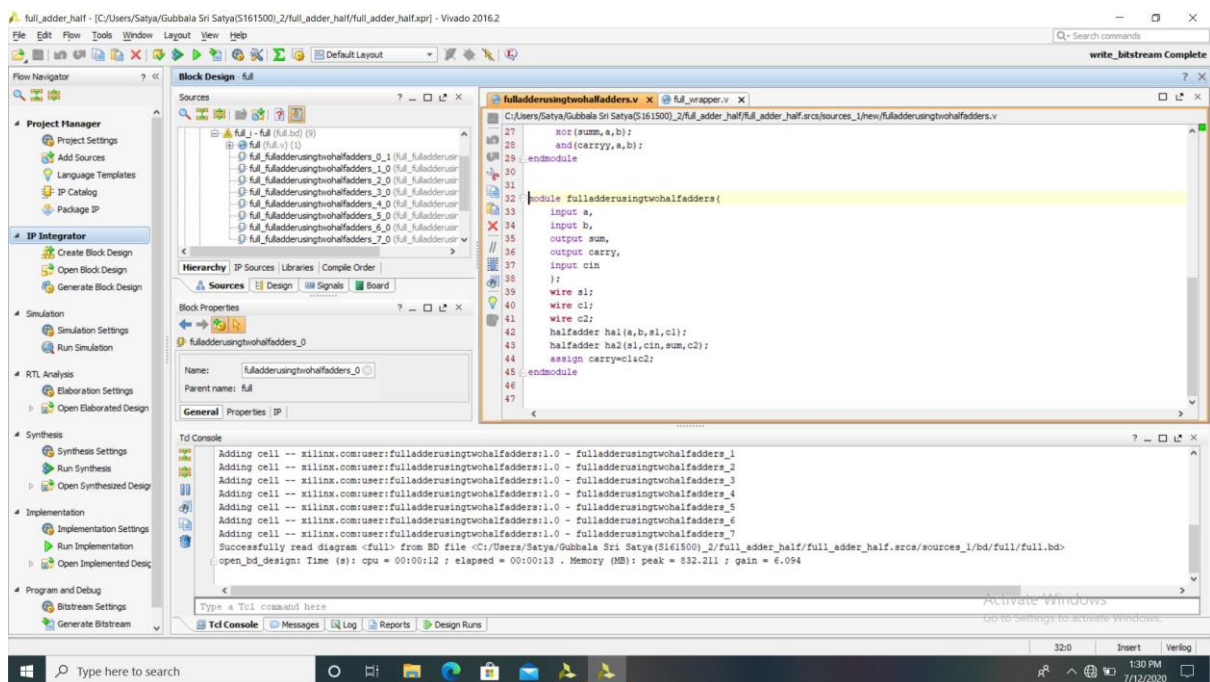
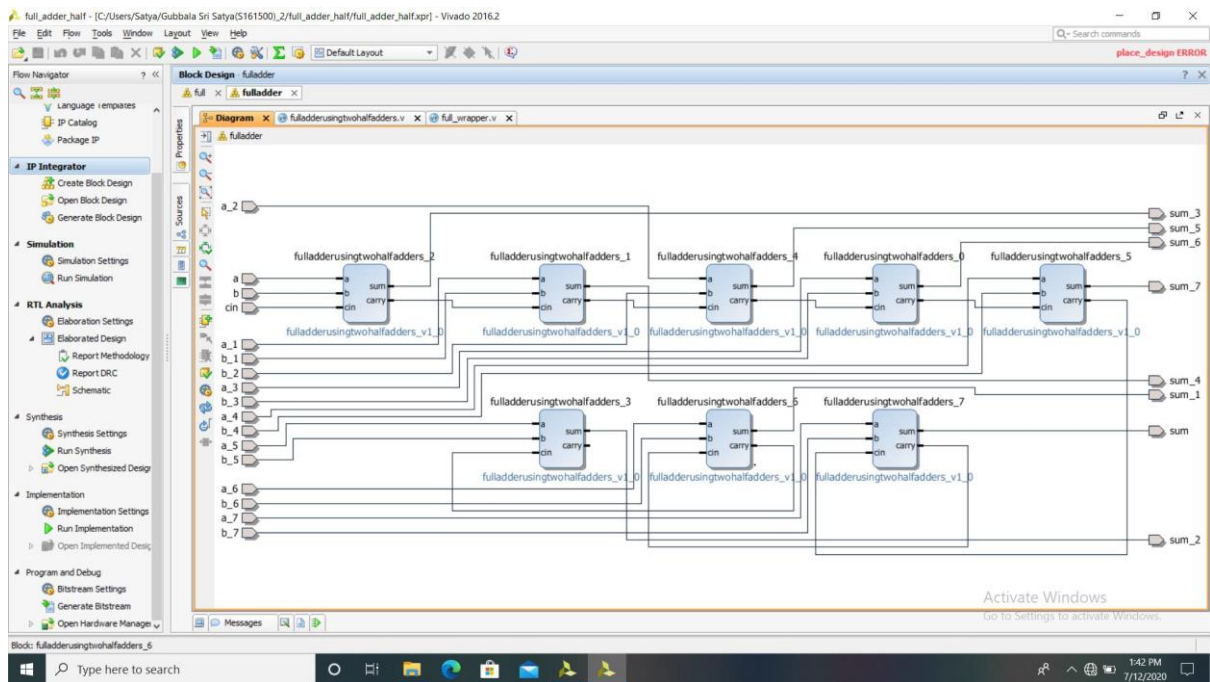
8. Click on Run simulation. Enter the leading edge and trailing edge values when you click on force clock option. Click on Run for 1 micro second and see the output.



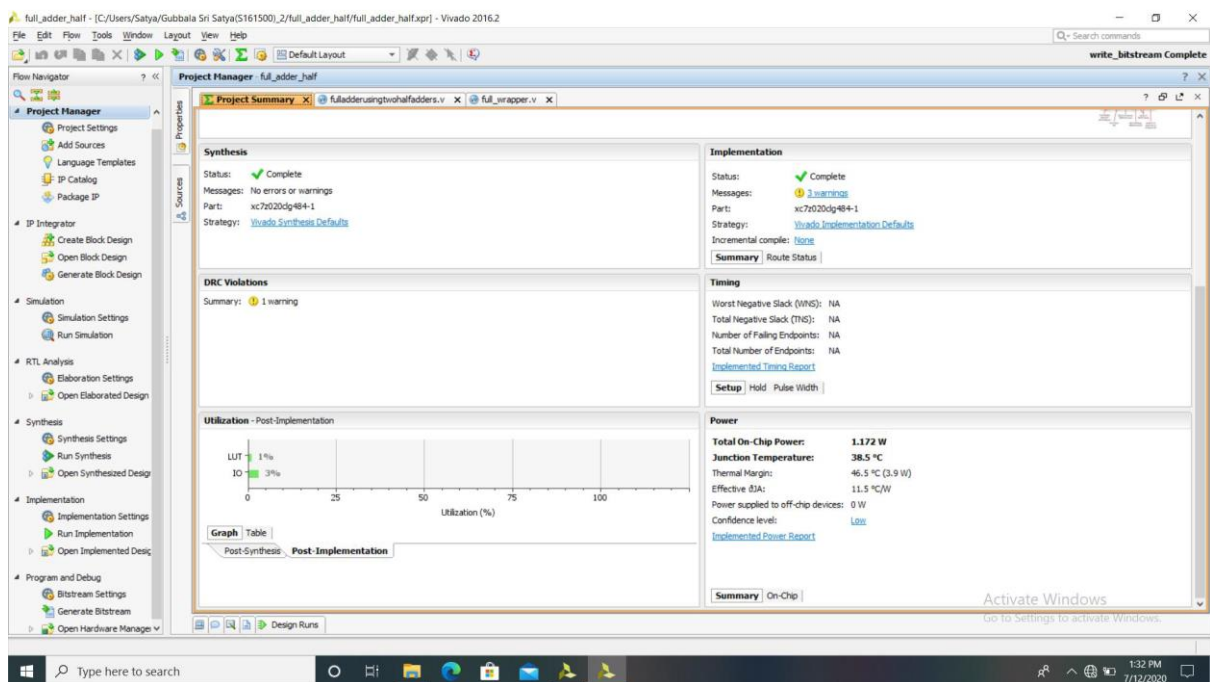
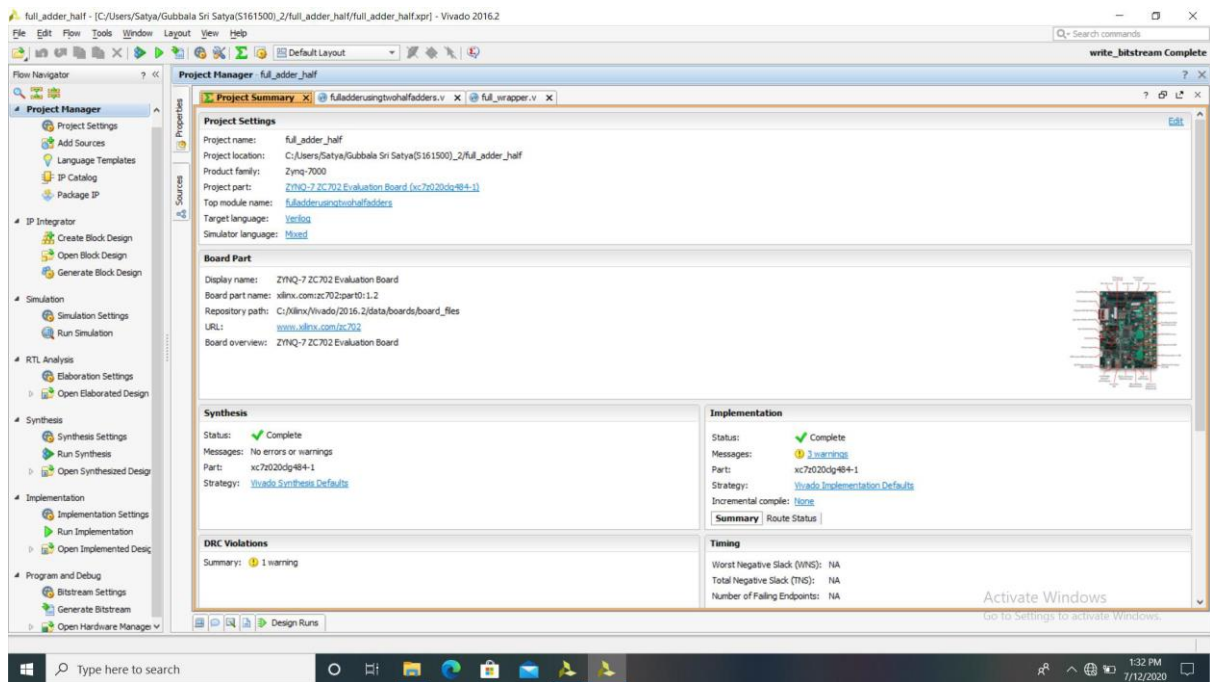
9. Click on Run Synthesis then Implementation and then generate bit stream. And generate IP for full adder.



10. Cascade 8 full adders to create 8-Bit Full Adder. Save the file and Validate the design and create hdl wrapper for this design. And Run Synthesis, Implementation, and Generate Bit stream.



11. The over all progress for this project can be seen in the Project Manager.



Result:8-Bit adder is successfully created.