Different benchmark circuits

ITC'99 benchmarks

1. Introduction

These consist of 22 RTL level sequential benchmarks, ranging from 45 gates and 5 FFs to 98,000 gates and 6600 flip-flops. Some of the larger benchmarks are composed of several of the smaller benchmarks connected together. They are all simple in the sense of being single clock designs, without internal memory or tristate buses

For more details, please refer to this website: https://ddd.fit.cvut.cz/prj/Benchmarks/ITC99.htm

2. Circuits description

Please see Figure1 and Figure2

	gates	#FF	PI	PO	#VHDL lines	#process		
b01	45	5	4	2	110	1	r	4_10 (9293)
b02	25	4	3	1	70	1	r	4_isbcd (9293)
b03	150	30	6	4	141	1	r	arbitro (9293)
b04	480	66	13	8	80	1	r	minmax (9394)
b05	608	34	3	36	319	3	r	elab_ram (9293)
b06	66	9	4	6	128	1	r	gest_int (9293)
b07	382	51	3	8	92	1	r	retta (9293)
b08	168	21	11	4	89	1	r	ric_incl (9293)
b09	131	28	3	1	103	1	r	67246 (9495)
b10	172	17	13	6	167	1	s	ostraco (9495)
b11	366	30	9	6	110	1	r	77449 (9596)
b12	1000	121	7	6	567	4	s	simon (9596)
b13	309	53	12	10	296	5	s	meteo (9495)
b14	3461	247	34	54	518	1	f	viper
b15	6931	447	37	70	648	3	f	80386

Figure1

	gates	#FF	PI	PO	#VHDL lines	#process		
	30	4	5			4		4_2
	35	4	11			4		4_2_e
	57	8	6			8		8_3
	78	8	27			8		8_3_e
	106	16	7			16		16_4
	170	16	67			16		16_4_e
	140	16	7			16		16_4n
b16	147	16	8	1	68 @	16	n	16_5n
	123	20	7			20		20_4
	211	20	83			20		20_4_e
	169	20	9			20		20_6n
	180	26	11			26		26_8
	249	28	11			28		28_8n
	197	28	19			28		28_16
	233	30	33			30		30_30
	508	64	19			64		64_16n
b17	21191	1407	38	97	135 *	6	n	
b18	49293	3308	37	30	94 *	1	n	
b19	98726	6618	47	40	65 *	2	n	
b20	7741	494	34	22	1040	3	n	
b21	7931	494	34	22	63 *	1	n	
b22	12128	709	34	22	1547	4	n	

Figure2

3. Supported format

In formats Bench, BLIF, Edif, VHDL

4. Download link

https://ddd.fit.cvut.cz/prj/Benchmarks/ITC99.7z

LGSynth'91 benchmarks(MCNC)

1. Introduction

The logic synthesis and optimization benchmark set consists of examples from four broad categories including Finite-state tables in KISS2 format, Sequential Multi-level logic in extended BLIF or SLIF, Combinational Multi-level logic in BLIF or SLIF format, Two-level logic in ESPRESSO or SLIF format.

For more details, please refer to this website:

https://ddd.fit.cvut.cz/prj/Benchmarks/LGSynth91.pdf

2. Circuits description

Just list all the combinational circuits. Please see Figure3,Figure4 and Figure5.

Combinational Multi-Level Examples

Circuit Name	Circuit Function	Inputs	Outputs	Approx. Gates
9symml	Count Ones	9	1	43
C1355	Error Correcting	41	32	546
C17	Logic	5	2	6
C1908	Error Correcting	33	25	880
C2670	ALU and Control	233	140	1193
C3540	ALU and Control	50	22	1669
C432	Priority Decoder	36	7	160
C499	Error Correcting	41	32	202
C5315	ALU and Selector	178	123	2307
C6288	16-bit Multiplier	32	32	2406
C7552	ALU and Control	207	108	3512
C880	ALU and Control	60	26	383
alu2	ALU	10	6	335
alu4	ALU	14	8	681
apex6	Logic	135	99	452
apex7	Logic	49	37	176
b1	Logic	3	4	13
b9	Logic	41	21	125
c8	Logic	28	18	164
cc	Logic	21	20	47
cht	Logic	47	36	229
cm138a	Logic	6	8	17
cm150a	Logic	21	1	69
cm151a	Logic	12	2	33
cm162a	Logic	14	5	43
cm163a	Logic	16	5	42
cm42a	Logic	4	10	17
cm82a	Logic	5	3	27
cm85a	Logic	11	3	38
cmb	Logic	16	4	41
comp	Logic	32	3	151
cordic	Logic	23	2	102
count	Counter	35	16	143
cu	Logic	14	11	48
dalu	Dedicated ALU	75	16	1697
decod	Decoder	5	16	22

Figure3

Circuit Name	Circuit Function	Inputs	Outputs	Approx. Gates
des	Data Encription	256	245	4000
example2	Logic	85	66	277
f51ml	Arithmetic	8	8	43
frg1	Logic	28	3	105
frg2	Logic	143	139	1004
i1	Logic	25	16	46
i10	Logic	257	224	2260
i2	Logic	201	1	109
i3	Logic	132	6	90
i4	Logic	192	6	120
i5	Logic	133	66	285
i6	Logic	138	67	340
i7	Logic	199	67	471
i8	Logic	133	81	1831
i9	Logic	88	63	522
k2	Logic	45	45	1201
lal	Logic	26	19	114
majority	Voter	5	1	9
mux	Mux	21	1	91
my_adder	Adder	33	17	223
pair	Logic	173	137	1434
parity	Parity	16	1	68
pcle	Logic	19	9	68
pcler8	Logic	27	17	84
pm1	Logic	16	13	39
rot	Logic	135	107	691
sct	Logic	19	15	91
t481	Logic	16	1	2072
tcon	Logic	17	16	41
term1	Logic	34	10	358
too_large	Logic	38	3	578
ttt2	Logic	24	21	200
unreg	Logic	36	16	97
vda	Logic	17	39	585
x1	Logic	51	35	285
x2	Logic	10	7	42
x3	Logic	135	99	715
x4	Logic	94	71	369
z4ml	2-bit Add	7	4	20

Figure4

Two-Level Examples

Circuit Name	Inputs	Outputs	Product Terms
5xp1	7	10	75
9sym	9	1	87
apex1	45	45	206
apex2	39	3	1035
apex3	54	50	280
apex4	9	19	438
apex5	117	88	1227
b12	15	9	431
bw	5	28	87
clip	9	5	167
con1	7	2	9
cordic	23	2	1206
cps	24	109	654
duke2	22	29	87
e64	65	65	65
ex4	128	28	620
ex5	8	63	256
ex1010	10	10	810
inc	7	9	34
misex1	8	7	32
misex2	25	18	29
misex3	14	14	1848
misex3c	14	14	305
o64	130	1	65
pdc	16	40	2406
rd53	5	3	32
rd73	7	3	141
rd84	8	4	256
sao2	10	4	58
seq	41	35	1459
spla	16	46	2296
t481	16	1	481
vg2	25	8	110
xor5	5	1	16
Z5xp1	7	10	128
Z9sym	9	1	420

Figure5

3. Supported format

In formats BLIF, Slif, Verilog, PLA, KISS2

4. Download link

https://ddd.fit.cvut.cz/prj/Benchmarks/LGSynth91.7z

https://ddd.fit.cvut.cz/prj/Benchmarks/MCNC.7z

EPFL Benchmarks

1. Introduction

It consists of 23 natively combinational circuits designed to challenge modern logic optimization tools. The benchmark suite is divided into arithmetic, random/control and MtM parts

For more details, please refer to this website:

https://www.epfl.ch/labs/lsi/page-102566-en-html/benchmarks/

2. Circuits description

Please see Figure6 .

TABLE IV
LUT-6 MAPPING EXPERIMENTS

Benchmark name	Inputs	Outputs	LUT-6 count	Levels
Arithmetic				
Adder	256	129	254	51
Barrel shifter	135	128	512	4
Divisor	128	128	9311	867
Hypotenuse	256	128	44635	4194
Log2	32	32	8008	77
Max	512	130	842	56
Multiplier	128	128	5913	53
Sine	24	25	1458	42
Square-root	128	64	5720	1033
Square	64	128	3985	50
Total	1663	1020	80638	6427
Random/Control				
Round-robin arbiter	256	129	2722	18
Alu control unit	7	26	29	2
Coding-cavlc	10	11	122	4
Decoder	8	256	287	2
i2c controller	147	142	365	4
Int to float converter	11	7	49	3
Memory controller	1204	1231	12096	25
Priority encoder	128	8	210	31
Lookahead XY router	60	30	89	7
Voter	1001	1	2691	16
Total	2832	1841	18660	112
MtM				
sixteen	117	50	5648909	29
twenty	137	60	7189658	33
twentythree	153	68	8246898	36
Total	407	178	21085465	98

Figure6

3. Supported format

In formats AIG, BLIF, Verilog, VHDL

4. Download link

https://ddd.fit.cvut.cz/prj/Benchmarks/EPFL.7z

Reference

I mainly refer to one website. The website link is as follows

https://ddd.fit.cvut.cz/prj/Benchmarks/