Dayananda Sagar College of Engineering

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A Report on RIPPLE CARRY ADDER

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CADENCE VIRTUOSO

- Cadence virtuoso is a very important EDA tool for electronics students learning about IC design/analysis and PCB design/analysis.
- At undergraduate level, virtuoso is majorly used for custom design and analysis of circuits based on MOS technologies, especially in the CMOS VLSI course.
- The Virtuoso System Design Platform allows IC designers to easily include system-level layout parasitic in the IC verification flow, enabling time saving by combining package/board layout connectivity data with the IC layout parasitic electrical model.
- It enables engineers to design concurrently across chip, package, and board, saving time and minimizing errors. It is ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices.

Some key benefits of Cadence Virtuoso are:

1. Easy to use, easy to understand software with an interactive interface.

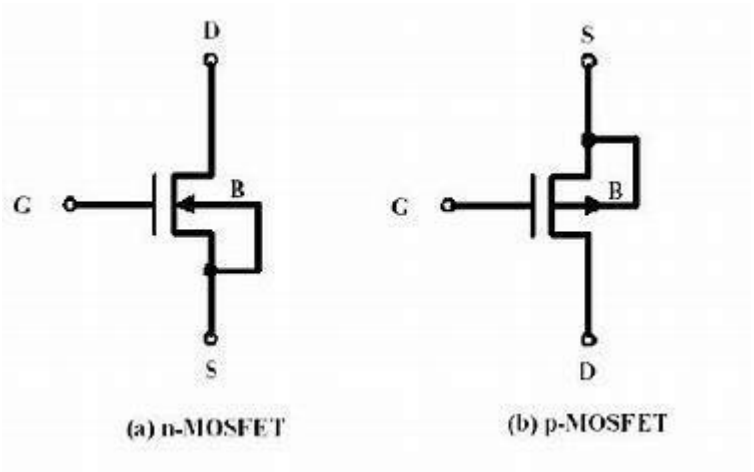
2. Supports circuit design by using symbols and structures in the workspace and also allows textbased design.

3. Great platform for beginners in the core industry to start learning about design and synthesis.

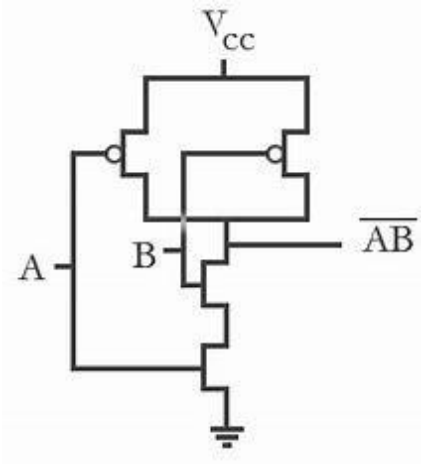
4. Allows the user to analyse the designs on various parameters like power consumption, area usage and delay.

INTRODUCTION

NMOS is a N channel metal oxide semiconductor system. It has P type Substrate and n+ type region in the drain and source. It is used to pass strong logic zero and weak logic1.
PMOS is a P channel metal oxide semiconductor system. It has N type Substrate and p+ type region in the drain and source. It is used to pass strong logic one and weak logic zero.



CMOS is Complementary metal oxide semiconductor system. It uses pair of NMOS and CMOS to design a different logic.
Below diagram shows CMOS circuit for 2 input NAND gate



RIPPLE CARRY ADDER

The **Ripple Carry Adder (RCA)** is a basic type of digital adder used in computing to add binary numbers. It is constructed using a series of **full adders (FAs)**, where each full adder computes the sum of corresponding bits from the input binary numbers and the carry bit from the previous stage.

Structure and Working

An RCA is made up of nn full adders for nn-bit binary numbers. The least significant bit (LSB) of the inputs is added in the first full adder, which generates a sum and a carry-out. This carry-out is fed as the carry-in to the next full adder, and the process continues until all bits are added. The last carry-out becomes the carry-out of the entire adder.

Advantages

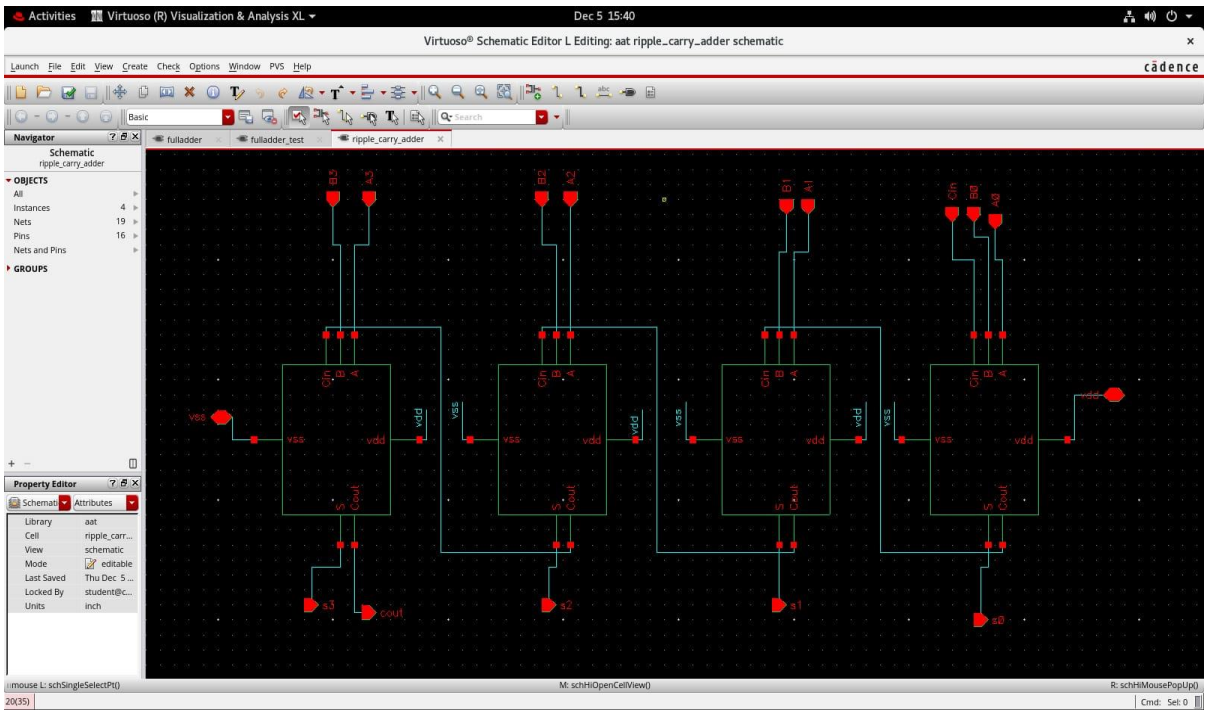
- **Simplicity**: The design is straightforward, making it easy to implement.
- **Low cost**: It requires fewer components compared to more complex adders.

Limitations

- **Propagation delay**: The carry-out from each full adder depends on the carry-in, so the computation time increases linearly with the number of bits. This makes RCAs slower for larger bit widths.
- **Not suitable for high-speed applications**: The sequential nature of the carry propagation limits its performance.

Applications

- RCAs are often used in simple, low-power systems where speed is not critical.
- They serve as building blocks in more complex arithmetic units or as a reference for designing faster adders like carry-lookahead or carry-save adders.



This schematic represents the design of a 4-bit Ripple Carry Adder (RCA) in Cadence Virtuoso. The circuit consists of four interconnected **full adder (FA) blocks**, each performing binary addition for one bit of the input numbers (AiA_i and BiB_i) along with a carry input (CinCin). The RCA is designed to calculate the sum and propagate the carry sequentially across its stages, producing sum outputs (s3s3, s2s2, s1s1, s0s0) and a final carry-out (CoutC_{out}).

Working Principle

- The first full adder takes the least significant bits of AA and BB along with the initial carry-in (CinCin), generating a sum (s0s0) and a carry-out.
- The carry-out from each full adder is forwarded as the carry-in to the next stage. This ripple effect continues until the final carry-out is produced after the last full adder.

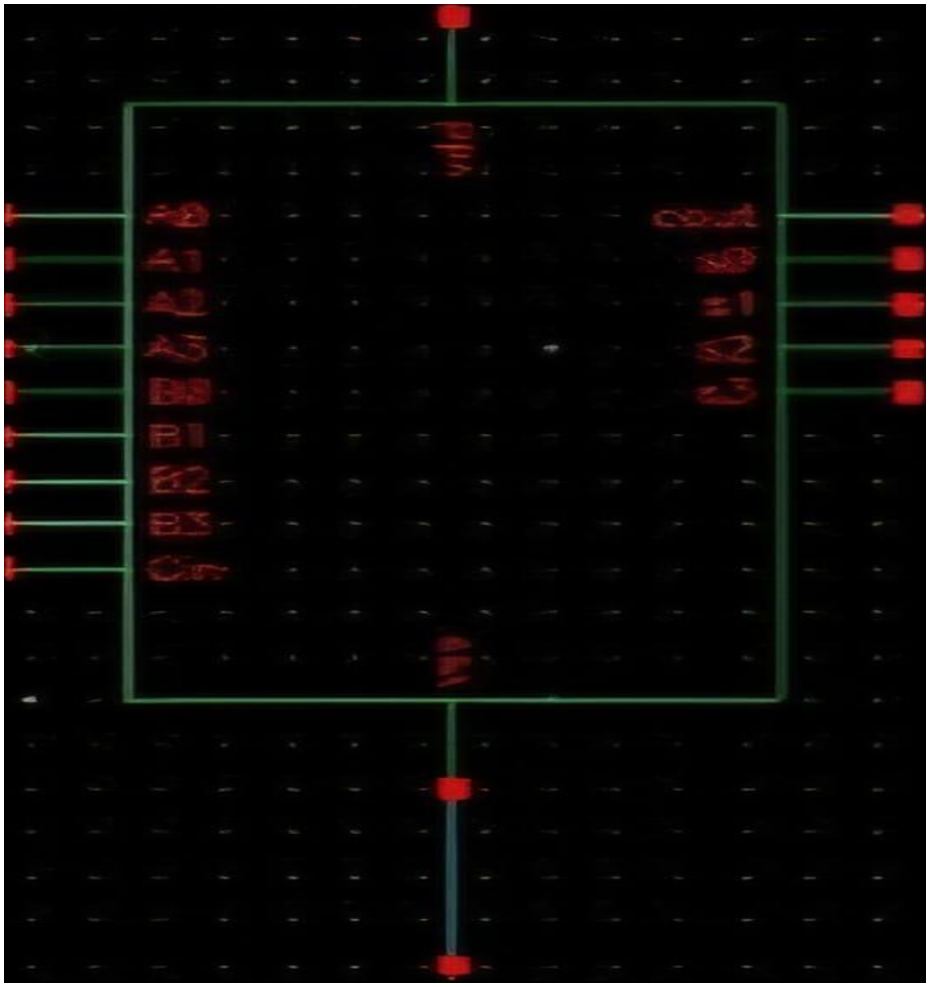
Design Details

- Each full adder block is powered by the supply voltage (VddV_{dd}) and connected to ground (VssV_{ss}).
- The wiring clearly shows the sequential connections of the carry-out from one adder to the carry-in of the next.
- The final outputs represent the binary sum of the 4-bit inputs and the carry result.

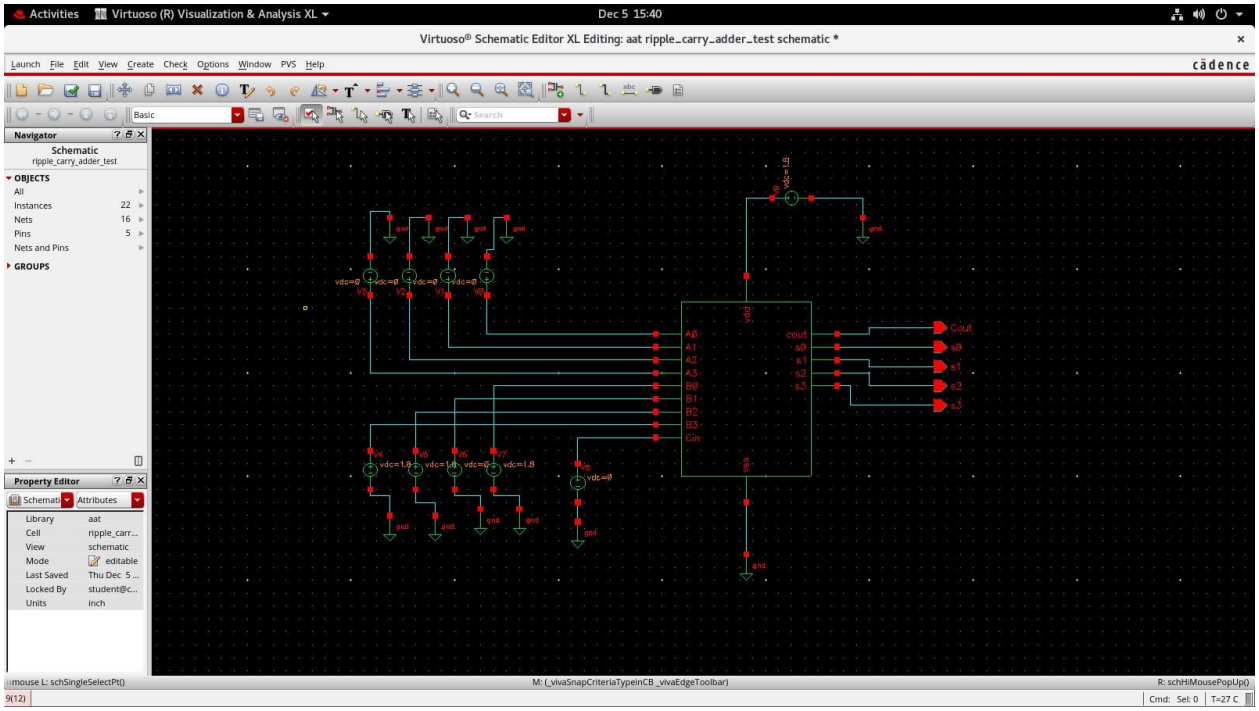
Key Characteristics

- The RCA design is simple and modular, making it easy to extend to larger bit-widths by adding more full adder blocks.
- However, it suffers from **carry propagation delay**, where the sum output of higher bits depends on the completion of carry propagation through earlier stages, limiting its speed for large-bit applications.

SYMBOL



TEST SCHEMATIC FOR RIPPLE CARRY ADDER



This schematic depicts a testbench setup for a 4-bit Ripple Carry Adder (RCA) circuit in Cadence Virtuoso. The central block represents the RCA module, with its inputs and outputs connected to test signal sources and measurement probes, allowing the verification of its functionality.

Circuit Description

- **Inputs:** The module takes two 4-bit binary numbers (A[3:0]A[3:0] and B[3:0]B[3:0]) and an initial carry-in (CinCin) as its inputs. These inputs are generated using test signal blocks visible on the left, configured to produce various logic patterns during simulation.
- **Outputs:** The RCA generates a 4-bit sum (s3,s2,s1,s0s3, s2, s1, s0) and a carry-out (CoutCout), which are routed to the right side of the schematic. Probes are placed here for waveform observation during transient simulations.

- **Internal Logic:** The RCA block contains interconnected full adders that perform the bitwise addition. The carry-out from one adder propagates to the next, following the ripple carry logic.

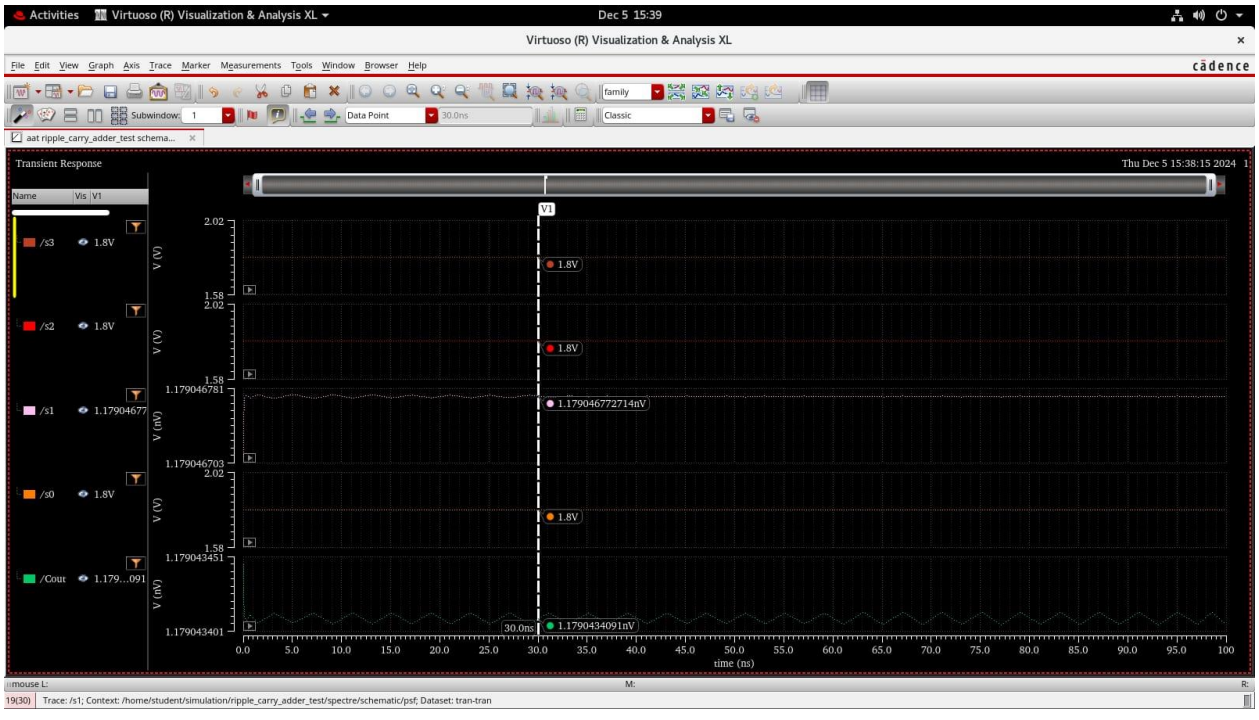
Additional Features

- **Power Connections:** The circuit is connected to VddV_{dd} (power supply) and ground, ensuring proper operation.
- **Test Signal Generation:** Signal blocks and inverters on the left create input signals to test the RCA's performance across a range of scenarios.

Purpose

This setup is used to verify the correct functionality and timing of the RCA. Waveform outputs from the simulation help evaluate the propagation delay caused by the ripple carry effect and ensure the adder produces accurate sum and carry outputs for all input combinations.

OUTPUT WAVEFORM



This image shows the transient simulation of a Ripple Carry Adder (RCA) circuit in Cadence Virtuoso. The waveforms represent the output signals (s3s3, s2s2, s1s1, s0s0) and the carry-out (CoutC_{out}) during the operation of the adder. The x-axis shows time in nanoseconds, while the y-axis represents voltage levels. Each output signal corresponds to a bit in the binary sum, and CoutC_{out} reflects the

carry propagation from the final stage. The voltage levels stabilize near 1.8V (logic HIGH) or 0V (logic LOW). The ripple nature of the RCA causes visible propagation delays between inputs and outputs, critical for timing analysis.

CONCLUSION

The Ripple Carry Adder (RCA) is a fundamental and straightforward digital circuit used to perform binary addition. Its modular design, composed of cascaded full adders, makes it easy to implement and extend for larger bit-widths. However, the sequential nature of carry propagation introduces significant delays, as the carry must ripple through all stages before the final output is determined. This limits its performance in high-speed applications. RCAs are ideal for small-scale, low-power systems where simplicity and cost-effectiveness are priorities. For faster performance, advanced adders like carry-lookahead or Kogge-Stone adders are preferred, but RCAs remain essential for understanding basic addition principles.