**IMPLEMENTATION OF VEDIC MULTIPLIER USING N-P BASED ECRL ADIABATIC LOGIC**

**ABSTRACT**:

Low power VLSI design methodology is crucial in the current context since low power devices require fewer heat sinks and hence less area, which is a cost-effective process. The "delay" option in this method of designing low-power circuits has a significant cost. Keeping this in mind, Adiabatic Logic is used to create an N-P based ECRL 4X4 Vedic multiplier with the goal of decreasing power dissipation . As previously stated, power dissipation and delay are two opposing characteristics. This research has lowered power dissipation by 28.30% when compared to an existing ECRL based 4X4 Vedic Multiplier at the expense of delay.

**Contribution of the paper**:

The paper is divided into six sections. The Introduction is the first section. The second portion covers adiabatic logic, which is divided into three subsections: operating concept, mathematical demonstration of power reduction in adiabatic logic circuits, and adiabatic circuit types. As subsections of ECRL logic, the third component comprises of merits and demerits. The proposed transmission logic operation is described in the fourth part, along with its advantages over ECRL logic. The suggested transmission logic is used to create logic circuits such as fundamental gates, combinatorial circuits, and Vedic multipliers in the fifth section. Furthermore, the performance of both existing and proposed logics is analyzed and compared in terms of power dissipation and delay metrics in the sixth part. Finally, the document is ended by presenting the results of the study, followed by the inclusion of reference papers.

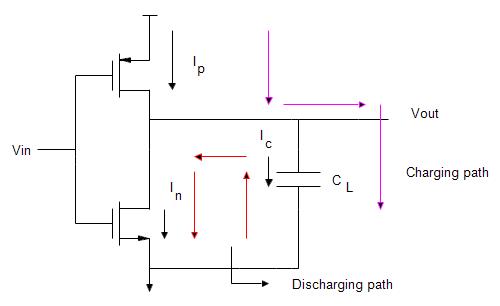
**1.INTRODUCTION**:

The today's world is rapidly adjusting to new technologies. The technology that is used today is entirely reliant on two fundamental elements. The first is because of the software that has been using today to create a new technology, and the second is because of the hardware that supports it. When it comes to hardware circuits, there are a number of elements to consider when assessing overall functionality. Power dissipation, propagation latency, and device area are among the parameters. During the past decades CMOS was responsible for creating low power equipment [1].Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances, which cause power dissipation increasing with the clock frequency[1]. Power dissipation in CMOS can be reduced by decreasing the terminal capacitance value and by reducing the voltage supply[2]. This results in low performance of device[2].The adiabatic technique prevents such losses[3].Hence adiabatic logic is proposed for low power consumption in later researches. Efficient charge recovery logic (ECRL) is one of the standard logic style investigated from Adiabatic logic[4].It is observed that ECRL has a voltage drop problem and increase in delay. Therefore, N-P based ECRL logic is proposed in this paper to overcome the disadvantages of ECRL adiabatic logic. This paper gives the description of the performance and comparative analysis of existing ECRL Vedic Multiplier with the proposed N-P based 4X4 vedic multiplier in power dissipation, propagation delay and area metrics. The next section explains adiabatic logic styles in detail.

**2. ADIABATIC LOGIC**:

Adiabatic logic circuits are low-power electronic circuits that save energy by employing "reversible logic." The term adiabatic refers to a thermodynamic process that exchanges no energy with the surrounding environment. Power is dissipated by CMOS transistors during switching. The need to charge and discharge the gate capacitance C via an electronic device with some resistance R accounts for the majority of this dissipation. Ediss=(RC/T) CLVdd2 is the energy dissipated when charging the gate[5]. Where T denotes the time required for the gate to charge or discharge. The charging time T in non-reversible circuits is proportional to RC. Because a single clock cycle is much longer than RC, reversible logic attempts to distribute gate charging over the entire cycle. The energy is not dissipated but it is recycled. The energy stored in load capacitor is given by E stored= 1/2 CLVdd2[2]. As a result, energy dissipation is reduced.

**2.1. Operation of adiabatic logic circuits**:

The power source in adiabatic logic is a ramp signal. It is a slowly varying ramp signal, whereas with static CMOS logic, the power supply is constant VDD. Because the **power in static CMOS** is constant VDD, no matter how much power it has been given , the entire power will evaporate across the resistor, while the energy held in the capacitor will be less or zero. As a result, whatever power supplied as a voltage source in static CMOS logic will be dissipated across the resistor.

In **adiabatic logic**, a slowly varying ramp signal is offered as the input voltage source, which results in a slowly varying ramp signal appearing only at the resistor. A linear increase in T causes a linear decrease in power dissipation[6].Adiabatic discharge can be arranged in a similar manner with a descending ramp[6]. As a result, the power dissipation across the resistor will be very low, and the capacitor will begin to charge after some time.

**Fig 2.1.a. CMOS inverter**

As a result, the energy wasted by the resistor will be lower during the charging phase, while the energy held by the capacitor will be higher. And, because the energy dissipated by the resistor is lower during the discharging phase, some of the energy held across the capacitor will be sent to the source, which is known as the **energy recovery technique**.

It implies that some of the energy stored in the capacitor is returned to the source during discharging. Because the capacitor is charged with a steadily varying ramp signal in adiabatic logic. In comparison to static CMOS circuits as shown in Fig 2.1.a, the voltage across the resistor is substantially lower, and the energy stored in the capacitor is greater than the energy released by the resistor while charging or discharging. The sources of power dissipation are covered in the next section.

**Sources of Power Dissipation:** The power dissipation in CMOS circuits majorly arrives from two sources. They are**:**

**(1) Dynamic dissipation caused by:**

* the charging and discharging of load capacitance.
* The "short circuit" current that flows while both PMOS and NMOS are partially turned on
* Pdynamic = Pswitching + Pshort circuit..........................................(1)

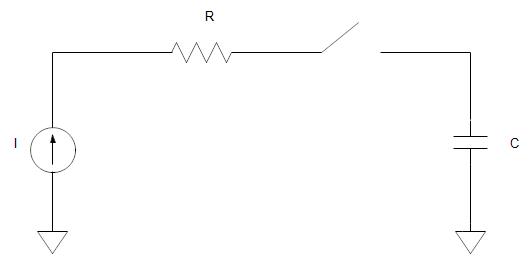
**(2) Static dissipation due to:**

* When VgsVt MOSFETs are turned off, subthreshold leakage current flows between the drain and the source, which is the primary source of static power dissipation.
* Leakage current flows from the gate to the body.
* When a source or drain diffusion region has a different potential than the substrate, junction leakage occurs.

Pstatic= (Isub+ Igate + Ijunction)Vdd...........................(2)

* Therefore, Ptotal = Pdynamic + Pstatic.............................(3)

Over the next section, mathematical verification is performed to verify power decrease in adiabatic circuits when compared to CMOS circuits.

**2. 2. Mathematical Proof of Power reduction in Adiabatic circuits:**

In adiabatic switching if we supply constant current source then it will result in a linear voltage ramp. Let us assume initially there is zero capacitance voltage (Vdd). We know that charge stored in a capacitor is directly proportional to voltage applied across its terminals i.e., Q=CLVdd  (2.4)

Where CL is Load Capacitance value that is proportionality constant. And also, we have charge (Q)=Current(I)/Time(T) Fig. 2.1.1 Circuit Explaining Adiabatic Switching

i.e., Q=I/T……… . (2.5)

By rearranging the terms 🡺 Vdd=(I.T)/CL ……… (2.6)

The total amount of energy dissipated in the resistor R from t=0 to t=T can be calculated as follows: Ediss =integration of p(t) dt where p(t)=I2 R…from 0 to T.



🡺Ediss=R.I2.T ………… (2.7)

From (2.6) I=(Vdd.CL)/T ……….. (2.8)

Therefore substitute (2.8) in (2.7) we get:

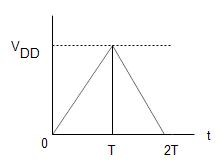
🡺Ediss= (RC/T)\*CVdd2…. (2.9)

Energy dissipation in CMOS circuits: T=2RC

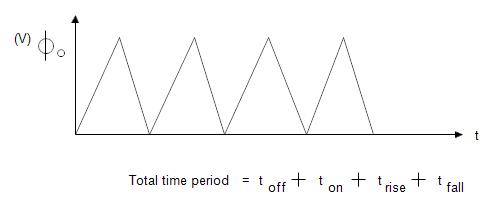
🡺 Ediss=(1/2)\*CVdd2 ….. (2.10)

Energy dissipation in Adiabatic circuits: T>2RC 🡺 here ramp voltage Time period is 2T 🡺 Ediss=(RC/2T) \*CVdd2🡺 Ediss=(RC/4RC) \*CVdd2

**🡺** Ediss=(1/4)\*CVdd2............ (2.11)

 Fig. 2.1.2 Triangular Supply of One Time Period

Hence, the power dissipation Pdiss=Ediss/T🡺Pdiss=C.Vdd2. f Since Energy dissipation and Power dissipation are directly proportional to each other, we can say that the power dissipated in Adiabatic circuits is reduced compared to CMOS circuits by increasing the charging and discharging duration.

**2.2. a. TRIANGULAR SUPPLY FOR ADIABATIC SWITCHING**:

The shape of the power clock generator is critical to how adiabatic logic circuits work. The power clock we used here is a triangular supply as shown in fig 2.2.a with frequency and voltage levels, just like a clock. This triangular supply is a two-phase supply, which means it has two levels: one rising and one falling. Hence Total supply time period=Ton+ Toff+ Trise+ Tfall

🡺 T=0+0+(T/2)+(T/2)…………………….(7)

**Fig 2.2.a. Periodic Time varying supply**

The time during which the load capacitor charges is referred to as the Trise. Tfall is the time it takes for the load capacitor to discharge. The following Section 2.3 depicts the adiabatic logic types and their tree structure.

**2.3. TYPES OF ADIABATIC LOGIC CIRCUITS:**

There are two types of adiabatic logic circuits:

i. Reversible logic (ECRL) ii. **Efficient Charge Recovery Logic (ECRL)**

🡺 This energy/charge recovery logic (ECRL) is separated into two sub-categories once again.

1. Asymptotically energy recovery logic/adiabatic logic

2. Quasi energy recovery logic/quasi adiabatic logic

🡺 Coming to the asymptotically energy recovery logic there are 3 main categories

a) Push-pull operation/latch type eg: 2N-2N-2N

b) Driving with split level pulses eg: 1N-1N

c) Driving with nested pulses eg: 1N-1N and 2N-2N-2N

🡺 Quasi energy recovery logic is broadly classified into 3 types

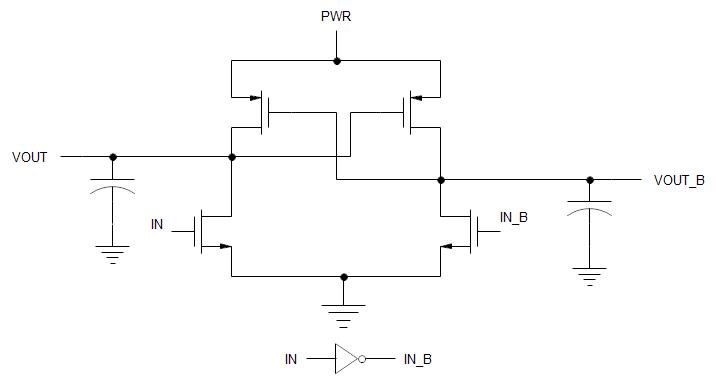
a) Single phase power clock eg: SCAL, CAL AND TSCL

b) Two phase power clock eg: PAL

c) Four phase power clock eg: 2N-2P, 2N-2N, DCPAL, PACAL, PFAL, CPAL,

ICPAL and NERL

**3. ECRL LOGIC:**

Cross-coupled PMOS transistors are used in Efficient Charge – Recovery Logic (ECRL). With differential signaling, it has a topology similar to Cascode Voltage Switch Logic (CVSL). It comprises of two NMOS transistors and two cross-coupled transistors M1 and M2[4]. ECRL gates are powered by an AC power source called PWRC, which allows the energy to be recovered and reused. The power clock generator generates both out and outbar so that it can always drive a consistent load capacitance regardless of the input signal. That is to say, ECRL always pushes full-swing charge into the output. However, as the supply clock voltage approaches. By returning provided energy to the source, ECRL saves energy. To efficiently replenish the charge, an AC power supply is required.

**Fig3.a. ECRL inverter**

As a result, we employ a triangular supply in this case. When the input is "1" and the triangle supply is rising, the NMOS is turned on in the ECRL inverter shown in Fig.3. a. Because the NMOS ON capacitor charges to 50% of the supply power. As a result of the dropping edge of the triangle supply, the capacitor will discharge and then PMOS will turn on. During the discharging process, the ECRL logic saves and reuses some part of the energy for each cycle.

**3.1. Disadvantages of ECRL :**

1.The delay will get increased if the rise time and fall time of the power supply is increased.

2.The ECRL logic reduces the power dissipation at the expense of delay.

3.It has voltage drop problem.

4.The gate count increases for every logic circuit that is implemented using this technique

So, to overcome all these demerits of ECRL logic to some extent, the transmission gate logic has been proposed. It is discussed in the upcoming section 4.

**4. Proposed N-P based ECRL Logic:**

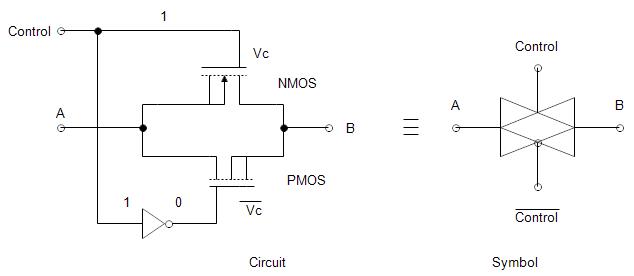
The voltage drop problem of the pass transistor logic is solved using transmission gate logic. The complimentary features of PMOS and NMOS transistors are used in this technology, with the NMOS device passing a strong '0' but a weak '1'. A strong'1' is passed by the PMOS device, whereas a weak'0' is passed by the PMOS device. By connecting the two devices in parallel, the transmission gate achieves the best of both devices shown in fig 4.a. The transmission gate's basic operation is described in Section 4.1.

**Importance of N-P based ECRL logic in power reduction:**

The power dissipation of adiabatic logic circuits can be minimized by lowering the PMOS ON resistance (R) or lengthening the supply voltage charging interval (T).

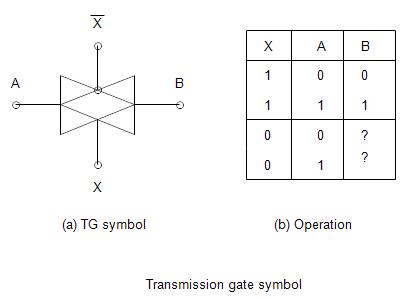
1.To reduce power dissipation, the existing ECRL adiabatic logic with triangle supply has used the method of increasing the charging duration of the power supply.

2.The resistance is reduced by placing PMOS and NMOS in parallel in the proposed N-P based ECRL logic. As a result, power dissipation is reduced to a more acceptable level.



**Fig 4.a. Transmission gate and its symbol**

The transmission gate symbol below in fig 4.b. depicts this bilateral action, with two overlaid triangles pointing in opposing directions to represent the two signal directions.



**Fig 4.b. Transmission gate symbol and its truth table**

**4.1. Transmission gate logic** **operation:**

(1). CASE I: When the Control signal is logic'0' (low), the gates of the PMOS and NMOS transistors are linked to logic"1" and logic"0," respectively. As a result, both transistors are in cutoff mode, resulting in a state of high impedance. Therefore, the transmission gate serves as an off switch.

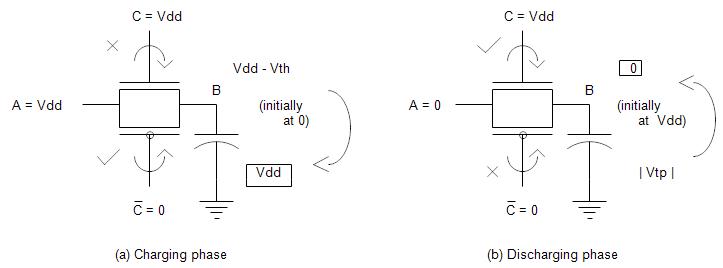
(2).CASE 2: When the Control Signal is logic 1 (High):

Both pass transistors are turned on, and they work as a closed switch, enabling the signal from the source side to travel through the gate and into the drain.

As a result, It is observed that A=B..

🡺 Transmission gate behaviour for various inputs when it is turned on:

**(1)When A is equal to VDD(logic'1'**): When input logic '1' passes through an NMOS transistor, the output node 'B' is pulled up to VDD-Vtn and the transistor is turned off. So NMOS can pass strong'0' but not strong'1'. The strong'1' has now arrived at the drain end thanks to this PMOS. Because PMOS can pass Strong '1' and acts as a PULL UP network by driving node B from "VDD-Vtn" to "VDD," it acts as a PULL UP network. As a result, capacitor is charged all the way through VDD through PMOS, and it can be concluded that this Transmission gate has passed strong '1'.

**(2) If A=VSS(logic '0'),** then: When it passes via a PMOS transistor, it cannot pass a strong'0' and will instead pass a weak'0'. As a result, this capacitance will only be charged up to |Vtp|. Because the NMOS transistor is a PULL DOWN transistor, it can pass Strong'0' by firmly pulling down the |Vtp| to '0' when input logic'0' is passed through it. As a result, Strong'0' is transmitted by this NMOS rather than through the PMOS, implying that thiscapacitor is fully depleted from VDD to 0. As a result, It is said that the transmission gate has passed strong'0'**.** 

**Fig 4.1.a. Charging and discharging phases of transmission gate**

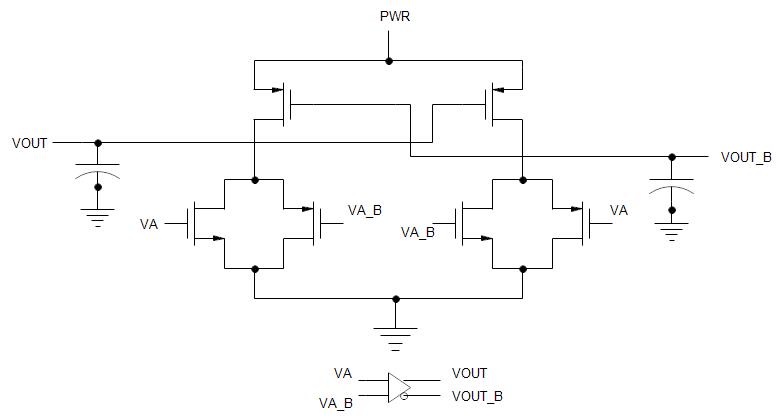
**4.2 Advantages of N-P based ECRL logic:**

* Complex gates can be implemented using minimum number of transistors, which also reduces parasitics.
* The combination of both an PMOS and NMOS in Transmission Gate arrangement avoids the problem of reduced noise margin, increase switching resistance and increased static power dissipation (caused by increased Threshold Voltage), but requires that the control and its complement be available**.**

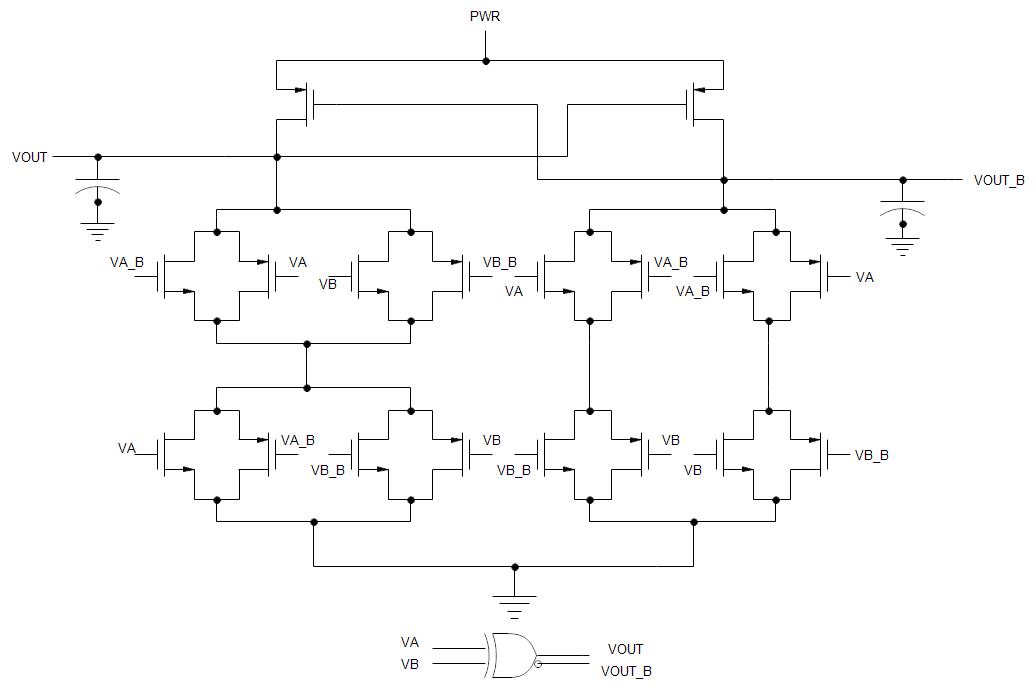
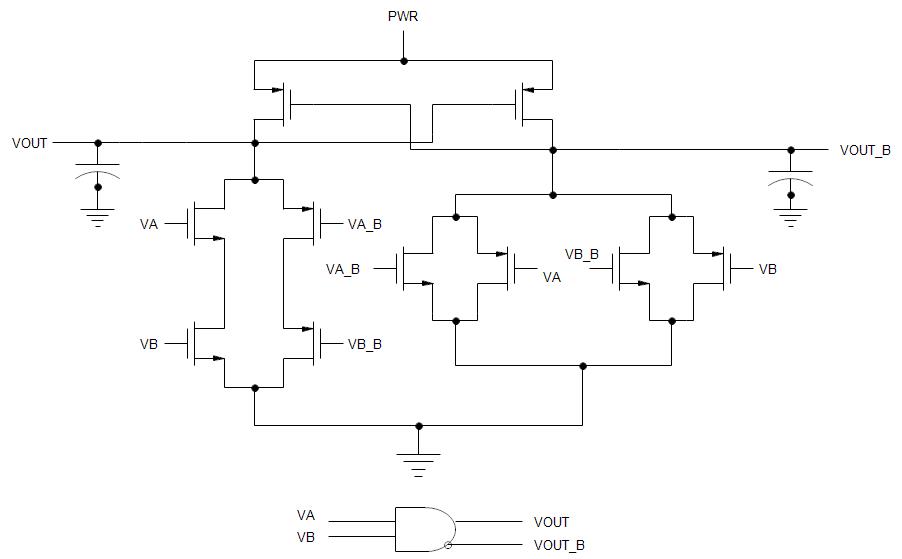
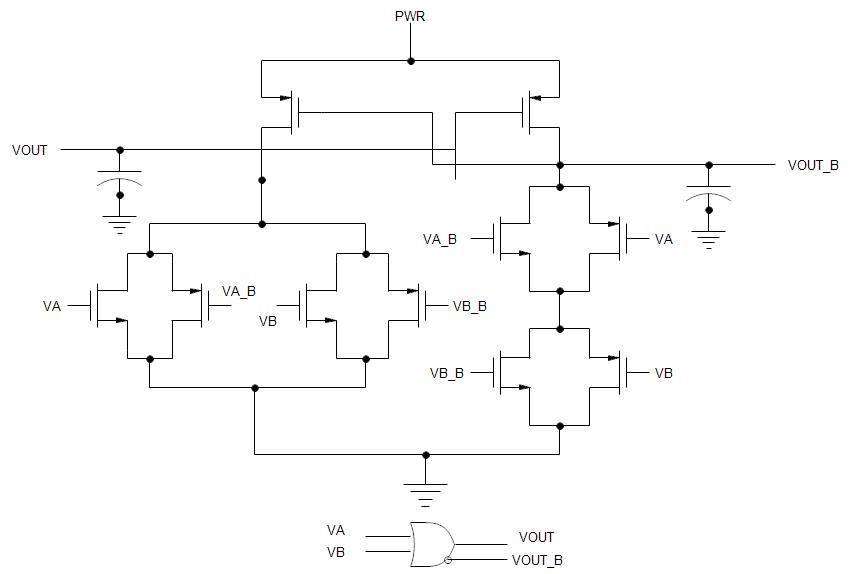
**5.Logic circuit implementation using Transmission gate logic**

**5.1.Schematic of proposed N-P based ECRL basic gates:**

**Fig 5.1.N-P Based ECRL Inverter**

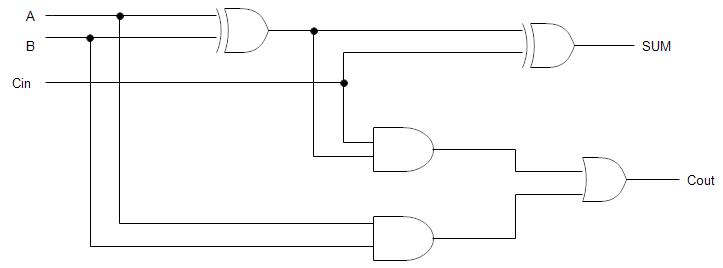
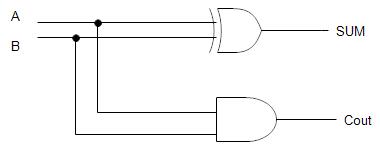


**Fig 5.2. N-P Based ECRL OR-NOR GATE**

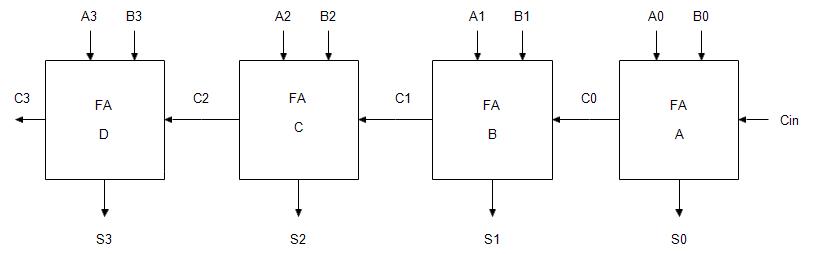
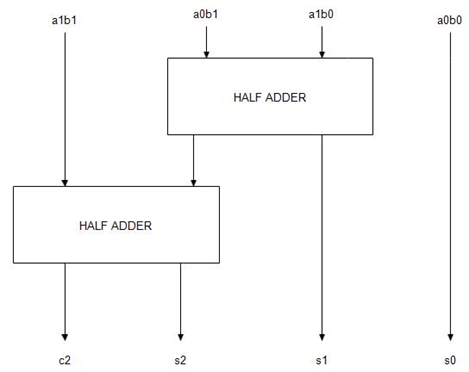
**5.2.Schematic of N-P based Half adder,Full adder ,Ripple carry adder and 2X2 Vedic Multiplier:**

**Fig 5.3 N-P Based ECRL AND- NAND GATE**

**Fig 5.4 .N-P Based ECRL XOR-XNOR GATE**



**Fig 5.6. N-P Based ECRL Full Adder**



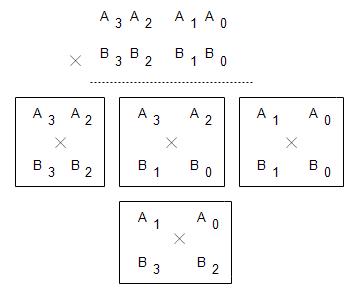
**Fig 5.8. N-P Based ECRL 2X2 Vedic Multiplier**

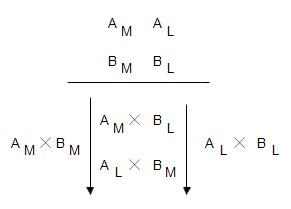
**Fig 5.7. N-P Based ECRL Ripple Carry Adder**

**Fig 5.5 N-P Based ECRL Half Adder**

**5.3. Vedic Multiplier:**

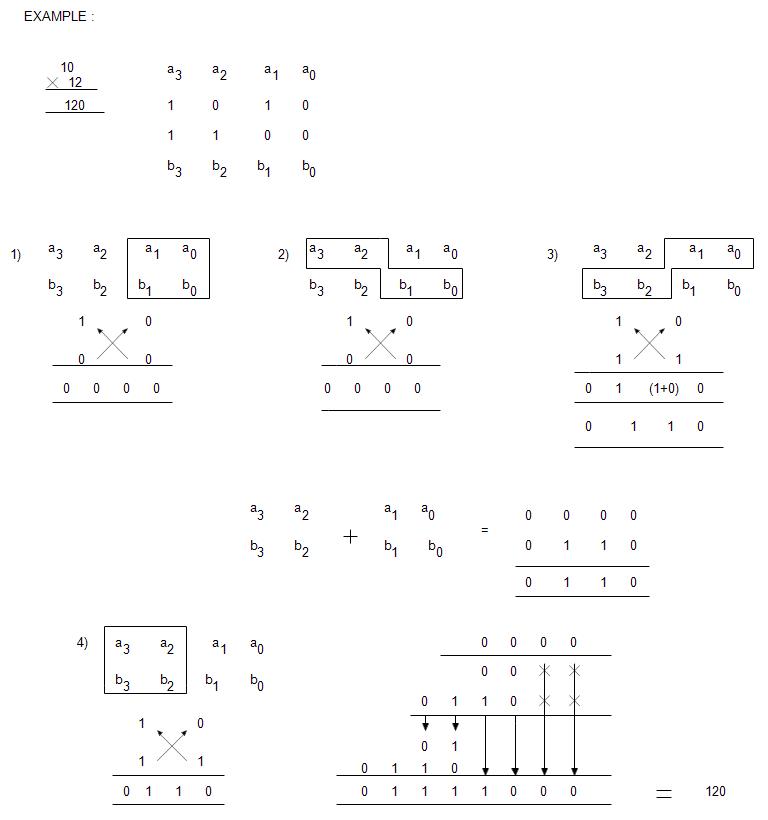
The Vedic Multiplier is one of the fastest multiplier. It follows Urdhva-Triyakbhyam sutra. Therefore, structure of Vedic Multiplier is Vertical & Crosswise. Since the partial products and their sum are calculated in Parallel, it generates all partial products and their sum in one step. Here since the generation of partial products and their sum are calculated in parallel (that is together), the multiplier is independent of clock frequency of the processor.



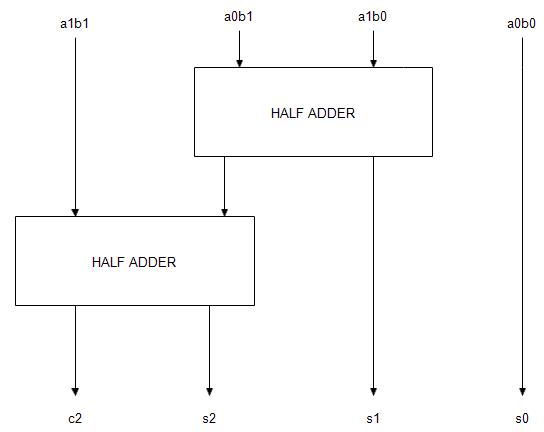
**Urdhva–Triyakbhyam**:

**Fig 5.3.a. General representation of vedic multiplication**

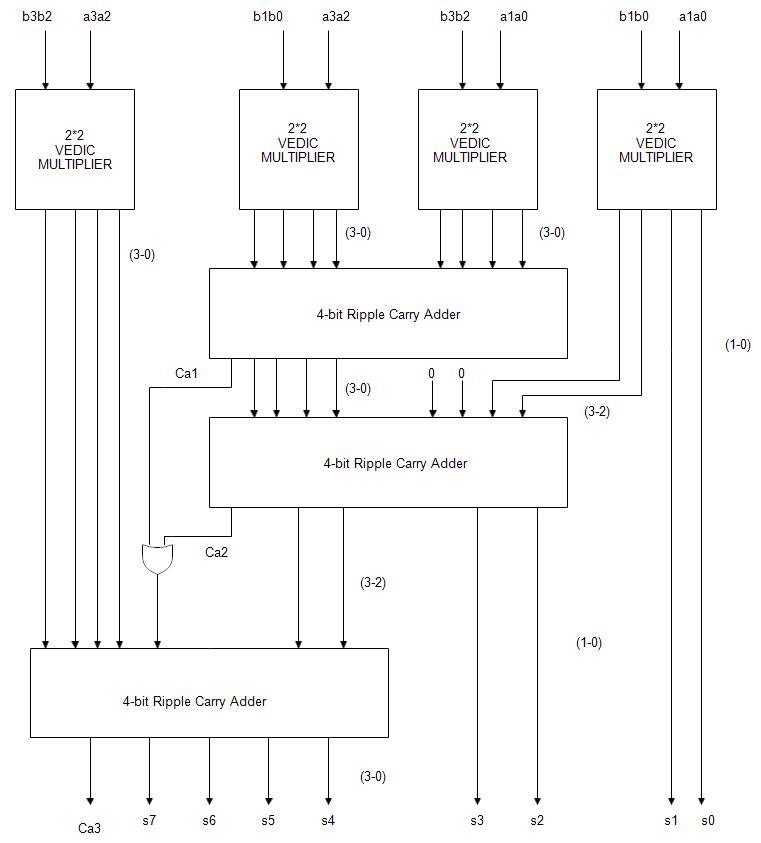
**Fig 5.3.b. representation of 4X4 vedic multiplication**

The word “Urdhva-Tiryakbhyam” resources vertical and crosswise multiplication. This multiplication formula is pertinent to all cases of algorithm for N bit numbers. Urdhva Triyakbhyam Sutra is performed by two multiplication techniques that is straight above multiplication and diagonal multiplication. Then finally, their sum is taken. Figs 5.3.a and 5.3.b represents the implementation of vedic multiplication. The fig 5.3.c. explains the 4bit vedic multiplication. The advantage of this multiplier is that as the number of bits increases, delay and area is less compared to other multiplier s.The 2x2 Vedic multiplier and 4X4 Vedic multiplier are shown in Fig5.3.d and Fig 5.3.e.

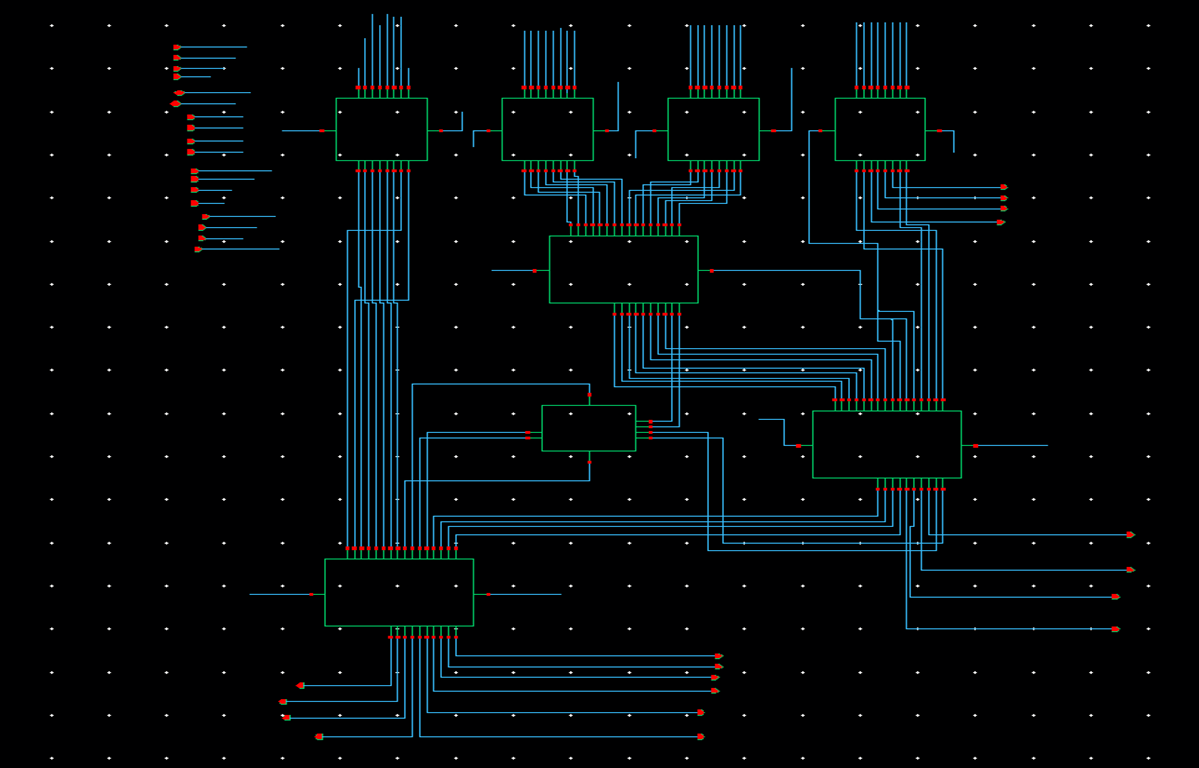
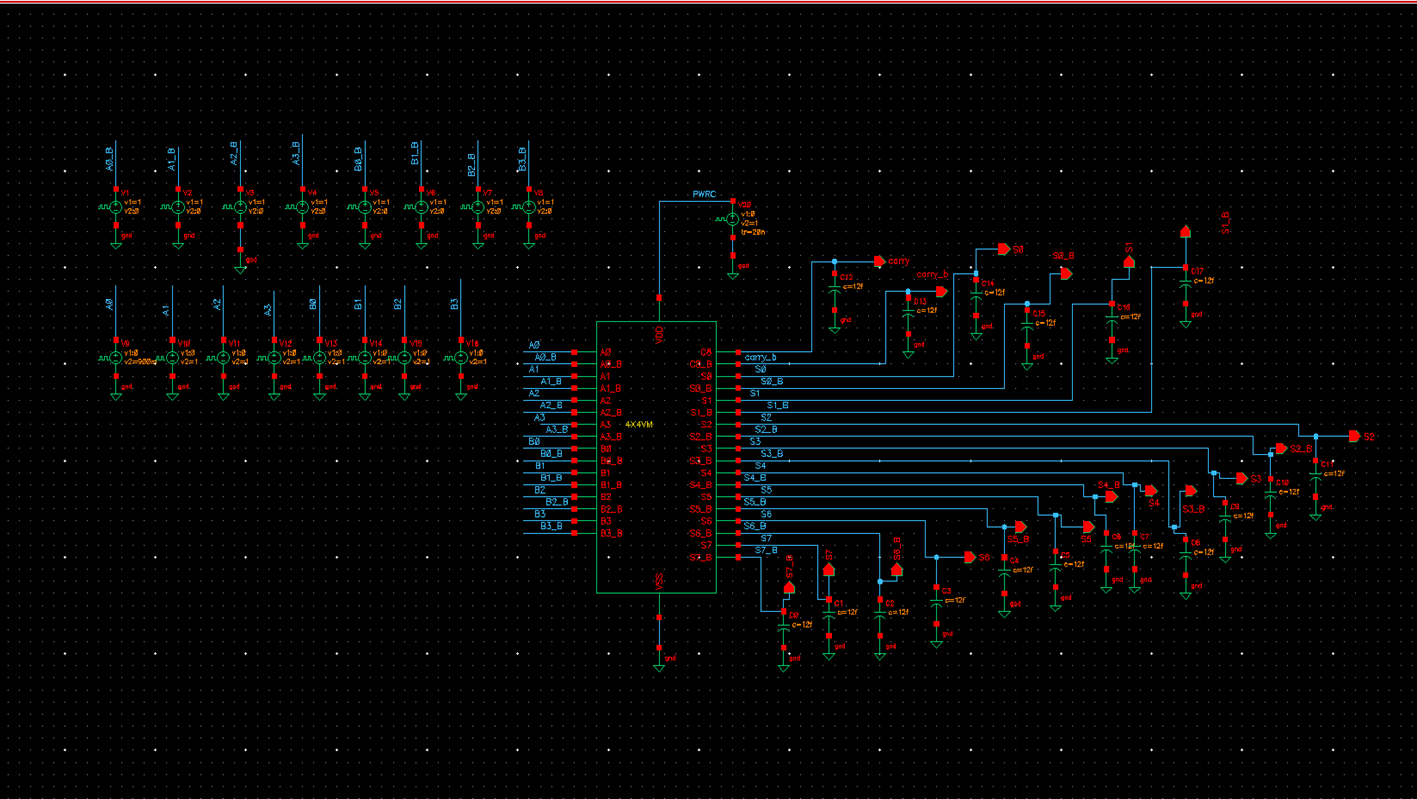
**Fig 5.3.c. Example of 4bit vedic multiplication**

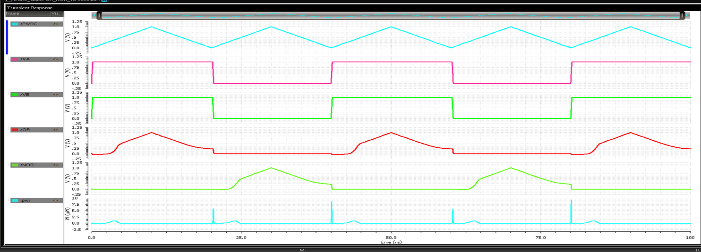


**Fig 5.3.d. Block diagram of 2X2 Vedic Multiplier**

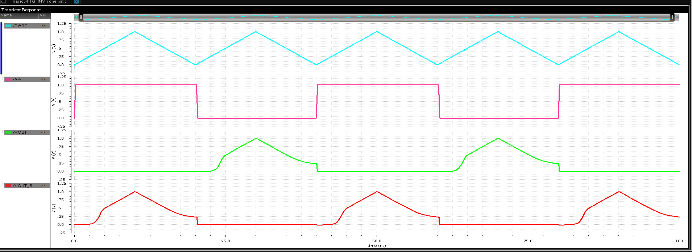


**Fig 5.3.e.Block diagram of 4X4 Vedic multiplier.**

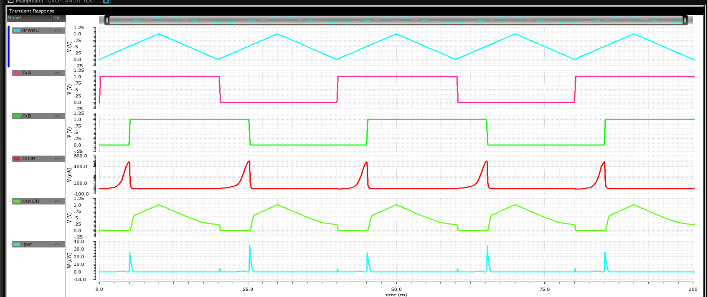
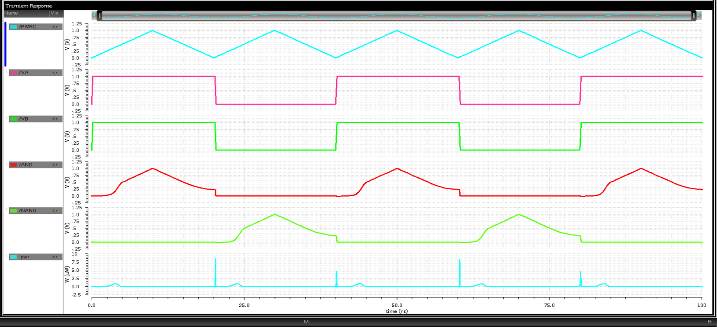
**5.3 Schematic of N-P based 4X4 Vedic Multiplier:**

**6.Simulation results and analysis:**

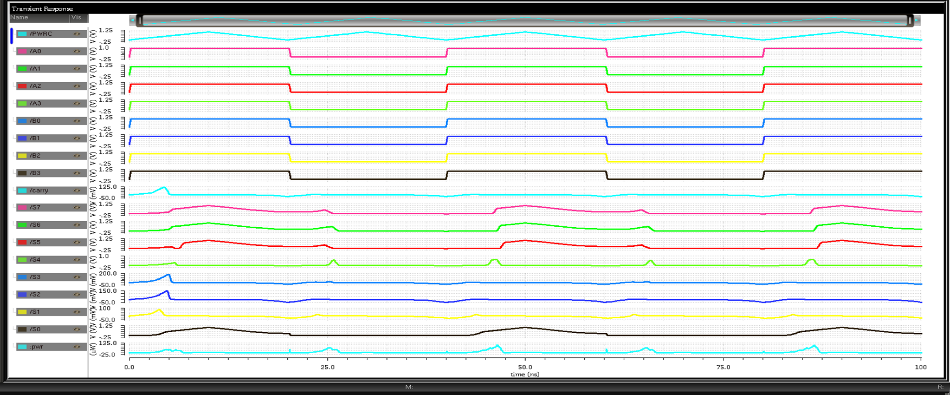
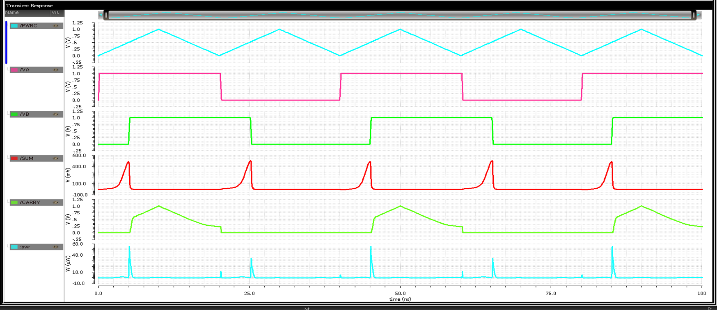
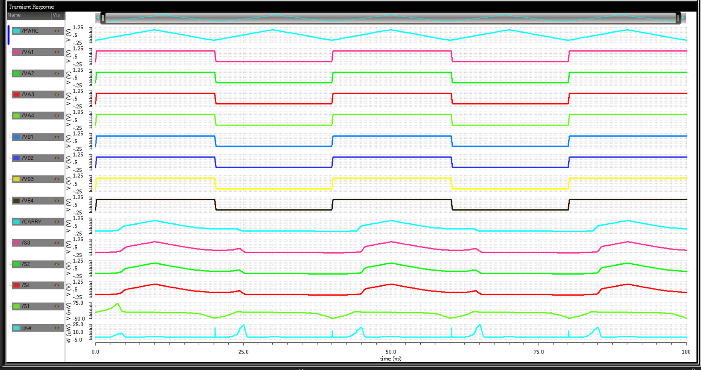
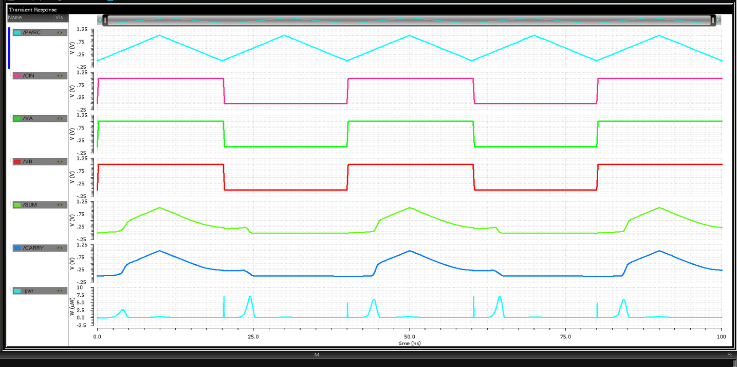
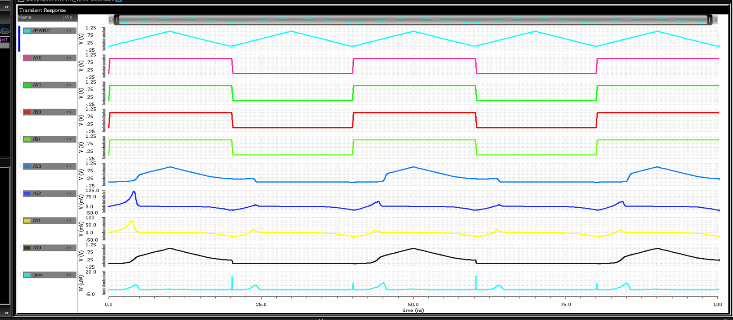
**Fig 5.9. Schematic of N-P Based ECRL 4X4 Vedic Multiplier**



**Fig 4.2 .N-P Based ECRL OR\_NOR GATE**

** Fig 4.1 .N-P Based ECRL inverter**

**Fig 4.3. N-P Based ECRL AND-NAND GATE**

****

**Fig 4.9.N-P Based ECRL 4X4 Vedic Multiplier**

**Fig 4.8. N-P Based ECRL 2X2Vedic Multiplier**

**Fig 4.4. N-P Base ECRL XOR-XNOR GATE**

**Fig 4.6.N-P Based ECRL Full Adder**

**Fig 4.5.N-P Based ECRL Half Adder**

**Fig 4.7. N-P Based ECRL Ripple Carry Adder**

**6.1 N-P based ECRL Logic circuits functionality:** Each of the circuits depicted in section 5 has its own logic for product generation. Figures 5.1 to 5.4 show the schematic implementation of basic gates such as inverter-buffer, Or-Nor, And-Nand, and Xor-Xnor gates using N-P based ECRL logic. Each basic gate has two complementary outputs. Figures 5.5 to 5.7 show the schematic implementation of adders such as the half adder, full adder, and ripple carry adder. Figure 5.8 depicts the schematic 2x2 vedic multiplier, while Figure 5.9 depicts the 4X4 vedic multiplier. Figures 6.1 to 6.4 depict simulation results for inverter,Or-Nor,And-Nand, and Xor-Xnor gates, which are used to validate the functionality of each circuit. Figures 6.5 to 6.9 show the functionality of a half adder, full adder, ripple carry adder, 2X2Vedic Multiplier, and 4X4Vedic Multiplier, respectively. All of these circuits can now be created with fewer transistors because of the proposed transmission gate logic. As a result, the number of gates has been drastically reduced. The space, power consumption, and cost features are all lowered as a result of the lower gate count. Finally,the suggested N-P-based ECRL 4X4 vedic multiplier produces accurate outputs for a wide variety of inputs while running at an acceptable speed, taking up little space, and costing little power..

**7.Performance Evaluation**:

**7.1 DELAY COMPARISION TABLE OF BASIC GATES:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Basic Gate** | **Existing ECRL Logic Delay(ns)** | | | | **Proposed N-P Based ECRL Logic Delay(ns)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **1.INVERTER** | **4.709** | **0.056** | **4.805** | **0.177** | **4.710** | **0.0612** | **4.808** | **0.176** |
| **2.OR** | **4.909** | **0.029** | **5.006** | **0.127** | **0.005** | **0.0348** | **5.007** | **0.128** |
| **3.NOR** | **4.713** | **0.111** | **4.812** | **0.288** | **4.716** | **0.118** | **4.816** | **0.273** |
| **4.AND** | **4.913** | **0.117** | **5.010** | **0.287** | **4.916** | **0.112** | **5.015** | **0.271** |
| **5.NAND** | **4.709** | **0.030** | **4.806** | **0.127** | **4.710** | **0.035** | **4.808** | **0.128** |
| **6.XOR** | **4.742** | **0.111** | **4.891** | **0.281** | **4.722** | **0.108** | **4.859** | **0.267** |
| **7.XNOR** | **15.13** | **0.077** | **5.561** | **5.152** | **5.239** | **5.124** | **5.606** | **5.282** |

**7.2.DELAY COMPARISION TABLE OF ADDERS:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Circuit** | **Existing ECRL Logic Delay(ns)** | | | | **Proposed N-P Based ECRL Logic Delay(ns)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12Ff)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **1.HA** | **5.130** | **5.088** | **5.525** | **5.267** | **5.161** | **5.099** | **5.545** | **5.262** |
| **2.FA** | **4.913** | **0.095** | **5.022** | **0.002** | **4.941** | **0.001** | **5.092** | **0.003** |
| **3.RCA** | **4.909** | **0.001** | **5.040** | **0.002** | **4.909** | **0.001** | **5.011** | **0.002** |

**7.3. DELAY COMPARISON TABLE OF MULTIPLIERS:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Circuit** | **Existing ECRL Logic Delay(ns)** | | | | **Proposed N-P Based ECRL Logic Delay(ns)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **1.2X2VM** | **0.004** | **0.003** | **5.056** | **0.004** | **4.934** | **0.003** | **5.079** | **0.005** |
| **2.4X4VM** | **4.949** | **0.008** | **5.084** | **0.009** | **6.202** | **1.079** | **6.616** | **1.245** |

**In section 7.4,7.5 and 7.6** it’s used shortcut terminology for TRI🡪Triangular supply; VDD🡪DC supply; TRI(12fF)🡪triangular supply with 12 femto farad load capacitance; VDD(12fF)🡪 DC supply with 12 femto farad load capacitance;d🡪decreased and i🡪 increased.

**7.4.POWER DISSIPATION TABLE OF BASIC GATES:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Circuit** | **Existing ECRL Logic Power Dissipation(uw)** | | | | **Proposed N-P Based ECRL logic Power Dissipation(uw)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **1.INVERTER** | **0.0123** | **0.462** | **0.097** | **1.475** | **0.011**  **🡺10.57%d** | **0.497**  **🡺7.57%i** | **0.091**  **🡺6.18%d** | **1.489**  **🡺0.94%i** |
| **2.OR-NOR** | **0.0088** | **41.02** | **0.055** | **41.535** | **0.006**  **🡺35.94%d** | **41.03**  **🡺0.02%i** | **0.047**  **🡺14.46%d** | **41.55**  **🡺0.036%i** |
| **3.AND-NAND** | **0.0102** | **0.270** | **0.056** | **0.8219** | **0.0075**  **🡺35.80%d** | **0.289**  **🡺7.03%i** | **0.0496**  **🡺11.428%d** | **0.818**  **🡺0.47%d** |
| **4.XOR-XNOR** | **0.0613** | **0.289** | **0.230** | **33.56** | **0.0789**  **🡺29.34%i** | **32.544**  **🡺0.55%i** | **0.247**  **🡺7.34%i** | **33.70**  **🡺0.41%i** |

**7.5. POWER DISSIPATION TABLE OF ADDERS:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Circuit** | **Existing ECRL Logic Power Dissipation(uw)** | | | | **Proposed N-P Based ECRL Logic Power Dissipation(uw)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **HALF ADDER** | **0.0925** | **32.63** | **0.36** | **30.44** | **0.114**  **🡺23.24%i** | **32.87**  **🡺0.73%i** | **0.38**  **🡺6.11%i** | **34.57**  **🡺13.56%i** |
| **FULL ADDER** | **0.05955** | **32.812** | **0.2359** | **33.97** | **0.061**  **🡺2.43%i** | **33.12**  **🡺0.93%i** | **0.2142**  **🡺9.19%d** | **34.23**  **🡺0.77%i** |
| **RCA** | **0.538** | **33.585** | **0.787** | **38.27** | **0.304**  **🡺43.49%d** | **37.01**  **🡺3.22%i** | **0.787**  **🡺0%** | **39.31**  **🡺2.71%i** |

**7.6. POWER DISSIPATION TABLE OF MULTIPLIERS:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Circuit** | **Existing ECRL Logic Power Dissipation(uw)** | | | | **Proposed N-P ECRL Logic Power Dissipation(uw)** | | | |
|  | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** | **TRI** | **VDD** | **TRI(12fF)** | **VDD(12fF)** |
| **2X2VM** | **0.1318** | **2.171** | **0.315** | **3.257** | **0.121**  **🡺8.19%d** | **2.871**  **🡺13.81%d** | **5.490**  **🡺5.39%d** | **3.948**  **🡺21.21%i** |
| **4X4VM** | **4.49** | **34.77** | **5.49** | **38.27** | **2.861**  **🡺36.28%d** | **4.984**  **🡺85.66%d** | **3.936**  **🡺28.30%d** | **4.984**  **🡺86.97%d** |

**Performance analysis:** The suggested N-P based ECRL logic is compared to existing ecrl logic in four different scenarios: with load capacitor with triangle supply, with load capacitor with VDD supply, without load capacitor with triangular supply, and without load capacitor with VDD supply.The propagation delay (ns) comparison between existing ECRL logic and the proposed N-P based ECRL logic of basic gates, adders, and multipliers is shown in tables 7.1 to 7.3.Similarly, tables 7.4 to 7.6 compares the power dissipation of logic circuits in microwatts.The highest power reduction is 35.80 %, as shown in table 7.4. The bigger power decreases in tables 7.5 and 7.6 are 43.49 %and 86.97%respectively. For a 4x4 vedic multiplier with triangular supply and a 12fF capacitor, power dissipation is decreased by 28.30 %, while propagation delay is increased by 25%. Similarly for Constant VDD Supply with 12fF capacitor 86.97% and without capacitor 85.66% power dissipation reduced and delay is slightly increased to some extent when compared with existing ECRL 4X4 Vedic multiplier.

**8.Conclusions:** In modern world every electronic device demands for two important performance factors they are high speed and low power consumption .We have designed 4X4 Vedic multiplier using N-P based ECRL Adiabatic logic for low power consumption and high speed performance. N-P based ECRL Adiabatic logic reduces power dissipation and ancient Vedic mathematics sutra “Urdhva Tiryagbhyam” helps in improving the computational speed outstandingly. In this paper we have compared all the proposed basic gates, Adders and Multipliers with existing ECRL circuits. Hence the proposed N-P based ECRL adiabatic logic 4X4 Vedic Multiplier has less power consumption when compared with existing ECRL 4X4 Vedic multiplier. Therefore ,Our proposed multiplier is faster, power efficient and requires small area than the existing ECRL and conventional CMOS multipliers. Vedic multiplier is used in Implementation of Faster Real Time Harder Image Processing**,** parallel FIRArchitecture, Asynchronous Digital signal processor core and Image Compression.

**9.Reference papers:**

[1] G. Madan, “A Comparative Study of Power Dissipation of Sequential Circuits for 2N-2N2P , ECRL and PFAL Adiabatic Logic Families,” *Int. J. Res. Sci. Innov.*, vol. IV, no. Xii, pp. 59–63, 2017.

[2] A. Parveen and T. T. Selvi, “Power Efficient Design of Adiabatic Approach for Low Power VLSI Circuits,” *5th Int. Conf. Electr. Energy Syst. ICEES 2019*, no. February, pp. 1–4, 2019, doi: 10.1109/ICEES.2019.8719300.

[3] A. Chaudhuri, M. Saha, M. Bhowmik, S. N. Pradhan, and S. Das, “Implementation of circuit in different adiabatic logic,” *2nd Int. Conf. Electron. Commun. Syst. ICECS 2015*, no. Icecs, pp. 353–359, 2015, doi: 10.1109/ECS.2015.7124923.

[4] M. L. Keote and P. T. Karule, “Design and implementation of energy efficient Adiabatic ECRL and basic gates,” *Int. Conf. Soft Comput. Tech. Implementations, ICSCTI 2015*, no. 3, pp. 87–91, 2016, doi: 10.1109/ICSCTI.2015.7489543.

[5] A. K. Maurya and G. Kumar, “Energy efficient adiabatic logic for low power VLSI applications,” *Proc. - 2011 Int. Conf. Commun. Syst. Netw. Technol. CSNT 2011*, no. 1, pp. 460–463, 2011, doi: 10.1109/CSNT.2011.100.

[6] A. G. Dickinson and J. S. Denker, “Adiabatic dynamic logic,” *Low-Power C. Des.*, vol. 30, no. 3, pp. 268–272, 1998, doi: 10.1109/9780470545058.sect8.

[7] O. R. Anju, A. Anitha, S. Mohan, and R. Deepa, “Design of Ultra Low Power Vedic Multiplier using Adiabatic Logic,” *Int. J. Sci. Res. Eng. Technol.*, vol. 4, no. 3, pp. 136–141, 2015.

[8] S. S. Pandu, A. K. Adibhatla, and M. R. G, “Design of 4-bit ALU using sub-threshold adiabatic logic (SAL),” *Sadhana - Acad. Proc. Eng. Sci.*, vol. 46, no. 3, 2021, doi: 10.1007/s12046-021-01668-3.