Internship Task 1 Report - Arithmetic Logic Unit (ALU)

This report summarizes the design, implementation, and verification of a basic Arithmetic Logic Unit (ALU) as part of the VLSI internship at CODTECH IT SOLUTIONS PVT. LTD.

The ALU supports the following operations:

- Addition
- Subtraction
- AND
- OR
- NOT

Verilog Code:

```
module alu (
    input [3:0] a, b,
    input [2:0] sel,
    output reg [3:0] result
);

always @(*) begin
    case (sel)
        3'b000: result = a + b;   // Addition
        3'b001: result = a - b;   // Subtraction
        3'b010: result = a & b;   // AND
        3'b011: result = a | b;   // OR
        3'b100: result = ~a;      // NOT
        default: result = 4'b0000;
    endcase
end

endmodule
```

Testbench Code:

```
module alu_tb;

reg [3:0] a, b;
reg [2:0] sel;
wire [3:0] result;
```

```
alu uut (
    .a(a),
    .b(b),
    .sel(sel),
    .result(result)
);

initial begin
    $display("Time\ta\tb\tsel\tresult");

    a = 4'b0101; b = 4'b0011; sel = 3'b000; #10;
    $display("%t\t%b\t%b\t%b\t%b", $time, a, b, sel, result);

    sel = 3'b001; #10;
    sel = 3'b010; #10;
    sel = 3'b011; #10;
    sel = 3'b100; #10;

    $stop;
end

endmodule
```

Simulation Tool: ModelSim / Vivado / Xilinx (User Preferred)

The ALU was tested using various inputs to verify all the specified operations. The simulation results matched the expected output in each case.

Sample Simulation Results:

Time	a	b	sel	result	Operation
10	0101	0011	000	1000	ADD (5+3)
20	0101	0011	001	0010	SUB (5-3)
30	0101	0011	010	0001	AND
40	0101	0011	011	0111	OR
50	0101	xxxx	100	1010	NOT (~a)

Conclusion: The ALU design performs all arithmetic and logic operations correctly. The testbench confirms expected behavior through simulation outputs.