Internship Task 2 Report - RAM Design

This report presents the design and simulation of a simple synchronous RAM module as part of Task 2 of the VLSI internship at CODTECH IT SOLUTIONS PVT. LTD.

The objective is to develop a RAM module with basic READ and WRITE functionality using Verilog HDL.

Verilog Code:

```
module simple_ram (
    input clk,
    input we,
    input [1:0] addr,
    input [7:0] din,
    output reg [7:0] dout
);

reg [7:0] mem [3:0];

always @(posedge clk) begin
    if (we)
        mem[addr] <= din;
    else
        dout <= mem[addr];
end

endmodule
```

Testbench Code:

```
module simple_ram_tb;

reg clk, we;
reg [1:0] addr;
reg [7:0] din;
wire [7:0] dout;

simple_ram uut (
    .clk(clk),
    .we(we),
    .addr(addr),
    .din(din),
    .dout(dout)
```

```
);

initial begin
    clk = 0;
    forever #5 clk = ~clk;
end

initial begin
    we = 1;
    addr = 2'b00; din = 8'hAA; #10;
    addr = 2'b01; din = 8'hBB; #10;
    addr = 2'b10; din = 8'hCC; #10;
    addr = 2'b11; din = 8'hDD; #10;

    we = 0;
    addr = 2'b00; #10;
    addr = 2'b01; #10;
    addr = 2'b10; #10;
    addr = 2'b11; #10;

    $stop;
end

endmodule
```

Sample Simulation Results:

Time	WE	Addr	Din	Dout	Operation
10	1	00	AA	--	Write AA
20	1	01	BB	--	Write BB
30	1	10	CC	--	Write CC
40	1	11	DD	--	Write DD
50	0	00	--	AA	Read AA
60	0	01	--	BB	Read BB
70	0	10	--	CC	Read CC
80	0	11	--	DD	Read DD

Conclusion: The synchronous RAM module was successfully implemented using Verilog HDL. The simulation results validate correct read and write operations based on the clock signal. This task helped in understanding memory design and synchronous digital circuit behavior.