DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING

Rajiv Gandhi University of Knowledge Technologies – Nuzvid

Nuzvid, Eluru, Andhra Pradesh – 521202.

Design and Simulation of a 12-bit SAR ADC using Verilog HDL

A Project Progress Report
Submitted in partial fulfillment for the degree of

BACHELOR OF TECHNOLOGY
in
ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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Under the Esteem Guidance of

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CERTIFICATE OF COMPLETION

This is to certify that the work entitled, **"Design and Simulation of a 12-bit SAR ADC using Verilog HDL"** is the bonafide work of **B. TEJO PRIYA (N200429)** carried out under my guidance and supervision for 3rd year **Bachelor of Technology** in the department of Electronics and Communication Engineering under RGUKT IIIT Nuzvid. This work is done during the academic session December 2024 – May 2025, under our guidance.

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CERTIFICATE OF EXAMINATION

This is to certify that the work entitled **"Design and Simulation of a 12-bit SAR ADC using Verilog HDL"** is the bonafide work of **B. TEJO PRIYA (N200429)** and here by accord our approval of it as a study carried out and presented in a manner required for its acceptance in the final year of **Bachelor of Technology** for which it has been submitted. This approval does not necessarily endorse or accept every statement made, opinion expressed or conclusion drawn, as recorded in this thesis. It only signifies the acceptance of this thesis for the purpose for which it has been submitted.

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DECLARATION

B.TEJO PRIYA (N200429) hereby declare that the project report entitled **"Design and Simulation of a 12-bit SAR ADC using Verilog HDL"** done by us under the guidance of **Mr.Sivalal Kethavath** , Assistant Professor is submitted for the partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering during the academic session December 2024 – May 2025 at RGUKT - Nuzvid.

We also declare that this project is a result of our own effort and has not been copied or imitated from any source. Citations from any websites are mentioned in the references. The results embodied in this project report have not been submitted to any other university or institute for the award of any degree or diploma.

Date: 6-05-2025
Place: Nuzvid

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ABSTRACT

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) are widely used in modern electronic systems due to their favorable balance between power efficiency, resolution, speed, and design simplicity. Unlike other ADC architectures, SAR ADCs offer the advantage of a simple structure, lower power consumption, and compact area, making them highly suitable for embedded systems, biomedical instrumentation, IoT devices, and battery-powered applications. These features make SAR ADCs an active area of research and industrial development, particularly in the pursuit of higher resolution and energy-efficient digital conversion.

This project focuses on the design, modeling, and simulation of a 12-bit SAR ADC using Verilog Hardware Description Language (HDL). The entire architecture was developed and tested using the Xilinx Vivado Design Suite, enabling both behavioral simulation and synthesis. The SAR ADC operates on the principle of binary search, where each bit of the digital output is determined sequentially through comparison between the input analog voltage and the DAC output controlled by the SAR logic.

The main components of the design include the sample-and-hold circuit (idealized in simulation), the comparator, the DAC (implemented digitally for simulation purposes), and the SAR logic. The Verilog modules were hierarchically developed and functionally verified using a testbench to mimic analog input conditions. The testbench generates a set of predefined analog voltage levels, which are converted by the SAR ADC into 12-bit digital equivalents.

Simulation results confirm that the SAR ADC performs accurate and efficient conversion with low latency. Waveform analysis from the Vivado simulation environment verifies the proper functioning of the SAR control logic, bit-by-bit comparison, and final digital output generation. This work demonstrates the feasibility of implementing SAR ADCs in digital environments and provides a foundational step towards ASIC or FPGA-based prototyping.

Future enhancements may include implementing a real DAC interface, power and area optimization, and integrating the design into larger signal processing systems. Overall, this project provides a comprehensive understanding of SAR ADC operation and its digital realization using modern EDA tools.

CHAPTER 1 INTRODUCTION

1.1 Background and Context of the Project

As embedded systems evolve to handle more real-world data, the demand for efficient analog-to-digital conversion continues to grow. From biomedical monitoring to industrial automation, a wide range of applications rely on accurate digital representations of analog signals. Among the various types of ADC architectures, SAR ADCs have emerged as a practical solution for medium-speed and medium-resolution needs due to their minimal power consumption and architectural simplicity. With growing emphasis on power-aware design in battery-operated and portable devices, SAR ADCs are now integral to low-power data acquisition systems.

The motivation behind this project stems from the need to understand and implement such a critical building block of modern electronics through a digital design perspective. By using Verilog HDL to model the behavior of a 12-bit SAR ADC, the project aims to bridge the gap between theoretical operation and practical realization within FPGA design flows. Leveraging tools like Xilinx Vivado not only provides simulation support but also opens possibilities for hardware deployment and integration into more complex signal processing chains in the future.

1.2 Objectives and Goals of the Project

Objectives:

- To study the working principle of Successive Approximation Register (SAR) ADCs and understand their significance in real-world applications.
- To design a 12-bit SAR ADC architecture using Verilog HDL, simulating its behavior in a purely digital environment.
- To develop a testbench to verify functional correctness across various input scenarios using Xilinx Vivado.
- To implement the SAR logic that performs bitwise comparisons and resolves digital outputs based on a binary search algorithm.
- To represent analog input values as digital equivalents for the purpose of simulation and verification

Overall Goal:

To design and simulate a 12-bit SAR ADC using Verilog HDL that performs accurate analog-to-digital conversion through a successive approximation algorithm. It aims to verify the functionality of the design using waveform analysis in Xilinx Vivado and demonstrate its suitability for digital integration in low-power embedded systems.

1.3 Literature Review

Analog-to-Digital Converters (ADCs) have been extensively studied due to their crucial role in interfacing the analog world with digital systems. Among various ADC architectures, SAR ADCs have been favored for their moderate speed, low power, and minimal area, making them a popular choice in embedded systems and portable applications. Jan M. Rabaey's *Digital Integrated Circuits* emphasizes the role of digital design techniques in optimizing such mixed-signal blocks, including the SAR logic and comparator interfaces, especially under area and power constraints.

Recent advancements in SAR ADCs include techniques like calibration, capacitor mismatch correction, and asynchronous logic control to improve resolution and reduce power. A notable work by Deming Wang et al. on a 12-bit SAR ADC with calibration demonstrates how dynamic comparator optimization and digital correction can significantly enhance performance in CMOS technology. Their approach highlights the growing importance of digital calibration in extending SAR ADC resolution beyond 10 bits.

In terms of implementation, digital design and simulation using Verilog HDL has become a standard practice in prototyping ADC control logic. Tools such as the Xilinx Vivado Design Suite allow behavioral modeling, verification, and potential hardware deployment, supporting rapid testing and iteration. The reviewed literature collectively points to SAR ADCs as a scalable and efficient solution for medium-resolution applications, especially when designed with digitally controlled logic and validated through simulation platforms like Vivado.

1.4 Limitations

While the designed SAR ADC demonstrates accurate functionality in simulation, there are several limitations associated with this implementation:

- **Lack of Real Analog Interface**: The project simulates analog input (vin) using a digital representation, which does not reflect real-world analog behavior such as noise, offset, or drift.
- **Not Hardware-Validated**: The design is verified only in the simulation domain; it has not been implemented on an actual FPGA or ASIC to confirm its behavior under physical constraints.

CHAPTER 2 METHODOLOGY

2.1 Methodology

This project follows a structured approach to design and simulate a 12-bit SAR ADC using Verilog HDL. The entire methodology is divided into several stages: architecture design, HDL implementation, testbench development, simulation, and verification using Xilinx Vivado.

SAR ADC Architecture Design:

The SAR ADC was modeled using a digital approximation of its core components: the SAR logic, comparator, and DAC. The binary search algorithm was implemented in the SAR logic to set and clear bits based on comparisons. In this simulation-oriented design, the analog behavior was approximated by treating vin as a 12-bit digital input that represents a sampled analog voltage.

Verilog HDL Implementation:

The ADC was implemented in Verilog with a focus on register-based logic. Key modules include:

SAR Logic: Sequential logic to perform bit-by-bit comparison from MSB to LSB.

Comparator Logic: Implemented through conditional statements within the SAR block to simulate comparison between vin and trial values.

Control Logic: Manages the bit index, conversion cycles, and asserts the done signal once conversion is complete.

A top-level module (saradc.v) takes clock, reset, and 12-bit vin as inputs and generates a 12-bit dout output along with a done signal indicating conversion completion.

Testbench Design and Simulation

A testbench module (tb_sar_adc.v) was developed to validate the design. It initializes the clock and reset, provides various input values for vin, and monitors the output dout. The clock toggles every 5 ns, simulating a 100 MHz clock frequency. After resetting the system, a known digital value representing an analog voltage (e.g., 12'h055) is applied and the ADC's output is observed.

Simulation and Verification

Using Xilinx Vivado, both the design and testbench were compiled and simulated. Waveform analysis was performed to trace the bit-by-bit operation of the SAR logic and verify the final digital output. A schematic view was also generated after elaboration to visualize the top-level connections.

This methodology ensures a clean and verifiable design process that models the functionality of a SAR ADC within a digital simulation framework.

2.2 Workflow of the system

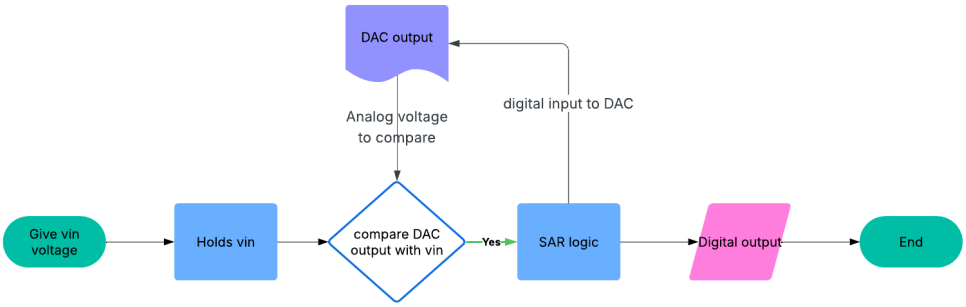


Fig 2.2 -Workflow of the system

2.2.1 Working Principle:

The **Successive Approximation Register (SAR) ADC** works by successively approximating the value of an analog input signal to a digital value. It uses a **binary search** technique to determine the digital equivalent of the input signal. Here's how it works step by step:

1. Input Signal Sampling:

The analog input signal (Vin) is first connected to the Sample-and-Hold Circuit (S/H), which captures and holds the analog signal at a constant value during the conversion process. This ensures that the ADC works with a steady voltage rather than fluctuating with time.

2. Initialization:

The SAR ADC is initialized, where the **successive approximation register** (SAR) starts with the **most significant bit (MSB)**. The resolution of the ADC (e.g., 4 bits, 8 bits, or 12 bits) determines the number of iterations required to complete the conversion.

3. Successive Approximation Process:

The conversion process begins by approximating the input voltage in successive steps, starting with the MSB and moving to the least significant bit (LSB):

Step 1: Set the MSB to 1.

- The SAR sets the first bit (MSB) of the output to 1.
- The value of the reference DAC (Digital-to-Analog Converter) is now generated, corresponding to this initial approximation (e.g., ½ of the reference voltage if the MSB is 1 in a 4-bit ADC).

Step 2: Compare with the input signal**.**

- The **Comparator** compares the DAC output (generated by the SAR) with the input signal (Vin).
- If the DAC voltage is greater than the input signal, the MSB is set to 0; if the DAC voltage is less than the input signal, the MSB remains 1.

Step 3: Move to the next bit (next lower significance).

- The SAR shifts to the next bit and repeats the process:
  - Set the next bit to 1 and compare the DAC output with the input signal.
  - Adjust the bit to 0 or 1 based on whether the DAC voltage is greater than or less than the input signal.

Step 4: Repeat for all bits (until LSB).

- The process continues for each subsequent bit, narrowing the range for the input signal's digital equivalent with each iteration.

4. Digital Output:

After all bits have been processed, the output of the SAR register contains the **final digital representation** of the input signal.

The number of bits in the digital output corresponds to the resolution of the ADC (e.g., a 4-bit ADC produces a 4-bit binary number).

5. End of Conversion:

- The SAR ADC outputs the digital equivalent of the input signal at the end of the conversion. The process is complete, and the digital value can be read from the output register.

2.2.2 System Requirements

Hardware Requirement

- Windows 10
- 8 GB RAM

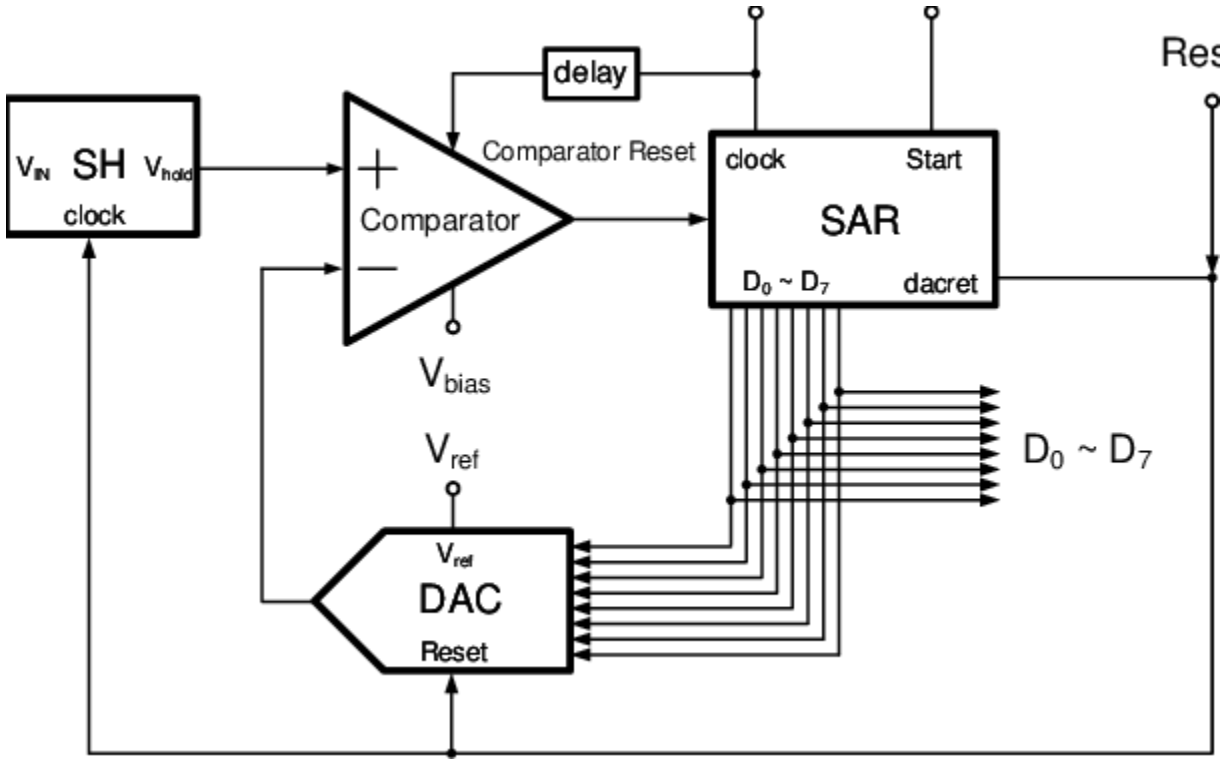
Software Requirement

- Xilinx Vivado

Description Language

- Verilog

Circuit Diagram:



CHAPTER 3 IMPLEMENTATION

3.1 Verilog Implementation:

The SAR ADC was modeled using Verilog HDL. Key components such as the SAR logic and bitwise comparison were implemented.

The design follows:

1. Start conversion by initializing the Most Significant Bit (MSB).

2. Iteratively compare and set bits from MSB to Least Significant Bit (LSB).

3. Complete the conversion after 12 cycles.

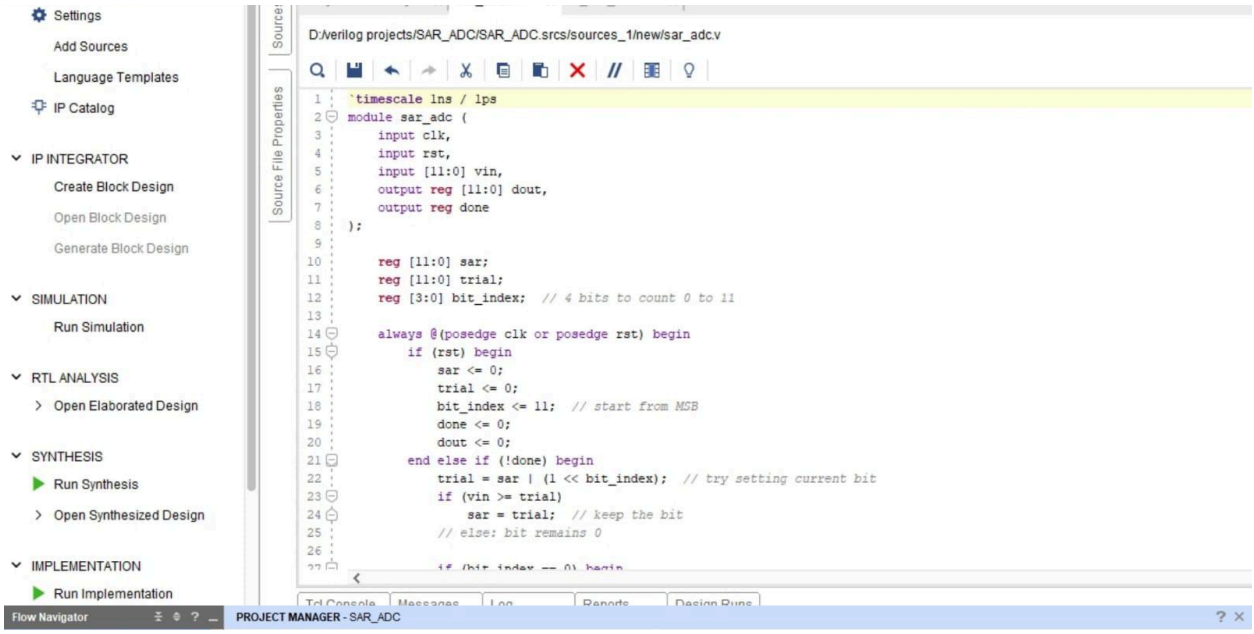


Fig.3.1. Verilog module of SAR ADC

This ”saradc.v” module explains majorly: ”timescale 1ns/1ps” sets simulation time units for better accuracy during testing. The module sar_adc takes a clock, a reset, and a 12-bit analog input vin, and outputs a 12-bit digital result dout along with a done signal. Internal registers sar and trial store the current approximation and the trial value during the conversion. bitindex controls which bit (starting from MSB) is currently being tested and approximated. On every

clock edge (or reset), the SAR algorithm runs: it tries to set a bit high (trial), checks if vin is still larger or equal, and either keeps or clears the bit. The loop continues, moving bit-by-bit from MSB to LSB, until all bits are decided. When the last bit is processed (bitindex equal 0), the final result is stored in dout and done is set high. Overall, this is a simple sequential SAR logic using pure register operations without an explicit comparator module (comparison is done inside the if statement).

3.2 Testbench Implementation:

A Verilog testbench was developed to simulate the ADC functionality. It provided input voltages ('vin') ranging from low to high and verified the output ('dout') against expected values. The simulation used a 100 MHz clock. module

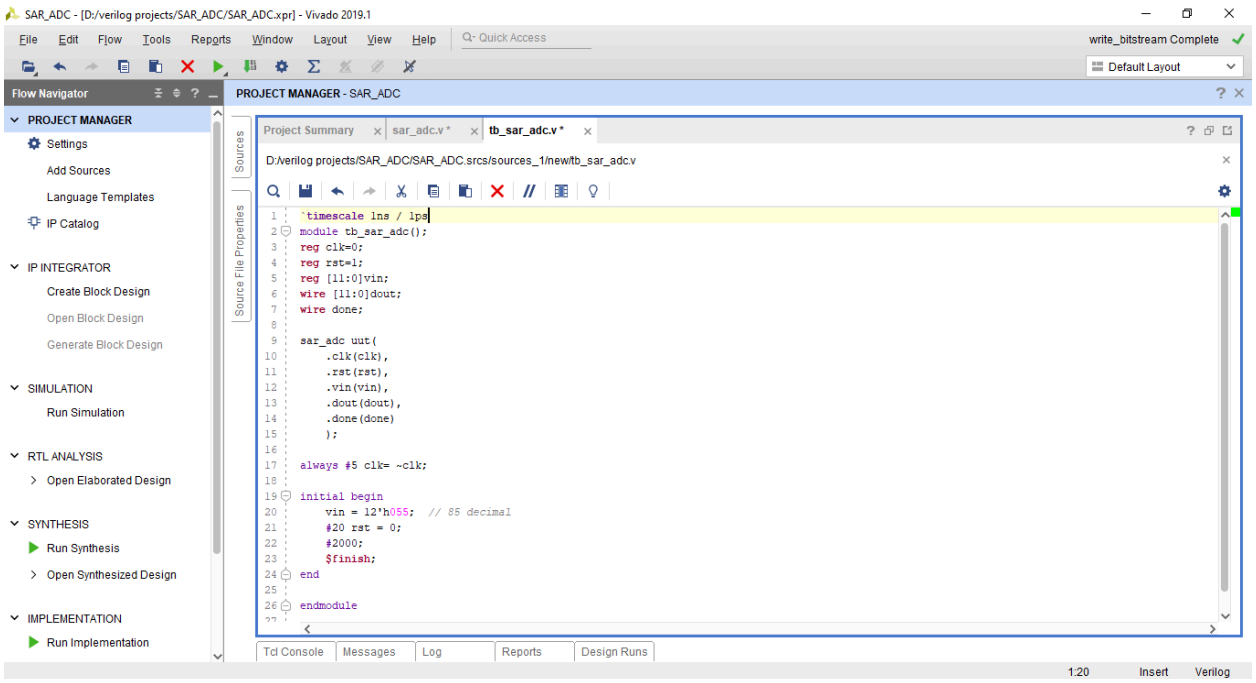


Fig.3.2. Testbench code of SAR ADC

The tb-sar-adc(); defines a testbench to verify the SAR ADC module functionality with no inputs/outputs needed here. reg clk = 0; initializes the clock signal to 0; clk =not(clk); toggles the clock every 5 ns, giving a 10 ns period (100 MHz clock). reg rst = 1; keeps the ADC in reset initially so that it starts cleanly. An instance of the saradc module (uut) is created, connecting testbench signals to module ports. Inside initial begin, vin is set to 12'h055 (which is 85 in decimal) — this is the analog input to be converted. After 20 time units, rst is deasserted (rst = 0), allowing the SAR ADC to begin its bit-by-bit approximation algorithm. The SAR ADC now starts approximating the input value (85) across clock cycles, one bit at a time, starting from MSB After some time (2000 units), simulation ends using finish keyword.

CHAPTER 4 RESULT

4.1 Waveforms:

After creating the xilinx project with these two verilog modules, run the simulation and we get some waveforms to verify the working of this SAR ADC.

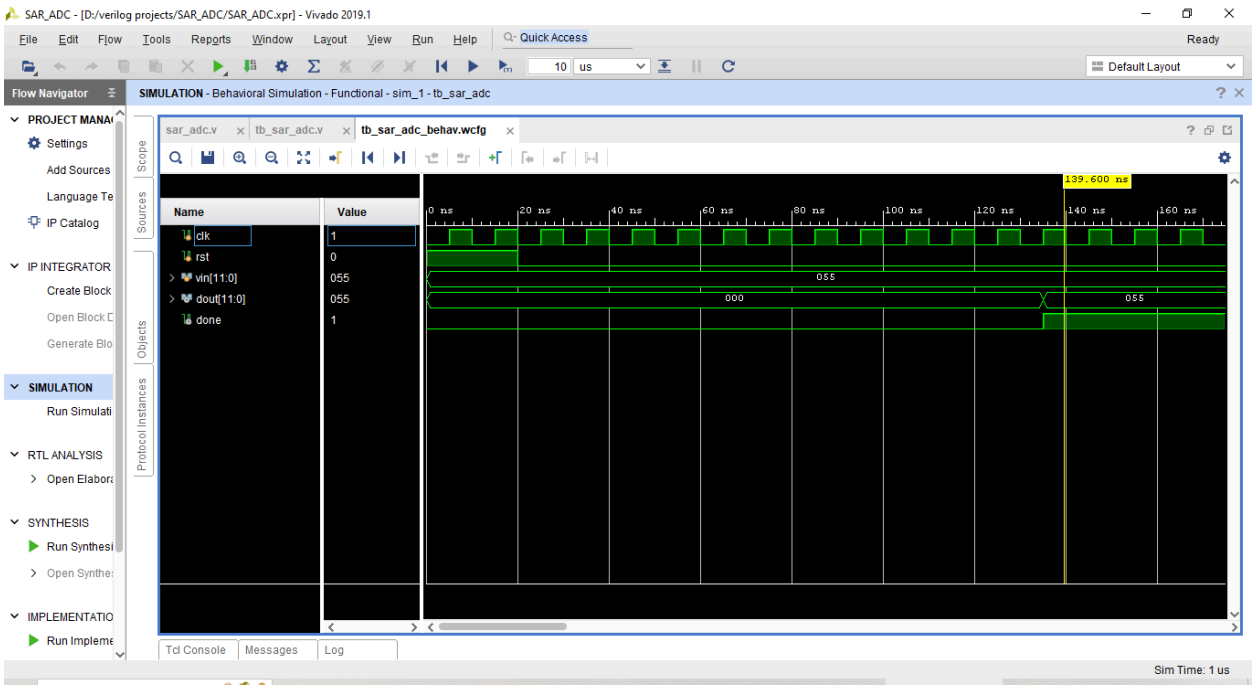


Fig.4.1. Waveforms of SAR ADC

The simulation results verify the SAR ADC functionality. For an input voltage (’vin’) of 85 (decimal), the ADC produced an accurate digital output (’dout’) of 85 after 12 clock cycles. The ’done’ signal was asserted, indicating the completion of the conversion

4.2 Schematic:

After analyzing all the waveforms, open elaborated design where you can see a schematic with a module having inputs clock,reset,vin,and outputs dout and done

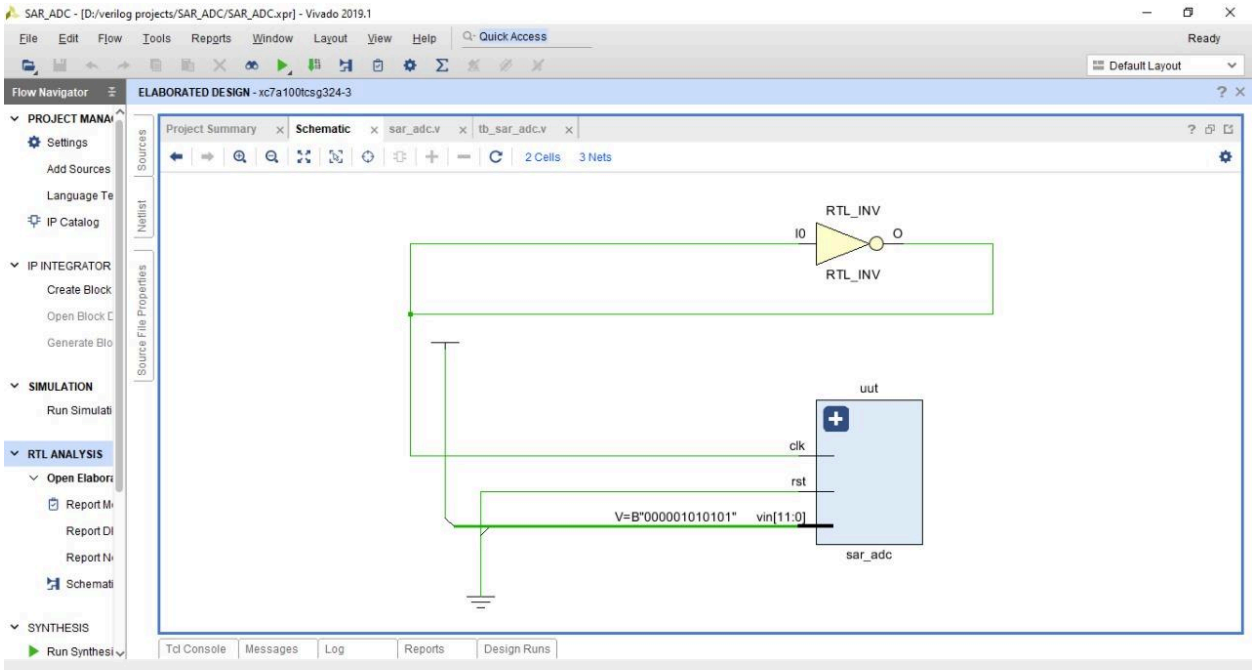


Fig.4.2. Schematic of SAR ADC

CHAPTER 5 CONCLUSION

5.1.Summary

In this project, a 12-bit Successive Approximation Register (SAR) ADC was successfully designed and simulated using Verilog HDL on the Xilinx Vivado platform. The modular approach—consisting of the SAR logic, comparator, and DAC model—helped in understanding the internal architecture and step-by-step conversion process of the SAR ADC.

Through functional simulation and waveform analysis, the correctness of the SAR algorithm was verified. Each bit decision, from MSB to LSB, was accurately made based on comparator feedback, thereby confirming the proper working of the successive approximation process. The 12-bit resolution provided a fine level of quantization, suitable for many low- to medium-speed signal acquisition applications.

This project not only reinforced the theoretical understanding of ADC architectures but also demonstrated practical digital design skills using hardware description languages and FPGA simulation tools. The design can be extended further for physical implementation stages like synthesis, power analysis, and ASIC layout.

5.2.References

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