9 Challenges to FinFET Process and Device Technology

9.1 INTRODUCTION

In Chapter 1 we discussed Moore's law as the driving force in the microelectronics industry to continue to provide integrated circuits (ICs) with more and more powerful transistors with higher integration density and lower power consumption [1]. However, the continued scaling of transistors in the decananometer regime is constrained by several physical phenomena leading to short-channel effects (SCEs) [2–6]. In order to control SCEs, not only has the device substrate been changed from the bulk silicon to silicon-on-insulator (SOI) [7], but the device structure has also been continuously engineered and transformed from the two-dimensional (2D) planar transistors to three-dimensional (3D) vertical devices [2,3]. Through this technological evolution of transistors, the *fin field-effect transistor* (FinFET) has been adopted to high volume manufacturing as the alternative to 2D planar complementary metal-oxide-semiconductor (CMOS) technology due to its excellent short-channel immunity [2–4,8]. As presented in Chapter 4, the FinFET is a complex 3D device with complex fabrication technology. Therefore, the implementation of such 3D devices in the manufacturing of very large scale integrated (VLSI) circuits requires innovative efforts in process architecture as well as the integration of new materials required for the fabrication processes. Thus, many new challenges have emerged during the transition from the 2D to 3D device manufacturing technology. There are several published reports on the challenges and difficulties of FinFET process technology for VLSI manufacturing [9,10]. In this chapter, a brief overview of the challenges of the FinFET process and device technology is presented.

9.2 PROCESS TECHNOLOGY CHALLENGES

9.2.1 Lithography Challenges

The patterning of fins, as described in Section 4.3.3, poses an enormous challenge in the fabrication of FinFET devices. A state-of-the-art lithography is required to create sharp fin patterns. Thus, for the fabrication of 20 nm and 14 nm node devices, the most developed technique used is the 193 nm ArF immersion lithography with multiple-patterning [11]. And, in 7 nm technology node, the 193 nm ArF immersion lithography with *self-aligned double patterning* (SADP) and *self-aligned quadruple patterning* (SAQP) techniques are required [12]. SADP, as discussed in Section 4.3.3, is a technique that applies a spacer transfer process for small pitch, whereas SAQP is

a technique where the SADP is used twice to create the extremely narrow shapes and lines. There are different challenges with multiple-patterning such as edge placement error, pitch walking, and high cost [13]. Therefore, for 7 nm node, *extreme ultraviolet* (EUV) lithography and 193 nm immersion lithography along with multiple-patterning are very promising. The benefit of implementing such an expensive EUV lithography technique is to replace some of the most complex multiple-patterning layers. However, it is expected that ArF immersion lithography will continue to be used for some of the other critical layers in the 10 nm and 7 nm nodes [9].

9.2.1.1 ArF Lithography with Multi-Patterning

Overlay: The overlay accuracy in multiple-patterning lithography for 10 nm and 7 nm technology nodes is challenging. In order to drive the allowed overlay error down to extreme low values, high order overlay correction schemes are required to control the process variability [9]. Furthermore, the increase in the number of split layers increases the complexity of metrology in the total overlay and alignment tree exponentially while increasing the hard-mask steps in the process stack. As a result, the set-up and the verification of overlay metrology recipe becomes more critical and a holistic approach that addresses the total overlay optimization from process design to process setup is required for volume manufacturing [9]. Therefore, overlay accuracy must be improved in metrology, wafer processing, and masking steps for precision wafer patterning [9].

Mask with reticle enhancement techniques (RETs): For tall and narrow FinFET devices, the mask making is challenging. In order to deal with the diffraction issues, various RETs with optical proximity corrections (OPCs) are used to modify the mask patterns and improve the printability on the wafer. Advanced OPCs such as inverse lithography techniques (ILTs) or shapes approaching ILT are required to resolve the target process window in nanometer node technology with increasing structural complexity. Thus, the mask shapes are complex as they require finer geometries and spacing [9].

9.2.1.2 Extreme Ultraviolet Lithography

The extreme ultraviolet or EUV lithography offers the usage of only a single mask exposure instead of multiple exposures. However, there are three major challenges to implement EUV lithography for volume manufacturing of FinFET device technology: *power source*, *resists*, and *mask infrastructure* [9].

The major challenge in implementing EUV lithography for mass production is the source of light for 13.5 nm wavelength that enables cost-effective production capacity of the exposure tool. Though the source issue is considerably matured and several tools are available for the required power at the wafer-level, it is still inadequate for large-scale manufacturing of VLSI circuits.

Another critical technical challenge of EUV lithography is the development of resist material with high resolution and high sensitivity as well as low line-edge roughness (LER) and low outgassing simultaneously [14,15]. In addition, to improve throughput in high volume manufacturing, the resist sensitivity to the 13.5 nm wavelength radiation of EUV needs to be improved, while the line-width roughness (LWR) specification must be held at a low single-digit (nm) [16]. Though resist LER

is generally controlled by chemical processes, the replication of the mask pattern roughness and replicated surface roughness or photon noise will still play a significant role as the pattern dimensions continuously shrink [17].

The availability of defect-free reflective mask has been another most critical challenge in EUV lithography for high volume manufacturing [18]. The EUV patterned masks introduce new materials and surfaces that may cause particle adhesion and cleaning [9]. Therefore, a pellicle is needed to protect the mask during the use of EUV scanner to mitigate the risk of particle adhesion. The remaining challenge for EUV mask with pellicle is that the stress from pellicle mounting may cost overlay error.

9.2.2 Process Integration Challenges

As described in Section 4.3.3, the dense fins in FinFETs are patterned by using the SADP technique, followed by oxide filling, planarization, and recessing to pattern the fin active region and form shallow trench isolation (STI). This fin patterning in the overall process sequence (Figure 4.3) causes many challenges in the fabrication of FinFETs [18–22]. These challenges are related to the issues of: (1) *precise and uniform fin patterning*; (2) *3D gate and spacer patterning*; (3) *uniform junction formation in fin*; and (4) *stress engineering.*

9.2.2.1 Precise and Uniform Fin Patterning

We discussed in Chapters 5–8 that the electrical characteristics of FinFETs depend on the fin geometry (thickness, height, and verticality) [22]. On one hand, taller fins are required to achieve higher current that impose severe challenges to FinFET manufacturing. On the other hand, thinner fins are favorable to channel electrostatic control that causes mobility degradation, random discrete doping (RDD) from the source-drain doping gradients, and variation in the off-state leakage current.

For precision fin patterning, the fin etching in the bulk silicon must be controlled by a timing process. In most cases, the fins at the edges of a cluster suffer a higher variability than those in the middle. To achieve uniform fin thickness and height in a cluster, dummy fins are required [23] which are removed at the pitch. As fin pitch shrinks and approaches the overlay limit, fin removal becomes challenging. The fin isolation by STI and anti-punchthrough implant steps are also challenging due to the tighter pitch, difficulty to control STI depth, and doping variation.

Another challenge in fin patterning is the preservation of the structural integrity of fins with a high aspect ratio. The silicon surface of narrow fins appears different than the bulk silicon [24], and excessive silicon loss may occur after the usual wet cleaning step. Also, the oxidation is faster at the corner and at the tip of the fins. Furthermore, the dry etching of fins is more stringent due to the 3D topography. Therefore, a plasma pulsing scheme may be a viable alternative to minimize the silicon loss in fin patterning [22].

9.2.2.2 Gate and Spacer Patterning

The patterning of tall fins increases the process integration complexity of dummy polysilicon gate, spacer, and replacement metal gate. It is difficult to etch the

polysilicon gate with high aspect ratio and precise control of dimensions [22]. The charging and micro-loading in etching lead to variable gate length (L_g). Due to the tall vertical fin dimension, a significant over-etch is required to remove the residual polysilicon on the fin sidewalls as well as to remove the offset spacers on the fin sidewalls for selective epitaxial growth (SEG) of the source-drain regions of FinFETs [24,25]. These over-etchings cause damage to the silicon fins. Therefore, careful optimization of the dry and wet etch process is required to fabricate 3D gates with minimum L_g variation and fin damage.

The replacement metal gate module also poses severe challenges as it requires new steps to enable interaction during the chemical-mechanical planarization (CMP) process for STI as discussed in Section 4.3.8. The control of the gate height is essential in a replacement gate process. If the gate is over-polished, the raised source-drain region is exposed to the polish resulting in external resistance and mobility variation. On the other hand, if the gate is under-polished, the contact taper causes variation of the external resistance and may cause an open-contact yield issue. Therefore, a more precise and controllable CMP process is required for FinFET fabrication [26].

9.2.2.3 Uniform Junction Formation in Fin

Impurity doping is one of the most critical integration challenges for the fabrication of FinFETs [27,28]. The issues of doping challenges include: conformal doping in the source-drain contact and extension regions to ensure uniform carrier conduction in the fin channel; the shadowing from the neighboring fins due to the tight pitch of the fins that limits the beam incidence angles; and damage, accumulation, and annealing in the high aspect ratio fins.

It is challenging to dope impurities uniformly in tall and narrow fins with shrunk pitch using the conventional ion implantation processes [29]. The post-implant amorphization of the silicon fins causes poor re-crystallization during the junction anneal process thereby causing poor dopant activation and defected fins [27]. The implant condition for fin doping can also impact the quality and the selective epitaxial growth rate of the source-drain which in turn may affect the source-drain and contact resistance of the FinFET devices. Thus, innovative doping schemes are required to overcome the doping challenge in FinFETs and achieve uniform doping profiles.

9.2.2.4 Stress Engineering

Stress engineering is also a challenging issue for FinFET fabrication technology. The most effective process to induce stress in source-drain is embedded SiGe (compressive stress for *p*-channel FinFETs), SiC (tensile stress for *n*-channel FinFETs) or stress in trench contact, and in metal gate [30]. The effectiveness of the gate and source-drain stressors depends on the trade-off between reducing the stressor volume and enhancing the stressor proximity to the channel [31]. In order to further increase the stress and enhance the channel mobility, the Ge content in SiGe source-drain can be increased, similar to the fabrication process used in planar CMOS technology [32–35].

The source-drain SEG layers may suffer from several issues including facet formation [36,37], defects, micro-loading, non-uniform strain distribution, surface roughness, and pattern dependency [38–42]. The pattern dependency occurs due to

the variation of packing density and size of the transistor in a chip. The main reason for the pattern dependency of the SEG process is the non-uniform consumption of reactant gas molecules when the exposed silicon area varies in a chip. This problem can be minimized by optimizing the growth parameters and by designing chip layouts such that the exposed silicon is uniformly distributed over the area of the chip to create uniform gas consumption [42]. The uniformity of strain and the control of the defect density in the fin channel region is a huge challenge for FinFET process technology.

9.2.2.5 High-k Dielectric and Metal Gate

The high-*k* dielectric along with metal gate process is used for advanced CMOS technology due to the high dielectric constant and a relatively large bandgap of the high-*k* dielectric [43]. Typically, HfO_2 high-*k* dielectric with high permittivity (a dielectric constant of about 25) and a relatively large bandgap (5.7 eV) is used as the gate dielectric for both the *n*FinFET and *p*FinFET devices (Table 9.1) [9]. In addition, the HfO_2 has high heat of formation, good thermal and chemical stability on silicon, and large barrier height at interfaces with silicon. And, at an operation voltage of 1–1.5 V, the leakage current through HfO_2 dielectric films is several orders of magnitude lower than that through SiO_2 films with the same equivalent oxide thickness (EOT) [35,43]. However, one of the main challenges of HfO_2 integration for sub-22 nm FinFETs is the thermal instability of HfO_2/silicon interface. There is an inevitable SiO_x interlayer between HfO_2 and silicon substrate [43–45], even though the HfO_2/silicon is theoretically found to be thermodynamically stable [46]. Table 9.1 shows the relevant high-*k* HfO_2 dielectric and metal gate technology parameters for 22 nm and 14 nm technology nodes [9]. The table also shows the use of TiAlN and TiN metal gates for *n*FinFETs and *p*FinFETs, respectively.

Table 9.2 summarizes the typical technology parameters of the high-*k* dielectric and metal gate for 22 nm and 14 nm FinFET technology nodes [9]. It is to be noted from Table 9.2 that the thicknesses of the SiO_x interlayer thermal oxide have been reduced significantly from about 1.1 nm in 22 nm node to about 0.6 nm in 14 nm node. On the other hand, the thickness of the high-*k* dielectric increased from about 1.0 nm in 22 nm node to about 1.2 nm in 14 nm node. However, the overall EOT of the gate dielectric is decreased.

In FinFET architecture, the aspect ratio of the replacement gate structure is larger which makes it a huge challenge to fill the trench. Thus, alternative metal gate

TABLE 9.1
Typical Materials for High-*k* Dielectric and Metal Gate for 22 nm and 14 nm FinFET Technology Nodes

Technology nodes	Device structure	High-*k* dielectric		Metal gate	
		*n*FinFET	*p*FinFET	*n*FinFET	*p*FinFET
22 nm	FinFET	HfO_2	HfO_2	TiAlN	TiN
14 nm	FinFET	HfO_2	HfO_2	TiAl	TiN

TABLE 9.2
Typical Technology Parameters of the High-*k* Dielectric and Metal Gate for 22 nm and 14 nm Technology Nodes

Technology nodes	Film thickness (nm)			
	Thermal oxide	High-*k*	TiAl(N)	TiN
22 nm	~1.1	~1.0	~1.2	~1.4
14 nm	~0.6	~1.2	~3.7	*

processing such as atomic layer deposition (ALD) is considered as a solution for the metal gate deposition because of its excellent capability to achieve conformal step coverage [47,48]. However, for the implementation of ALD, the appropriate metal gate materials are required for workfunction engineering of *n*FinFET and *p*FinFET devices as well as good capability of step coverage.

9.2.2.6 Variability Control

Process variability control is more critical and has become increasingly challenging for FinFET devices [49,50]. The electrical variation in FinFET devices is very sensitive to the variations in fin thickness t_{fin} and fin height H_{fin}. The variation in H_{fin} occurs from fin etching, STI deposition, STI CMP, and STI recessing processing steps as described in Chapter 4.

In general, gate etching profile and L_g variation over fin topography are difficult to control. Source-drain epitaxy is a sensitive process over fin topography [51] and the resistance and stress fluctuations occur due to the change in the shape of fins. Furthermore, in the ion implantation process, the defected layers are another source of variability [50]. In a fin with channel doping concentration of 6×10^{17} cm^{-3}, about a third of the variability is due to random discrete doping (RDD) as observed in planar MOSFETs [52]. Although the channel doping can be avoided in FinFETs, RDD from the source-drain doping gradient causes variability for devices with $L_g <$ 10 nm [29,53]. The channel interface and gate stack workfunction variations have a remarkable negative effect on the transistor performance. Double patterning raises concerns about the way in which individual polygons are split across two masks. Since overlay is not scaled as fast as the minimum feature size, the mask-alignment issues introduce a new source of variability in the spacing between the polygons [23].

9.2.2.7 Spatial Challenges

The reduction in contacted gate pitch for sub-22 nm FinFET devices requires a trade-off between gate length L_g, source-drain spacer thickness, and source-drain contact area. A minimum spacer thickness is defined by reliability requirements as well as on the target specification of capacitance between the gate and source-drain electrodes. Narrow source-drain contacts increase the access resistance of the device.

It is well known that the downscaling of device technology degrades the performance of interconnect wiring. At and below 22 nm technology nodes, the interconnect resistance is expected to increase significantly due to the reduction in the wire

cross-section. In addition to a reduction in the wire cross-section, carrier scattering from the boundaries of the individual copper crystal grains and interfaces with barrier layers rapidly increase the interconnect resistivity as well as the resistance of the individual wires. Also, the double patterning causes routing challenges and difficulties in the access to standard cell pins due to the constraints on the interconnect pitch. In sub-22 nm FinFET technology nodes, the interconnect resistance and capacitance (RC) start to dominate the delay. It is challenging to reduce the line via resistance and capacitance and maintain reliability (electromigration (EM)), time-dependent dielectric breakdown (TDDB), bias temperature instability (BTI), and hot carrier injection (HCI)) to acceptable values. In order to achieve low interconnect resistance while maintaining reliability, the metal filling process must be defect-free. However, reducing line resistance requires enough space for actual wiring material, leaving less room for barrier, thus causing degradation in reliability. Furthermore, to achieve lower via resistance, a thinner barrier at the bottom of the via is required which causes the EM blocking boundary to be insufficient [54]. Thus, there are significant challenges for FinFET process integration and innovative engineering solutions are needed to overcome them.

9.2.3 Dopant Implantation Challenges

The challenges in the FinFET device fabrication process include conformal doping of source-drain areas and lowering fin damage due to ion implantation [55].

9.2.3.1 Conformal Doping

For FinFETs, the major challenge is the conformal distribution of dopants within the fins irrespective of the source-drain extension (SDE) dopant activation, diffusion, and profile abruptness [55–57]. The non-conformal doping profile causes degradation in the drive current of FinFETs. The conformal distribution of dopants can be achieved by a large tilt beamline implantation. However, the shadowing by the neighboring fins limits the conformal doping. An alternative technique to achieve conformal distribution of dopants within the fin is plasma doping with optimized process parameters.

9.2.3.2 Damage Control

In FinFETs, the damage control during doping is another challenge to achieve the target performance of the devices. In FinFET structure, a narrow fin on the pedestal of the well is isolated from large crystal volume. Thus, the surface proximity and 3D structure pose a severe constraint on the recrystallization of post-implant amorphous silicon fin. In the case of a complete amorphization of silicon fins, only a very small seed for recrystallization can cause a defective growth, causing degradation in the resistivity and drive current of the devices [58,59]. Therefore, in FinFET fabrication it is critical to reduce the amorphization depth created by ion implantation and annealing to minimize the fin damage. In order to achieve damage-free SDE fin doping, hot implantation can be used. Using high temperature implantation, damage accumulation can be significantly reduced, thus decreasing the self-amorphization of the implant. The hot implant technique also improves the fin line conductance and junction leakage [60].

9.2.4 The Etching Challenges

9.2.4.1 Depth Loading Control of Fin Etching

During the fin etch (Section 4.3.3), only a small part of the process gases is *ionized* into plasma under the radio frequency power. Most of the gas molecules exist in the chamber as *neutrals* which induce deposition during the etching process. The neutral molecules are easy to stick onto the surfaces before entering at the bottom of the trench, inducing taper profile (Chapter 4) that blocks ions from reaching the bottom [9]. On the other side, new stored ions are formed at trench bottom to react upon the incoming ions. As a result, as the etching reaction continues and etching depth increases, the flux ratio of ion and neutral molecules decreases and etching bombardment is weakened [9]. Within the critical dimension (CD) sizes, the smaller CD induces weaker bottom reaction. Therefore, the etching depth depends on the opening CD size: bigger size induces deeper depth. The CD dependence of etching depth can be improved using the bias-pulsing technique [9]. The bias-pulsing etching process can be used to achieve a smaller depth loading effect that is caused by different opening CD size [61,62].

9.2.4.2 Gate Etch Control

The selective and residue-free etch processes are challenging in FinFET device fabrication. There are a few new process and materials challenges in FinFET fabrication as summarized below. First of all, an excessive Si loss is observed after the usual pre-gate-oxide clean as discussed in Chapter 4. Therefore, wet cleaning must be optimized with dilute concentration and lower temperatures. Secondly, the oxidation of fins is also faster at the corner and tip of the fins. And, the dry etching on fins is more stringent due to the 3D structures, and a plasma bias-pulsing scheme may be a viable alternative for minimizing silicon loss [63,64]. The gate etch control is critical to maintaining uniform fin height H_{fin}. The variation in H_{fin} impacts the electrical properties of FinFETs such as the threshold voltage V_{th}. This indicates that the (dry or wet) etching step is crucial for 3D transistors compared to the planar ones.

In addition, controlling the selectivity of self-aligned etching (Section 4.3.3) is challenging for FinFETs of gate length below 14 nm [65] to enable appropriate contact slit opening for local transistor contacts.

9.2.4.3 STI Process for Gate

As discussed in Section 4.3.3, the fin height is defined by etching STI oxide (TEOS). It is one of the critical processes to control the fin height H_{fin}. The oxide is etched back using a highly selective etch process and it is challenging to have full control to form a silicon fin with defined dimensions. Thus, it is especially critical to define H_{fin} by etching STI oxide. The variation in H_{fin} severely impacts the electrical properties of transistors such as the threshold voltage V_{th}. This indicates that an appropriate etching step must be used for STI recess to define H_{fin}.

9.2.4.4 Gate Process

In Section 4.3.8, we described the replacement metal gate (RMG) process by removing the polysilicon dummy gate and SiO_2 dummy gate oxide with the wet process [66–69].

The RMG process is complicated and challenging as described in Chapter 4. Typically, due to the chemical nature of the HF-based wet etchant, the dummy gate oxide etching process cannot remove the polysilicon without any oxidizer [70–72]. However, it is critical to completely remove the polysilicon dummy gate without leaving any residues in the narrow and steep trenches [67–69]. The residues occupy the space of the intended location of the high-*k* and metal gates and may cause device failure.

Typically, the wet processes use aqueous solutions using water as the solvent and the final rinses using deionized water or ultra-pure water to clean away the chemicals from the surface of the wafers. However, it is well known that some defects can be generated due to the surface tension of water. During the drying process, the high capillary force of water could pull nearby structures to form permanent defects, so-called pattern collapse [73] or stiction [74]. In order to eliminate pattern collapse, gas phase etching such as the HF vapor process can be used where the intermolecular force is not too strong compared to the liquid phase.

In FinFET-like vertical structures, "new materials" including multilayers of SiGe/Si are used. Since it is needed to selectively etch either silicon or SiGe layers, a lot of effort is made to use $HF:H_2O_2:CH_3COOH$ mixtures to etch SiGe selectively to Si [75–77] or to use tetra-methyl-ammonium hydroxide (TMAH) based to remove silicon from SiGe [78].

9.3 DEVICE TECHNOLOGY CHALLENGES

9.3.1 Multiple Threshold Voltage Devices

Threshold voltage V_{th} control and multiple-V_{th} device options of a manufacturing CMOS technology are important for analog applications. A typical planar CMOS technology at a node offers different options for V_{th} including low-V_{th} for high performance VLSI circuits, standard-V_{th} for logic design, and high-V_{th} for analog and radio frequency (RF) applications. This V_{th} control of a planar-MOSFET device can be defined from the expression [3] given by

$$V_{th} = V_{fb} + 2\phi_B + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}\left(2\phi_B + V_{bs}\right)N_b} \tag{9.1}$$

where:

V_{fb} is the flat band voltage
ϕ_B is the bulk potential
C_{ox} is the gate capacitance = ε_{ox}/T_{ox}; ε_{ox} being the permittivity of gate dielectric
V_{bs} is the body bias
N_b is the channel doping concentration

Equation 9.1 shows that V_{th} depends on T_{ox}, N_b, and V_{bs}. Thus, multiple-V_{th} devices of a planar CMOS technology node can be achieved by changing the substrate doping concentration N_b and/or by gate dielectric thickness T_{ox}. In addition, V_{bs} can be used to modulate V_{th} of a MOSFET device.

For multigate FinFET devices, the body is generally undoped or lightly doped. It is also difficult to implement multiple dielectric thicknesses in 3D structures due to lithography and etching challenges. Therefore, it is difficult to achieve multiple-V_{th} FinFET devices in a non-planar CMOS technology using the conventional fabrication process. In order to analyze the options for multiple-V_{th} FinFET devices in a technology node, let us derive a first order expression for V_{th} of FinFET devices from Equation 3.30 given by

$$V_{gs} = V_{fb} + \phi_s - V_{ch}(y) - \frac{Q_s}{C_{ox}} \tag{9.2}$$

where:

V_{gs} is the gate voltage
ϕ_s is the surface potential
$V_{ch}(y)$ is the channel potential due to applied drain bias V_{ds}
Q_s is the total charge density in the silicon fin channel

Now, for metal gate FinFET devices, V_{fb} is given by Equation 3.21 as

$$V_{fb} = \Phi_{ms} - \frac{Q_0}{C_{ox}} \tag{9.3}$$

where:

Φ_{ms} (= $\Phi_m - \Phi_s$) is the difference between the metal gate electrode workfunction (Φ_m) and bulk-silicon workfunction (Φ_s)
Q_0 is the oxide charge at the Si/gate oxide interface and ≈ 0 for ideal defect-free oxide

Again, if Q_i and Q_b are the inversion and bulk charges, respectively, then $Q_s = Q_i + Q_b$. Since at the subthreshold region $Q_i << Q_b$, we have $Q_s \cong Q_b$. Also, since at threshold condition, the drain voltage V_{ds} and hence $V_{ch}(y)$ is negligibly small, therefore from Equations 9.2 and 9.3 we can express V_{th} of FinFET devices as

$$V_{th} \approx \Phi_m - \Phi_s + 2\phi_B + \left(\frac{qN_b t_{fin}}{C_{ox}}\right) H_{fin} \tag{9.4}$$

where:

t_{fin} is the fin thickness
H_{fin} is the fin height

Thus, from Equation 9.4, we observe that there are several possible *options* for multiple-V_{th} FinFET devices in a non-planar CMOS technology. First of all, by changing C_{ox} using multiple oxide thickness and patterning multiple fin height H_{fin} (that is, taller fins to achieve higher-V_{th} devices). However, as described in Chapter 4, achieving multiple T_{ox} is challenging in complex FinFET fabrication technology. Also, since fins are patterned by spacer defined technology, the various spacer techniques required to patterning multiple height fins on the same substrate is difficult.

Thus, to have full control to form a silicon fin with defined dimensions is a difficult task. It is especially critical to define the fin height by etching the shallow trench isolation oxide. Therefore, it is challenging to achieve multiple-V_{th} devices in FinFET technology using conventional methods. Alternatively, as shown in Equation 9.4, an innovative technique such as metal workfunction Φ_m engineering can be used to achieve multiple-V_{th} FinFETs in non-planar CMOS technology.

In a FinFET technology, with HfO_2 high-k gate dielectric and TiN metal gate, V_{th} control and multiple-V_{th} device technology are achieved by workfunction engineering using aluminum (Al) implantation as described in Chapter 4. In the high-k metal gate process, aluminum ($1 \times 10^{15} - 1 \times 10^{16}$ cm^{-2}) is implanted into TiN metal (not into the high-k) using ultralow energy implanter. The effective workfunction (EWF) of MG is modulated by Al implantation via Al-induced dipole at the HfO_2/SiO_x interface layer. Al diffuses differently in/through TiN depending on its growth method. Since Al-rich TiN has a more n-type effective workfunction, stacks with higher amount of Al diffused into TiN translate into lower EWF values (that is, more n-type EWF). And, TiN (least in Al-rich) is selected for p-type workfunction as shown in Tables 9.1 and 9.2.

9.3.2 Width Quantization

One of the major differences between a FinFET and a planar MOSFET device is the fact that the FinFET device consists of multiple small unit fins of height H_{fin} and fin thickness t_{fin}. As discussed in Chapter 5, the width of a FinFET device is given by

$$W = n \times \left(2H_{fin} + t_{fin}\right) \tag{9.5}$$

where:

n is the number of fins of a device and $n = 1, 2, 3, \ldots, n$

The factor "2" in H_{fin} is due to two sidewall gates

Equation 9.5 shows that the width W of a FinFET depends on the integer n, the number of fins used to build a device and thus quantized. This is referred to as the "width quantization." This unique *width quantization* property of FinFETs is due to the constraint in patterning multiple height FinFETs at a technology node [79]. Due to the technology complexities, only fins of constant height are patterned by lithography techniques as discussed in Chapter 4. Thus, a large device is designed using multiple unit fins. As a result, the larger devices with multiple unit fins are susceptible to random V_{th} variation among fins due to RDD within each fin channel and therefore, the effect of dopant fluctuations must be considered on device performance [80].

The width quantization severely impacts the device leakage current distribution due to random V_{th} variation [79]. The width quantization-induced FinFET leakage current can potentially lead to the chip failure due to insufficient noise margin, inaccurate full chip power estimates, and improper guidelines for leakage-sensitive circuits [81]. Also, width quantization is critical for analog application. In analog IC design, W is a circuit design parameter and is a continuous variable. However, due to width quantization, the design parameter W is a set of small positive integers instead

of a continuous variable. Thus, the width quantization poses a severe challenge in FinFET circuit design and therefore, requires width quantization aware FinFET circuit design with advanced statistical modeling techniques for accurate prediction of the leakage current distribution due to width quantized FinFET devices in VLSI circuits [81]. Furthermore, the width quantization increases the complexities and number of layout design rules including spacing rules to reduce coupling, SADP rules for fin patterning, and dummy gate rules for replacement metal gate.

9.3.3 Crystal Orientation

Traditionally, CMOS ICs are fabricated on silicon substrates with a ⟨100⟩ crystalline orientation due to their high electron mobility compared to hole mobility [82–85] as shown in Figure 9.1 and reduced interface trap density. Similar mobility trends are observed for high-*k* gate dielectric as gate oxide as shown in Figure 9.2 [86].

Figure 9.3(a) shows the layout of IC devices at different crystal orientations to optimize electron and hole mobilities. As shown in Figure 9.3(a), the device orientation, (1) *perpendicular* and (4) *parallel* to the wafer flat or notch, the channel surface lies in the ⟨110⟩ plane where the hole mobility is the highest, whereas the electron mobility is the lowest (Figures 9.1 and 9.2). On the other hand, the device orientation, (2) at a 45-degree angle, the channel surface lies in the ⟨100⟩ plane, the hole mobility is the lowest and electron mobility is the highest (Figures 9.1 and 9.2). For any intermediate orientations, such as position (3), the electron and hole mobilities are at intermediate values [86,87].

Figure 9.3(b) shows a FinFET structure standing vertically on the wafer pedestal, hence the fin surface is orientated in the multiple crystal planes. Thus, the orientation of the fins depends on layout. This poses a serious challenge in layout design and fin patterning. In a FinFET, the conducting channel lies on the sidewall of a silicon

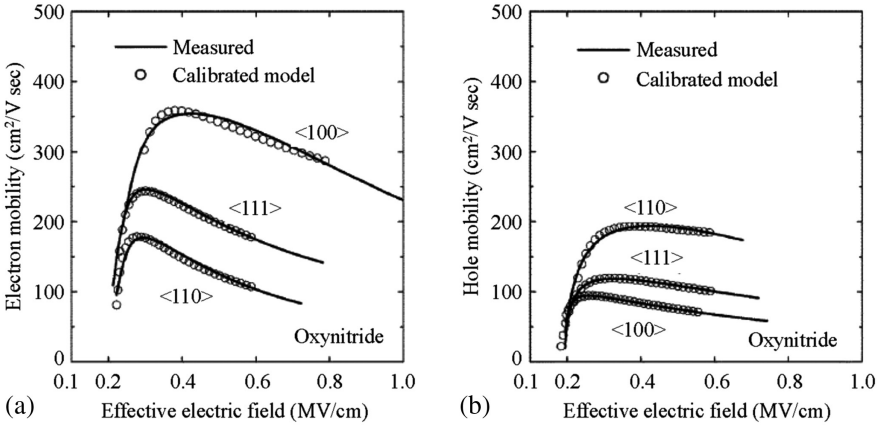

FIGURE 9.1 Carrier mobility for ⟨100⟩, ⟨110⟩, and ⟨111⟩ bulk-silicon crystal surfaces as a function of effective electric field for conventional nitrided oxide: (a) electron mobility; (b) hole mobility [86].

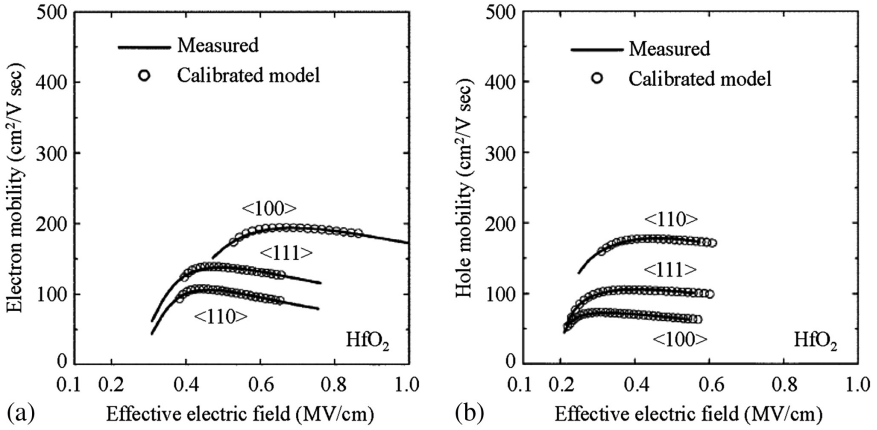

FIGURE 9.2 Carrier mobility for ⟨100⟩, ⟨110⟩, and ⟨111⟩ bulk-silicon crystal surfaces as a function of effective electric field for high-*k* gate dielectric: (a) electron mobility; (b) hole mobility [86].

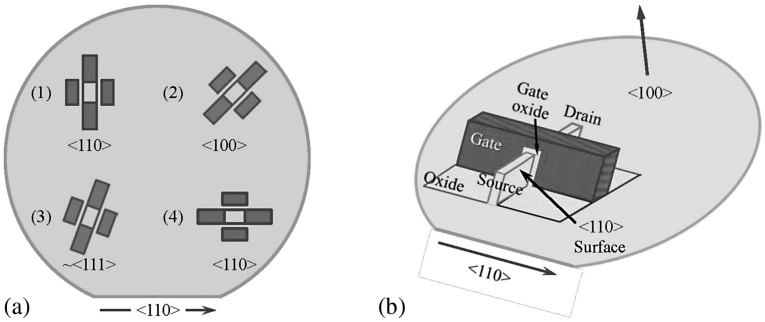

FIGURE 9.3 Device orientation on wafer for mobility optimization: (a) device orientation, (1) perpendicular or (4) parallel to the wafer flat offers highest hole mobility, (2) at a 45-degree angle to the wafer flat offers highest electron mobility, and at any intermediate position, intermediate values of electron and hole mobilities can approximate the ⟨111⟩ plane; (b) FinFET ⟨110⟩ orientation parallel to wafer flat, the electron and hole mobilities are at intermediate values.

pillar (fin channel). Thus, in a standard ⟨100⟩ wafer, where the gate and active fin area are aligned either perpendicular or parallel to the wafer flat, the device channel lies in the ⟨110⟩ plane. However, if the transistor layout is rotated by a 45-degree in the plane of the wafer, then the resulting orientation of the device channel is ⟨100⟩. With an intermediate rotation, the electron and hole mobilities are at intermediate values between ⟨100⟩ and ⟨110⟩ orientations, which can be approximated to ⟨111⟩ surface.

In FinFET layout design, all devices can be drawn at different angles relative to the wafer flat or notch to achieve ⟨100⟩, ⟨110⟩, and ⟨111⟩ orientations and maximize

mobility values for both *n*FinFET and *p*FinFET devices. The optimum mobility scheme to align the channels of *n*FinFET and *p*FinFET to lie in the ⟨100⟩ and ⟨110⟩ planes, respectively, can be achieved by rotating the layout of one of the two device types by a 45-degree angle. Although either the *n*FinFET or *p*FinFET device could be rotated depending on the wafer flat direction, however, the rotation of the *n*FinFET is preferable due to its smaller size. In either case, it is a lithography challenge to define minimum line-widths in both 0- and 45-degree rotations. In addition, under this orientation scheme of ⟨100⟩ for *n*FinFET and ⟨110⟩ for *p*FinFET devices, a 40% area penalty is incurred for small devices due to the area overhead required for implementation of a 45-degree device rotation [86].

Again, compared to the traditional ⟨100⟩ orientation, the wafers with ⟨110⟩ and ⟨111⟩ orientations improve the area efficiency due to reduced requirement for *p*FinFET width and hence the stronger *p*FinFET current drive per unit width. For a ⟨110⟩ wafer substrate, the layout area penalty could be minimized since the FinFET sidewalls of ⟨100⟩ and ⟨110⟩ orientations are at right angles to each other. Then *n*FinFET and *p*FinFET devices can be drawn parallel and perpendicular to ⟨110⟩ wafer flat direction. This may still incur a minor area penalty, but it would be significantly reduced from the orientation scheme in which one device type is rotated by 45 degrees [86].

9.3.4 Source-Drain Series Resistance

One of the challenges of FinFET device technology is achieving low source-drain series resistance. High source-drain resistance of FinFET devices poses a severe challenge to analog design due to the degradation of device conductance. Typically, merged raised source-drain (RSD) regions as shown in Figure 9.4 are used to achieve lower source-drain series resistance. However, the control of the growth of the RSD epitaxial layer can be challenging and may cause an increase in the defect density. Furthermore, stress provided by merged fins for strained-silicon fin channel is more difficult to control than unmerged fins.

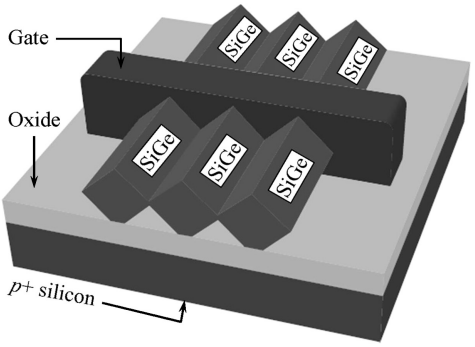

FIGURE 9.4 Merged raised source-drain structure using selective epitaxial growth SiGe layer to reduce the source-drain series resistance.

9.4 CHALLENGES IN FinFET CIRCUIT DESIGN

As the critical dimension of VLSI circuits approaches atomic size near the 3 nm regime, the VLSI circuit designs are becoming increasingly challenging. In designing VLSI circuits using near atomic scale FinFET devices, many issues including high leakage current, low gain, width quantization, and the sensitivity and tolerance of the manufacturing process become extremely critical and must be pre-estimated. With the increasing technical challenges in the circuit design to achieve the CD limit near the 3 nm regime, the circuit design methodologies are continuously evolving to provide novel solutions to address many of these challenges.

9.5 SUMMARY

This chapter presented an overview of the major challenges of the FinFET process, device, and circuit design in manufacturing VLSI circuits and systems. First of all, the lithography challenges such as overlay, pitch walking, and edge placement error, as well as high cost to the currently used 193 nm ArF immersion lithography with SADP and SAQP techniques for 22 nm technology node and beyond are highlighted. Though these issues of the current lithography can be minimized using the EUV lithography technique, it is challenging to implement the EUV lithography technique in high volume manufacturing of FinFETs due to its high cost.

After discussions on lithography challenges, the FinFET process integration challenges related to gate and spacer patterning, patterning of uniform fins, and the SEG SiGe stressor material on raised source-drain regions are overviewed. The SEG layers on FinFETs may cause serial problems including strain relaxation on fins-faceted shape leading to higher defect density and pattern dependency effect due to different transistor architecture and their density in the chip. Then the challenges in the high-k and metal gate processing and thermal instability of HfO_2/silicon interface for the integration of HfO_2 as the gate dielectric for FinFETs are discussed. In addition, the challenge in controlling gate workfunction using Al implant in TiN metal gate is highlighted.

Next, the challenges to fin doping and controlling fin dimensions of FinFETs are overviewed. It is discussed that the conformal doping challenge is due to the shadowing caused by the neighboring fins during ion implant of the fins in an array. The conformal distribution of dopants is required to mitigate the risk of drive current degradation. To overcome the challenges of conformal doping, plasma doping with optimized process parameters can be used. On controlling fin dimensions, it is challenging to define the fin height by etching the STI oxide. The variation in fin height influences electrical properties of transistors such as V_{th}. This indicates that (dry or wet) etching must be controlled in the FinFET fabrication process.

After discussing the process technology challenges, the major device technology challenges such as width quantization, multiple-V_{th} transistors at a technology node, and optimal crystal orientation in FinFET layout design to achieve high mobility for both nFinFETs and pFinFETs are overviewed. The width quantization imposes some challenges on VLSI circuit design, especially for analog applications. Limitation of

V_{th}-tuning or multiple-V_{th} transistors limits the application of FinFETs in analog circuit and mixed-signal applications. The channel orientation, such as ⟨110⟩ sidewall planes for higher hole mobility and ⟨100⟩ sidewall planes for higher electron mobility, poses challenges in layout design. A hybrid orientation scheme might be difficult to implement in practice. Finally, a brief overview of the challenges in circuit design is presented.

Most of the challenges discussed in this chapter are in development or partially solved. However, the most critical issue of achieving atomic scale FinFETs near 3 nm is the significant increase in the manufacturing cost due to the necessity for the implementation of new materials and innovative techniques.

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