VERSALOGIC CORPORATION

VSBC-1
VSBC-2

486 / 5x86 based SBC with
Embedded-PCI™
(PC/104-*Plus*) expansion site.

EMBEDDED PCI

Model VSBC-1 & VSBC-2

486 / 5x86 based SBC with
Embedded-PCI™(PC/104-*Plus*) expansion site.

REFERENCE MANUAL

Doc. Rev. 01/98

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Table of Contents

Other References

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PC/104 Resource Guide

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AM486DX5-133W16BGC Data Book (VSBC-2)

Microsoft Press, (800) 677-7377, http://mspress.microsoft.com
The Programmer's PC Sourcebook

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Overview 1

This chapter introduces the VSBC Single Board Computer, lists its features and specifications, and provides a brief overview of the installation and configuration process. The VSBC-1 features a 100 MHz 486DX CPU and the VSBC-2 features a 133 MHz 5x86 CPU.

Using This Manual

Each chapter in this manual corresponds to a step in the installation process:

Chapter 1 – Overview

Lists basic information about the CPU board, specifications, and system requirements. Use this chapter to familiarize yourself with the bard and it's capabilities.

Chapter 2 – DOS Based Quick Start

Describes how to quickly get your system set up and running. Summarizes how to install the VSBC and how to connect PC/104 and PC/104-*Plus* expansion modules.

Chapter 3 – Configuration

Describes how to jumper the board.

Chapter 4 – External Connections

Provides pinout information on the user connectors.

Chapter 5 – Register Descriptions

Provides details about the user-programmable registers on the CPU card.

Chapter 6 – CIO Chip

Provides operational details about the Zilog Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel I/O chip.

Appendix A – Schematics

Circuit diagrams.

Appendix B – Physical Dimensions

A drawing showing board outline and location of mounting holes.

Introduction

This manual covers operation of the VSBC-1 and the VSBC-2 Single Board Computers.

The **VSBC-1** features a 32-bit, 100 MHz, 486DX4 CPU chip, up to 64MB DRAM, up to 2MB Flash Disk System, two COM ports, one LPT port, IDE hard disk interface, floppy disk interface, and real time clock.

The **VSBC-2** is a faster version of the same board, featuring a 32-bit, 133 MHz, 5x86 CPU chip. This industrially rugged computer has performance similar to a Pentium 75 MHz machine, and does not require a cooling fan.

A full complement of PC type I/O ports is included on each board. Two PCI based IDE interfaces, floppy disk interface, two COM ports, one LPT port, keyboard interface, and the other standard DOS-based I/O are provided. A 16 channel Opto 22 style I/O interface and three additional counter/timers are also included.

I/O expansion is available through the high speed Embedded-PCI (also known as PC/104-*Plus*) expansion site. This plug-in site supports PC/104, PC/104-*Plus*, or Embedded-PCI expansion modules. Several modules can be stacked together for additional expansion.

PC/AT COMPATIBILITY

Standard I/O and peripheral interfaces and optional onboard BIOS firmware, self tests, and a setup utility, bring a full-function PC/AT compatible computer to an industry standard 5.75" x 8" single-board form factor.

PC/104-*PLUS* COMPATIBILITY

I/O expansion is available through the high speed Embedded-PCI expansion site. This plug-in site supports PC/104, PC/104-*Plus*, or Embedded-PCI expansion modules. Several modules can be stacked together for additional expansion.

ON-BOARD MEMORY

DRAM One 72-pin SIMM compatible socket will accept a standard 72-pin DRAM. Modules from 4 to 64 MB, parity or non-parity, standard or EDO type may be used. Application programs and files can be stored on an optional bootable flash disk system. Up to 2 MB of Flash memory is supported.

CMOS RAM Standard setup values are stored in a small battery-backed CMOS RAM chip.

FLASH Four 32-pin PLCC JEDEC compatible sockets accept 512K x 8 Flash EPROMs. You can start out with one device, and add a second one when your storage requirements grow. A Flash Disk System is available to make the Flash device(s) appear as a bootable disk drive.

HARD DISK DRIVE AND FLOPPY DISK DRIVE INTERFACES

A 40-pin IDE hard disk drive interface and a 34-pin floppy disk drive interface are included on the VSBC board for connection to industry standard IDE hard drive(s) and PC/AT style floppy drive(s) (5¼" or 3½"). Each interface supports two drives.

SERIAL PORTS

The two on-board serial ports are hardware and software compatible with 16550 type UARTs with 16 byte FIFOs. Baud rates are programmable from 50 baud to 115K baud. COM1 is a standard RS-232 interface, COM2 can be jumpered for RS-232, RS-422, or RS-485 operation.

PARALLEL PORT

The parallel port can be used as a standard bi-directional/ECP/EPP compatible LPT port or as 17 general purpose TTL I/O signals. When operating in standard bi-directional mode, each output line has a 24 ma current sink rating. Eight of the signals are programmable as a group for input or output, three are dedicated output, and five are dedicated inputs. A strobe signal, which produces a 50 µs pulse under program control, is also available as an output.

COUNTER/TIMERS

The VSBC board features six 16-bit counter/timer channels. Of the three PC standard 8254 type 16-bit counter/timers, one channel provides timing for dynamic RAM refresh, one channel generates an 18.2 ms DOS interrupt, and another channel is used to drive the speaker output. All channels are available for general purpose timing and periodic interrupt sources if they are not being used by an operating system. Three additional 16-bit channels are implemented in the CIO chip (see chapter 6). Control signals for these channels are available on connector J13 and J14.

REAL TIME CLOCK WITH CMOS RAM

A battery-backed 146818 compatible real time clock (RTC) provides accurate date and time functions. This PC/AT compatible RTC also contains 128 bytes of battery-backed CMOS RAM with 114 bytes available as a system resource to store standard DOS setup parameters. Normally, DOS requires 51 bytes, leaving 63 bytes for general purpose use.

INTERRUPT CONTROLLERS

Two PC AT compatible 8259 type programmable interrupt controllers (PICs) are provided for full MS-DOS functionality. Interrupt sources and destinations can be configured with jumper blocks and through CMOS Setup. Interrupt lines connect to on-board sources, PC/104 and PCI Buses, and to a user connector.

DMA CONTROLLERS

The VSBC has two DMA controllers which provide eight DMA channels. One channel is used for floppy disk data transfers, and the remaining channels are available to the PC/104 bus.

WATCHDOG TIMER

A 1232 type watchdog timer provides a degree of protection against hardware and software failures. When the watchdog timer is enabled, it must be periodically updated by software at least every 250 ms. A system failure which prevents updating will reset the CPU.

OPTO 22 INTERFACE

An industry standard Opto 22 interface provides 16 channels of buffered TTL input or output. The 34-pin connector is plug compatible with industry standard 4, 8, or 16-position modular I/O racks (Opto 22, Gordos, etc.) The open collector interface is also an excellent choice for general purpose TTL interfacing. Also featured is a rack power output which provides up to 500 mA at +5V, and is protected by a self resetting circuit breaker. See chapter 6 for other operating modes.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Size:
5.75" x 8.00"

Storage Temperature:
–40° C to 85° C

Operating Temperature:
VSBC-1:
0° C to +60° C (free air, no airflow)
VSBC-2:
0° C to +54° C (free air, no airflow)
0° C to +60° C (airflow = 100 ft/Min)

Power Requirements: *(with 32MB DRAM, 512K Flash, keyboard)*
5V ±5% @ 1250 ma typ.
±12V may be required by some expansion modules

System Reset:
V_{CC} sensing, resets below 4.70V
Watchdog reset

CPU Bus Speed:
CPU Internal:
VSBC-1: 100 MHz
VSBC-2: 133 MHz
CPU External: 33 MHz
PCI: 33 MHz
PC/104: 8MHz

DRAM Interface:
One standard 72-pin SIMM socket, parity or non-parity, standard or EDO, 70ns or faster

Flash Interface:
Four 32-pin PLCC sockets, compatible with 128Kx8 or 512Kx8 5V Flash or EPROMs

IDE Interface:
Two channels, standard 40-pin IDE, compatible with enhanced IDE modes 1, 2, & 3.
Supports up to four IDE drives

Floppy Disk Interface:
One 34-pin connector, supports two standard 5.25" or 3.5" drives

COM1 Interface:
RS-232, 16C550 compatible UART

COM2 Interface:
RS-232/422/485, 16C550 compatible UART

LPT Interface:
Bi-directional/EPP/ECP compatible

Opto 22 Interface:
16 channel, full compliance
Rack power output voltage: 4.7V typ. @ 500 ma

External Connectors:

Keyboard:	6-pin PS/2 style mini-DIN
IDE:	40-pin .1" headers
Floppy:	34-pin .1" header
COM Ports:	20-pin .1" header
LPT Port:	20-pin .1" header
Opto 22:	34-pin .1" header
CTC/INT:	14-pin .1" header
Power:	Standard 4-pin .156" disk drive style

Compatibility:
PC/104: Full compliance
Embedded-PCI (PC/104-Plus): Full compliance

Specifications are subject to change without notice.

Technical Support

If you have problems that this manual can't help you solve, contact VersaLogic for technical support at **(800) 824-3163 or (541) 485-8575**. You can also reach VersaLogic by e-mail at info@versalogic.com.

DOS Based Quick Start 2

This chapter describes how to quickly set up a bootable DOS-based system using your VSBC Single Board Computer.

Several recommended components are included in this discussion which are not necessarily required for low cost run-time systems. Video, keyboard, floppy disk, and hard drive devices are very convenient tools for the development environment, however, the VSBC does not demand their presence to boot and execute an application program. The simplest system consists of the VSBC with sufficient RAM, and a BIOS with a formatted, bootable Flash Disk System.

Caution Electrostatic discharge (ESD) can damage boards, disk drives, and other components. Do the installation procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part on the board cage.

Boards can be extremely sensitive to ESD and always require careful handling. After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an anti-static foam pad if available, but not the board wrapper. Do not slide the board over any surface.

The board should also be protected during shipment or storage with anti-static foam or bubble wrap. To prevent damage to the lithium battery, do not use black conductive foam or metal foil.

This chapter lists the recommended components for a development system, walks you through hardware assembly, and describes CMOS RAM Setup. When these steps are completed, the system will boot DOS from the on-board Flash Disk System.

The following steps are covered:

HARDWARE ASSEMBLY

- Attach standoffs
- Plug in SIMM RAM
- Plug in SVGA module
- Connect power supply to VSBC and peripheral components
- Plug in video, keyboard, floppy drive, hard drive

CMOS RAM SETUP

- Activating the battery
- Configure CMOS RAM

Typical Components

CORE ELECTRONICS

- VSBC with BIOS
- 4 Megabyte 72 pin SIMM RAM module
- PC/104 or Embedded PCI™ SVGA module
- Standard PC/AT power supply

MISCELLANEOUS HARDWARE

- Four 4-40 threaded 3/8" female-female metal hex standoffs
- Four 4-40 threaded 5/8" male-female metal hex standoffs
- Four 6-32 threaded 3/8" female-female metal hex standoffs
- Four 4-40 1/4" screws, pan head
- Four 6-32 1/4" screws, pan head

CABLES

- Video adapter cable (if EPM-SVGA-1 is used)
- Floppy drive cable
- IDE hard drive cable

PERIPHERALS

- VGA monitor
- Standard PC/AT keyboard
- Floppy disk drive
- IDE hard drive

Hardware Assembly

STANDOFFS

The VSBC mounts on four 6-32, 3/8" female-female hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using 1/4" 6-32 pan head screws threaded from the topside.

Four additional 4-40, 3/8" standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and demated. These are secured with four 4-40, 5/8" male-female standoffs (C) threaded from the topside which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or it can be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mouting surface to prevent circuit board flexing. Refer to the Physical Dimensions drawing on page 18 for details.

Note Standoffs and screws for (A and B) are available as part number VL-HDW-102. Standoffs and screws for (C) are available as part number VL-HDW-100.

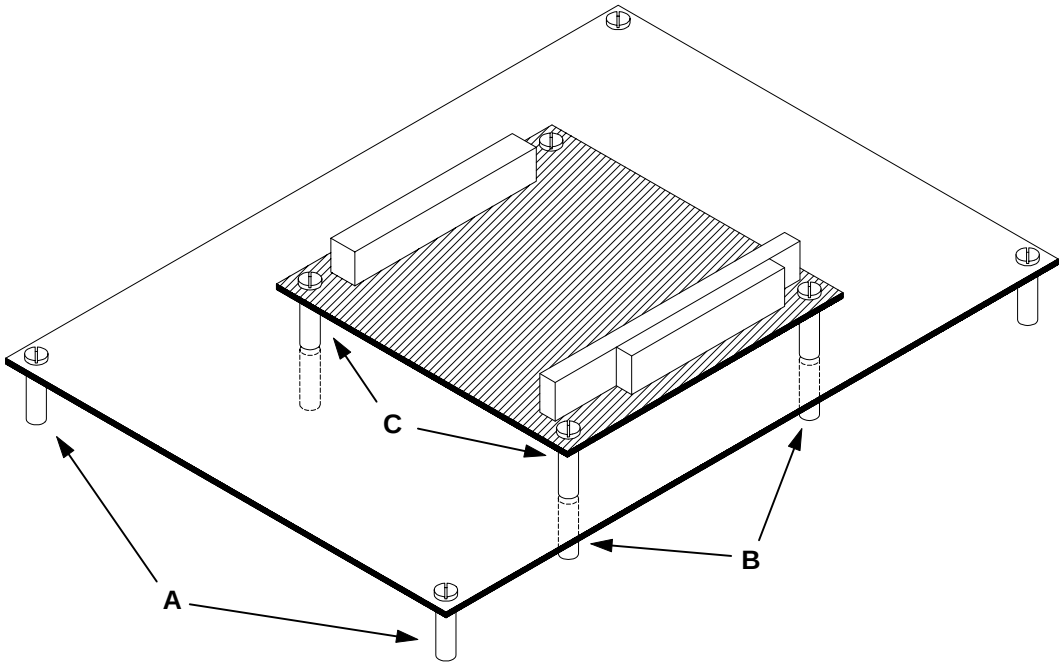
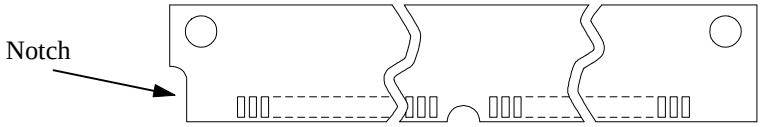


Figure 1. Standoff Locations

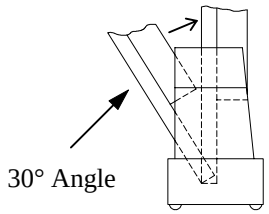
SIMM RAM

The VSBC is shipped with the SIMM module removed to prevent physical damage during shipment. Socket U1 will accept one 72-pin 4 to 64 MB SIMM module.

1. Orient the SIMM module so that the notch on the edge of the board aligns with the polarization key on socket U1 (left side of connector, near the lithium battery).



2. Grasp the SIMM module along the top edge and insert the contact pad edge into the connector at an angle of approximately 30° from vertical until it is seated in the slot.



Note Make sure that the module board is fully seated in the slot before rotating it into position. A slight force may be required to seat the board due to the connector contact "wipe" on the circuit pads at the edge of the board.

3. Maintain an even pressure over the length of the module board and rotate the module forward until the edges of the board ends snap behind the metal latch tabs of the connector. A slight force may be required to engage the latch tabs at both ends of the connector.

Caution It is extremely important that both latch tabs be engaged. Make sure the two plastic protrusions on the connector protrude through the holes on the module board. Failure to engage both latch tabs may result in a poor connector for the module board, broken latches, and the replacement of the connector. **This type of damage is not covered under warranty.**

SVGA MODULE

The next step is to plug in the SVGA video module. Having video allows you to interact with the CMOS Setup screens and with the DOS prompt, and assists in the debugging phase of your application development. Run-time systems do not need to have video if the application doesn't call for it.

The instructions in this section assume you are using VersaLogic's EPM-SVGA-1 Embedded-PCI™ (PC/104-*Plus*) module.

Note Before continuing, the four topside standoffs (C) must be installed as shown on page 9. These serve as mounting struts for the video module.

1. Line up the PC/104 and PCI connectors with the mating connectors on the VSBC. Firmly push down on the expansion module making sure to apply even pressure directly above both connectors with your fingers.
2. Secure the module to the standoffs using four 4-40 pan head screws.
3. Plug the video adapter cable (VL-CBL-1601) into connector J2 on the expansion module. This brings the SVGA signals out to a standard PC/AT 15-pin mini VGA connector.
4. Plug the video monitor into the adapter cable.

POWER SUPPLY

A standard PC/AT power supply is used to provide power to the VSBC and to the disk drive units. Plug one of the power supply cables into connector J7 on the VSBC. Plug the other power supply cables into the back of the floppy disk and hard disk drives.

Caution Do not turn the power supply on until all peripherals are plugged in.

PERIPHERAL CONNECTIONS

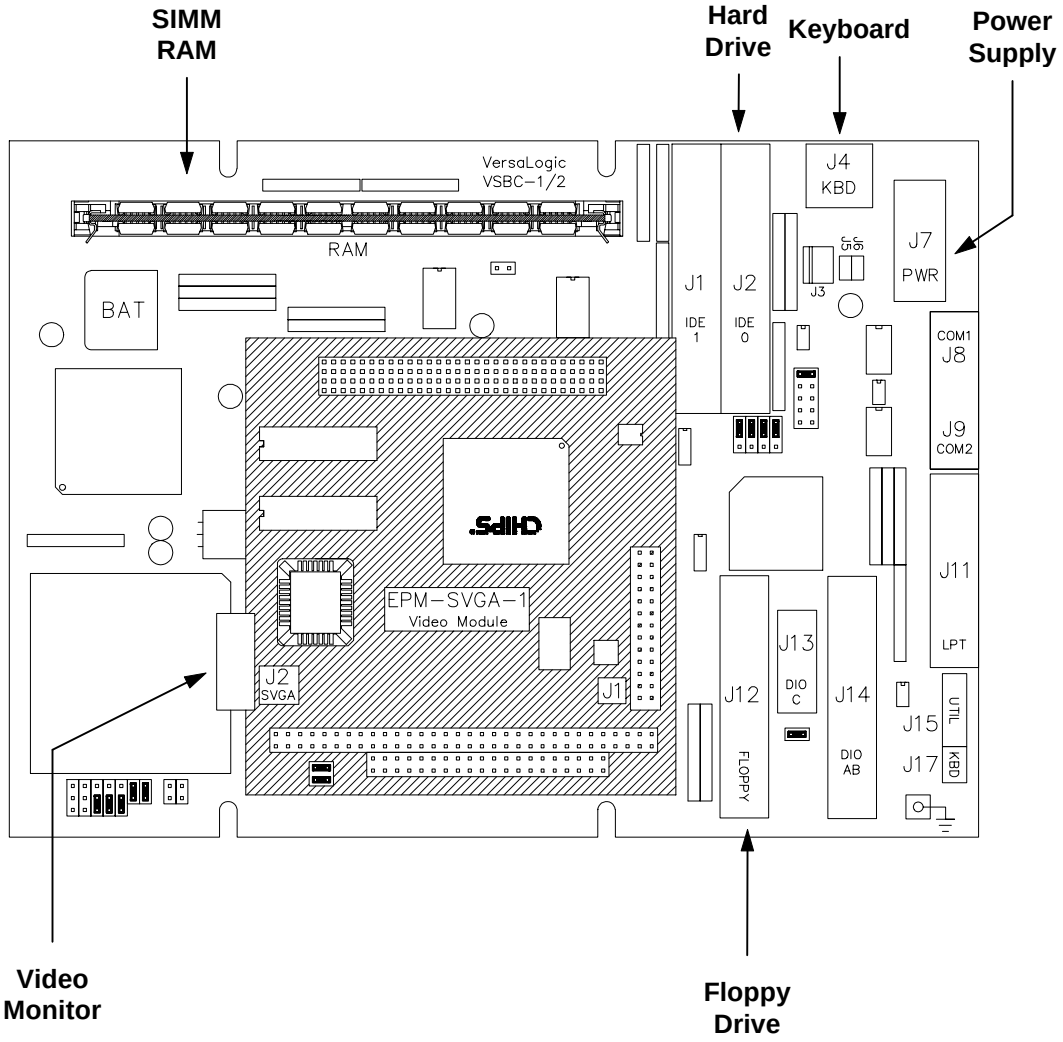
A variety of standard PC/AT peripheral devices are needed to round out the development system. A mouse and a printer are also options you might consider adding.

Hard Drive -- Plug IDE cable (VL-CBL-4001) into connector J2. Make sure your IDE hard drive is configured as a master.

Floppy Drive -- Plug floppy cable (VL-CBL-3403) into connector J12. If your floppy cable has a twist in it, use the connector at the far end of the cable, this will configure the floppy as A:

Video Monitor -- Plug the (VL-CBL-1601) adapter cable into connector J2 on the EPM-SVGA-1 module. Plug the monitor cable into the adapter.

Keyboard -- Plug a standard PC/AT keyboard into connector J4.



CABLE AND HARDWARE ASSEMBLIES

To bring the header connectors on the VSBC CPU board out to standard PC/AT style pinouts, the VersaLogic cable assemblies listed below are required.

Table 1: Single Board Computer Cable Assemblies.

Connector		Part #	Description	Connects to:
J1, J2	IDE	VL-CBL-4001	1.5 ft. 40-pin to two 40-pin, IDE	One or two external IDE drives
J3	AUX POWER	—	—	Negative voltage power supply
J4	KEYBOARD	VL-CBL-0601	Adapter from 6-pin mini DIN to standard AT style	Keyboard
J5	IDE 0 LED	—	—	External LED
J6	IDE 1 LED	—	—	External LED
J7	POWER	—	—	Power supply
J8, J9	COM1/COM2	VL-CBL-2001	1 ft. 20-pin socket to two DB-9M	External equipment (e.g, mouse)
J10	PLD	—	Factory use only	Specialty programming hardware
J11	LPT	VL-CBL-2601	1 ft. 26-pin socket to DB-25F	Printer
J12	FDC	VL-CBL-3403	1.5 ft. 34-pin to two 34-pin, floppy	One or two external floppy drives
J13	INT/CTC	—	—	External equipment
J14	OPTO 22	VL-CBL-3404	3 ft. 34-pin to 50-pin socket	Opto 22 rack
J15	UTIL	VL-CBL-1801	Cable kit: 18-pin socket & pins	Miscellaneous
J16	FAN	—	—	CPU Fan
J17	UTIL	VL-CBL-1801	Cable kit: 18-pin socket & pins	Miscellaneous

Table 2: Video Module Cable Assemblies.

Connector	Part #	Description	Connects to:
J1	N/A	VGA Feature Connector	Expansion daughterboards
J2	VL-CBL-1601	1 ft. 16-pin socket to 15-pin VGA	Video monitor

Jumper Configuration

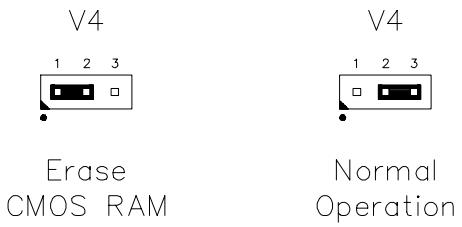
BATTERY ACTIVATION

Before the CMOS RAM can be configured, you must confirm that the on-board battery is activated.

Warning! The lithium battery may explode if mistreated. Do not wrap circuit board in aluminum foil or rest board on a conductive surface. Do not recharge, disassemble, or dispose of in fire.

The VSBC is shipped with the battery disconnected. Since the battery provides backup power to the CMOS RAM and the real time clock circuits when the board is powered down, the battery must be activated before putting the board in service.

To activate the battery, move jumper V4 to position [2-3].



CMOS RAM Setup

The VL-586-1 CPU card uses battery-backed, non-volatile CMOS RAM provided by the real time clock chip to store system configuration settings. You can change these system settings with the Setup program (accessed manually during system boot.) The configuration information is read by the CPU upon system reset.

The Setup program is permanently stored in ROM, and can be run with or without an operating system present. To run Setup, reset the CPU card and press the `DEL` key when prompted.

Select "`BASIC CMOS CONFIGURATION`" to display a summary of the information stored in the CMOS RAM. To change the values shown, use the cursor arrows to move the highlight bar to the desired entry field and press the – or + keys to change the values.

When you are finished, exit to the main Setup menu and select "`WRITE TO CMOS AND EXIT`" to save the changes and exit the Setup program.

CMOS Setup Options

MAIN CMOS SETUP MENU

SYSTEM BIOS SETUP - UTILITY VERSION 4.000.xxx (C) 1994-1996 VERSALOGIC, CORP. ALL RIGHTS RESERVED
Basic CMOS Configuration Advanced Configuration Format Integrated Flash Disk Reset CMOS to last known values Reset CMOS to factory defaults Write to CMOS and Exit Exit without changing CMOS
<ESC> TO CONTINUE (NO SAVE)

BASIC CMOS CONFIGURATION

This option goes to another menu which allows you to change the following:

- Date, Time
- Drive assignments and types
- Boot sequence
- Keyboard Parameters
- Memory Tests and Parity

ADVANCED CONFIGURATION

This option goes to another menu which allows you to change the following:

- Bus Timing
- Memory and I/O Mapping
- Cache Control

SHADOW CONFIGURATION

This option allows you to change ROM shadowing parameters.

RESET CMOS TO LAST KNOWN VALUES

This option acts like an undo function. It reverts all changes made in the *CMOS Setup Screens* to the values they had when Setup was first entered.

RESET CMOS TO FACTORY DEFAULTS

This option overwrites all information contained in the CMOS RAM with predefined parameters stored in the BIOS ROM, and reboots the CPU card.

The following parameters are loaded into CMOS RAM when this option is selected:

Basic CMOS Configuration

```
Base Memory       : 640                Date (month day year) : Jan 01, 1997
Extended Memory   : 15360              Time (hours:min:sec)  : 00 : 00 : 00
Drive A: type     : Flash Disk
Drive B: type     : Not installed      Cyln Heads WPcom LZone Sect Size
Hard disk C: type : Not installed
Hard disk D: type : Not installed

1st Boot Device   : Drive A:           Seek Floppy at Boot       : Enabled
2nd Boot Device   : (None)             Seek Hard Drive At Boot   : Enabled
3rd Boot Device   : (None)             Display "Hit <Del>..."    : Enabled
4th Boot Device   : (None)             System Configuration Box  : Enabled
Typematic Keys    : Enabled            Wait for F1 on Error      : Enabled
Typematic Delay   : 250 ms             NumLock State at Boot     : Disabled
Typematic Rate    : 30 cps
Memory Test Tick  : Enabled            PC/104 Video Shadowing    : Enabled
Test Above 1MB    : Enabled
```

Advanced Configuration

```
AT Bus Clock               : CPUCLK/4 | Fast PC/104 Cycle          : Enabled
DMA Clock                  : AT clock | Fast PCI Memory Cycle      : Enabled
16 bit ISA Wait States     : 1 w/s    | CPU->PCI Write Buffer      : Enabled
PC/104 I/O Recovery Setting: Enabled  | CPU->PCI Write Buff. Merge : Enabled
PC/104 I/O Recovery Time   : 24*ATClk | CPU->PCI Write Buff. Burst : Enabled
DRAM Read Timing           : Normal   | CPU->PCI Fast Back-to-Back : Enabled
DRAM Write Timing          : Normal   | PCI->CPU Read Buffer       : Enabled
SRAM/DRAM Decoding w/s     : 0 w/s    | PCI->CPU Write Buffer      : Enabled
SRAM Read/Write Timing     : Not Used | PCI->CPU Write Buff. Burst : Enabled
DRAM Hidden Refresh        : Enabled  | Internal Cache             : Enabled
Slot 1 Using INT#          : INT A    | PCI INT A -> IRQ#          : IRQ 15
Slot 2 Using INT#          : INT B    | PCI INT B -> IRQ#          : IRQ 12
Slot 3 Using INT#          : INT C    | PCI INT C -> IRQ#          : IRQ 11
Slot 4 Using INT#          : INT D    | PCI INT D -> IRQ#          : IRQ 10
```

WRITE TO CMOS AND EXIT

This option updates the CMOS RAM with the information in the *CMOS Setup Screens*. After writing, the CMOS checksum is updated and the CPU card is rebooted.

EXIT WITHOUT CHANGING CMOS

This option acts like a cancel function. Use it to exit Setup without changing CMOS RAM.

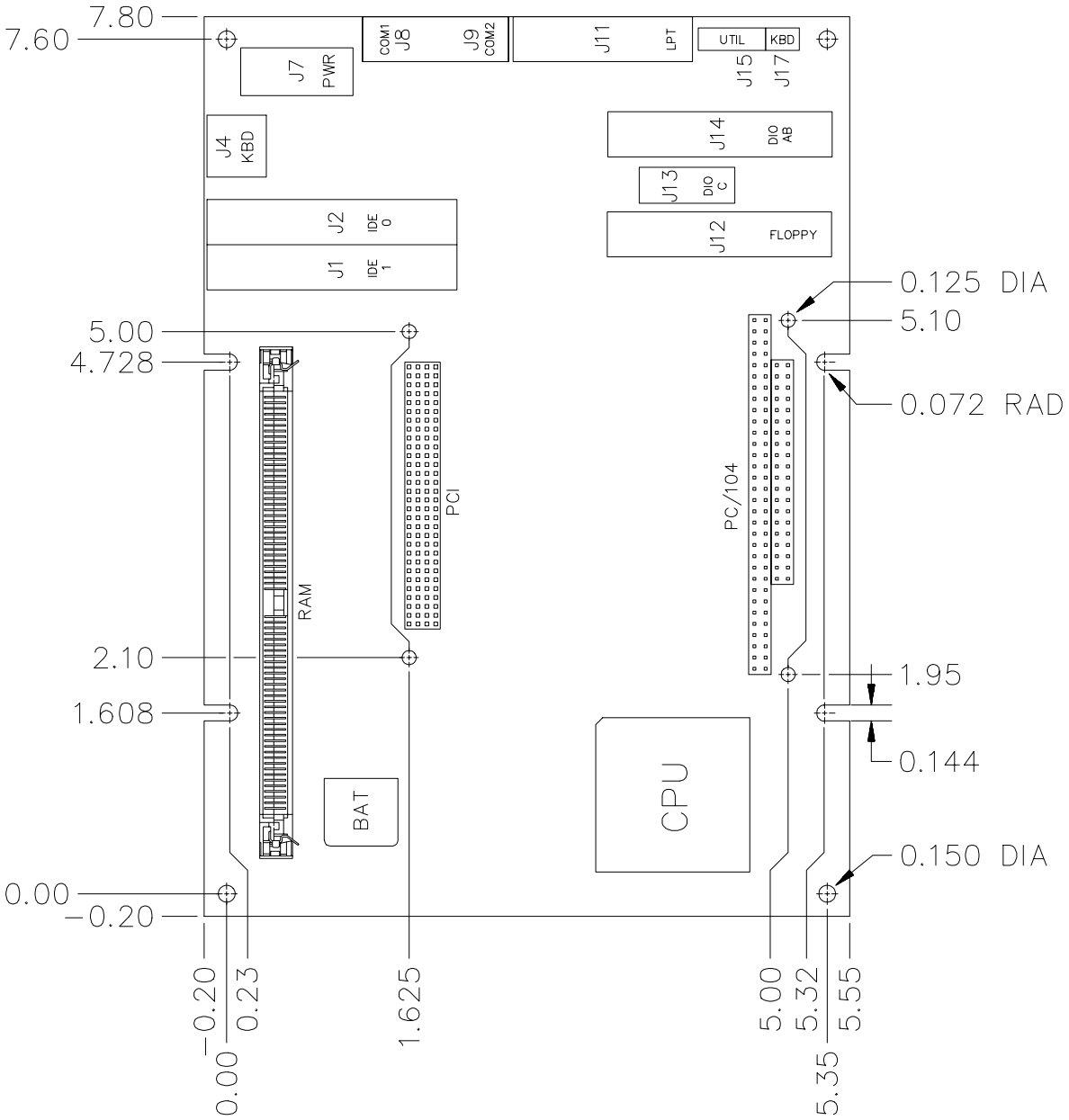
Clearing the CMOS RAM

Jumper V4[1-2] allows you clear the CMOS RAM contents if you remove the battery, install incorrect setup information, or otherwise corrupt CMOS RAM. To ensure integrity of the CMOS RAM, the Setup program calculates and stores an internal checksum of the setup data. Upon reset, the CPU detects if the CMOS RAM is corrupted by analyzing the checksum. If you wish to completely clear the contents of the CMOS RAM, briefly move jumper V4 to position [1-2] (top position) then back to the position [2-3] (lower position) and reboot the system. This process will load the factory default setup parameters into the CMOS RAM.

Warning! Do not apply power to the CPU board with jumper V4[1-2] installed, doing so may damage the chipset and void the warranty. Jumper V4[1-2] is only briefly used to clear the CMOS RAM.

Figure 2. CMOS RAM Jumper

Physical Dimensions



Not to scale. All dimensions in inches.

Figure 3. VSBC Physical Dimensions

Configuration 3

This chapter describes how to configure the on-board options for the VSBC CPU board. Configuration involves both hardware (jumper) and software (chipset) configuration. The jumpers configure the circuitry on the board for various modes of operation. The software configuration completes the process by initializing the circuits within the chipset. This chapter does not describe how to initialize the standard DOS peripheral devices such as the serial ports and disk drive interfaces.

Hardware Jumper Summary

Hardware option configuration is accomplished by installing or removing jumper plugs. In this chapter, the term “in” is used to indicate an installed jumper and “out” is used to indicate a removed jumper.

Use the following key to interpret the jumper diagrams used in this manual:

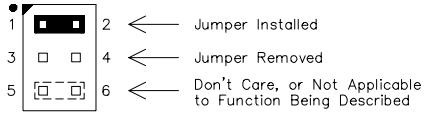


Figure 4. Jumpering Key

JUMPER BLOCK LOCATIONS

Note Jumpers and resistor packs shown in as-shipped configuration.

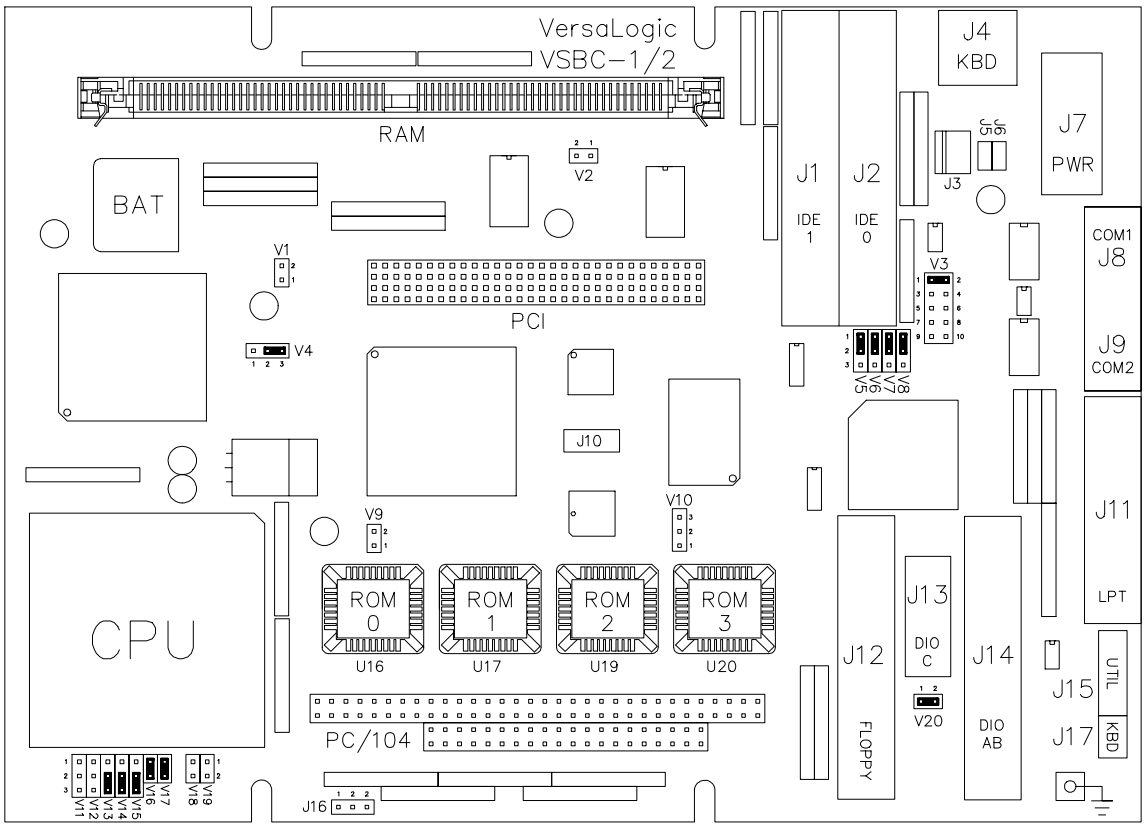
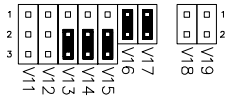
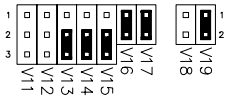


Figure 5. Jumper Block Locations

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**CMOS Battery Test Terminals** ***Note!*** *V1 is not a jumper. It is used as a test point to measure the current flowing in the CMOS battery circuit.*	—	—
V2[1-2]	**PCI / CPU Local Bus Speed** In — 25 MHz Out — 33 MHz	Out	—
V3[1-2]	**RS-232 Signal Enable** In — RS-232 mode. Enables the RS-232 line drivers and receivers. Out — RS-422/485 mode. Disables the RS-232 line drivers and receivers.	In	29
V3[3-4]	**RS-422/485 Ground Circuit** In — RS-422/485 mode. Connects ground to J9 pin 6. Out — RS-232 mode. Frees J9 pin 6 for CTS2 (COM2).	Out	29
V3[5-6]	**RS-232/422/485 Mode Selector** In — RS-422/485 mode. Out — RS-232 mode.	Out	29
V3[7-8]	**RS-422/485 Differential Line Driver Control** In — RS-485 mode. Enables software control of the RS-485 line driver. Out — RS-422 mode. Disables the RS-485 line driver.	Out	29
V3[9-10]	**RS-422/485 Transmission Line Termination** In — Terminates data circuit with 100 Ω resistor (RS-422, or RS-485 endpoint stations only) Out — Leaves data circuit unterminated (RS-485 intermediate multidrop stations only)	Out	29
V4[1-2]	**CMOS RAM Erase** In — Erases CMOS RAM and Real Time Clock contents. Out — Normal operation (V4[2-3] must be in)	Out	26
V4[2-3]	**CMOS RAM Power** In — Connects power to CMOS RAM and Real Time Clock circuits Out — Power disconnected	In	26
V5[1-2]	**Interrupt Configuration (IRQ11 / PC/104 interconnect)** In — Connects PC/104 IRQ11 (D4) to IRQ11 Out — Disconnects PC/104 from IRQ11	In	31
V5[2-3]	**Interrupt Configuration (IRQ11 / Front Plane 2 interconnect)** In — Connects Front Plane 2 (J13 pin 11) to IRQ11 Out — Disconnects FP2 from IRQ11	Out	31
V6[1-2]	**Interrupt Configuration (IRQ3 / PC/104 interconnect)** In — Connects PC/104 IRQ3 (B25) to IRQ3 Out — Disconnects PC/104 from IRQ3	In	31
V6[2-3]	**Interrupt Configuration (IRQ3 / Front Plane 1 interconnect)** In — Connects Front Plane 1 (J13 pin 9) to IRQ3 Out — Disconnects FP1 from IRQ3	Out	31
V7[1-2]	**Interrupt Configuration (IRQ12 / PC/104 interconnect)** In — Connects PC/104 IRQ12 (D5) to IRQ12 Out — Disconnects PC/104 from IRQ12	In	31
V7[2-3]	**Interrupt Configuration (IRQ12 / Front Plane 3 interconnect)** In — Connects Front Plane 3 (J13 pin 13) to IRQ12 Out — Disconnects FP3 from IRQ12	Out	31

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V8[1-2]	**Interrupt Configuration (IRQ15 / PC/104 interconnect)** In — Connects PC/104 IRQ15 (D6) to IRQ15 Out — Disconnects PC/104 from IRQ15	In	31
V8[2-3]	**Interrupt Configuration (IRQ15 / CIO interconnect)** In — Connects CIO Interrupts to IRQ15 Out — Disconnects CIO from IRQ15	Out	31
V9	**Chipset Configuration (PCI Bus Speed)** In — PCI Bus running at 50% CPU clock rate. Out — PCI Bus running at 100% CPU clock rate. ***Note!*** *This jumper must remain out.*	Out	—
V10[1-2]	**Chipset Configuration (Chipset Mfg. Selector)** ***Note!*** *This jumper has no function at this time.*	Out	—
V10[2-3]	**Chipset Configuration (Chipset Mfg. Selector)** ***Note!*** *This jumper has no function at this time.*	Out	—
V11 – V19	**CPU Chip Configuration (Miscellaneous Control Signals)** VSBC-1 (100 MHz 486)  VSBC-2 (133 MHz 5x86)  	Varies	—
V20	**Opto 22 I/O Rack Power** In — I/O rack power provided by VSBC Out — I/O rack power provided externally	In	—

Memory Configuration

FLASH CONFIGURATION

The four on-board ROM sockets (U16, U17, U19, and U20) accept 128Kx8, 256Kx8, or 512Kx8, 32 pin plastic PLCC or 32 pin J-lead ceramic memory devices. An extractor tool (such as VersaLogic part number 9685) is required to remove the rectangular PLCC device(s) without damage.

The VSBC is sold with two ROM options.

BIOS/Flash Option (-g) — *BIOS in 128 KB EPROM*. Socket U16 contains a 128KB BIOS ROM allowing the VSBC to boot an operating system from an attached Floppy Drive or Hard Drive. The remaining sockets (U17, U19, and U20) are empty.

BIOS/Flash Option (-h) — *BIOS & Flash Disk System in 512 KB Flash.* Socket U16 contains a 512KB Flash chip with BIOS and a Flash Disk System. The storage size of the flash disk system can be increased in 512KB increments by installing up to three flash chips (part number VL-FLSH-512) into sockets U17, U19, and U20, giving a maximum storage size of 2MB.

Table 4: Flash Disk System Storage

Number of Flash Chips	Storage Space (not counting operating system boot files)
1	377,344 bytes
2	886,272 bytes
3	1,395,200 bytes
4	1,905,152 bytes

There are no configuration jumpers for the ROM sockets.

DRAM CONFIGURATION

The on-board DRAM SIMM socket (U1) accepts one standard 72-pin SIMM module. A variety of DRAM sizes may be used (4M, 8M, 16M, 32M, or 64M.) Parity and non-parity modules may be used. Fast Page Mode and EDO type modules are supported, provided they are 70ns or faster.

See page 10 for a detailed explaination on how to insert SIMM modules from socket U1.

CMOS RAM CONFIGURATION

The VSBC CPU board is shipped with the battery connected. Since the battery provides backup power to the CMOS RAM and the real time clock circuits when the board is powered down, the jumper must remain in this setting for normal operation.

Jumper V4[1-2] (left position) can be briefly used to erase the contents of the CMOS RAM should it become necessary to do so.

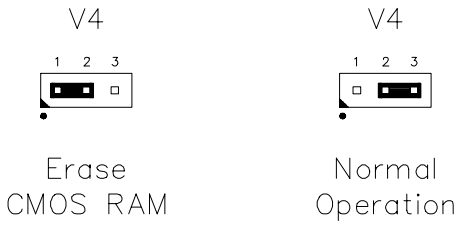
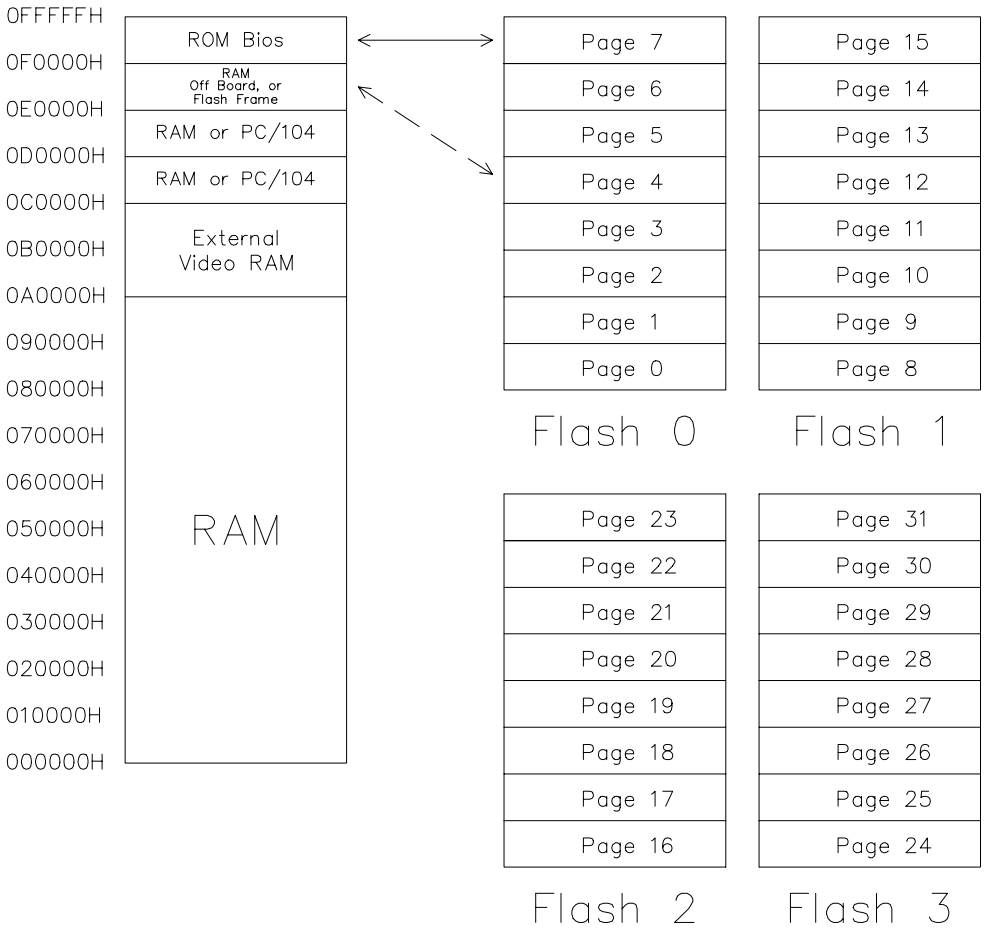


Table 5: CMOS RAM Jumpers

Jumper Block	Description	As Shipped
V4[1-2]	**CMOS RAM Erase** In — Erases CMOS RAM and Real Time Clock contents Out — Normal operation (V4[2-3] must be in)	Out
V4[2-3]	**CMOS RAM Power** In — Connects power to CMOS RAM and Real Time Clock circuits Out — Power disconnected	In

MEMORY MAPPING

The lower 1 Meg. memory map of the VSBC is arranged as follows. Page 7 of Flash 0 is the system BIOS, and always appears from 0F0000h to 0FFFFFh. Bits D4–D0 in the MPCR register select which Flash ROM page is mapped into the Flash Frame (0E0000h to 0EFFFFh). See MPCR register description on page 66 for further information.



I/O Configuration

PC/104 Expansion Modules

PC/104 I/O modules will work properly with the VSBC when addressed anywhere between 100h and 3FFh. Care must be taken to avoid the following I/O addresses used by on-board peripherals and video devices.

Table 6: On-Board I/O Devices

I/O Device	I/O Range
Hard Disk Controller #1	170h – 177h
Hard Disk Controller #2	1F0h – 1F7h
COM2	2F8h – 2FFh
LPT1	378h – 37Fh
SVGA	3B0h – 3DFh
Floppy Disk Controller	3F0h – 3F7h
COM1	3F8h – 3FFh

Note The address range occupied by an on-board device is freed up when the device is disabled in CMOS Setup.

PCI Expansion Modules

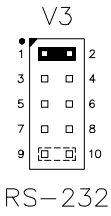
PCI Expansion Modules do not use CPU I/O addressing. No configuration is necessary except to jumper the expansion module for the correct stack position. See your expansion module reference manual for further information.

COM2 Configuration

Serial Port COM2 can be operated in RS-232, RS-422, or RS-485 modes. Jumper V3 is used to configure the port.

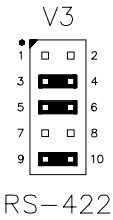
RS-232 OPERATION

For RS-232 operation, jumper V3 should be jumpered as shown. The state of jumper V3[9-10] doesn't matter, it can be in or out.



RS-422 OPERATION

For RS-422 operation, jumper V3 should be jumpered as shown.



Note This configuration inserts a 100 Ohm line termination resistor in the circuit. An equivalent resistor must exist at the opposite end of the cable to form a 50 Ohm balanced transmission line.

RS-485 OPERATION

Removing V3[9-10] leaves the data circuit unterminated so that COM2 can be used as an intermediate station in an RS-485 multidrop system. When COM2 is used in multidrop operations, remove jumper V3[9-10] from all stations except both ends of the line.

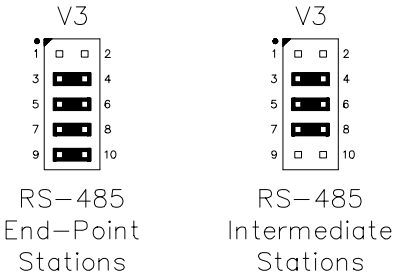


Table 7: Serial Port Jumpers

Jumper Block	Description	As Shipped
V3[1-2]	**RS-232 Signal Enable** In — RS-232 mode. Enables the RS-232 line drivers and receivers. Out — RS-422/485 mode. Disables the RS-232 line drivers and receivers.	In
V3[3-4]	**RS-422/485 Ground Circuit** In — RS-422/485 mode. Connects ground to J9 pin 6. Out — RS-232 mode. Frees J9 pin 6 for CTS2 (COM2).	Out
V3[5-6]	**RS-232/422/485 Mode Selector** In — RS-422/485 mode. Out — RS-232 mode.	Out
V3[7-8]	**RS-422/485 Differential Line Driver Control** In — RS-485 mode. Enables software control of the differential line driver. Out — RS-422 mode. Permanently enables the differential line driver.	Out
V3[9-10]	**RS-422/485 Transmission Line Termination** In — Terminates data circuit with 100 Ω resistor (RS-422, or RS-485 endpoint stations only) Out — Leaves data circuit unterminated (RS-485 intermediate multidrop stations only)	Out

Interrupt Configuration

Four three-position jumper blocks are used to configure the interrupt sources on the VSBC. Each jumper block is used to select one of two interrupt sources and route it to the interrupt controller. Wire wrap techniques can be used on V5, V6, V7 and V8 to route interrupt sources to the CPU's IRQ inputs if the factory provided jumpers do not provide suitable connections.

Interrupts from the PCI Bus are routed using a programmable matrix. Interrupt configuration for the PCI bus is handled through the CMOS Setup screen.

Note Jumpers shown in as-shipped configuration.

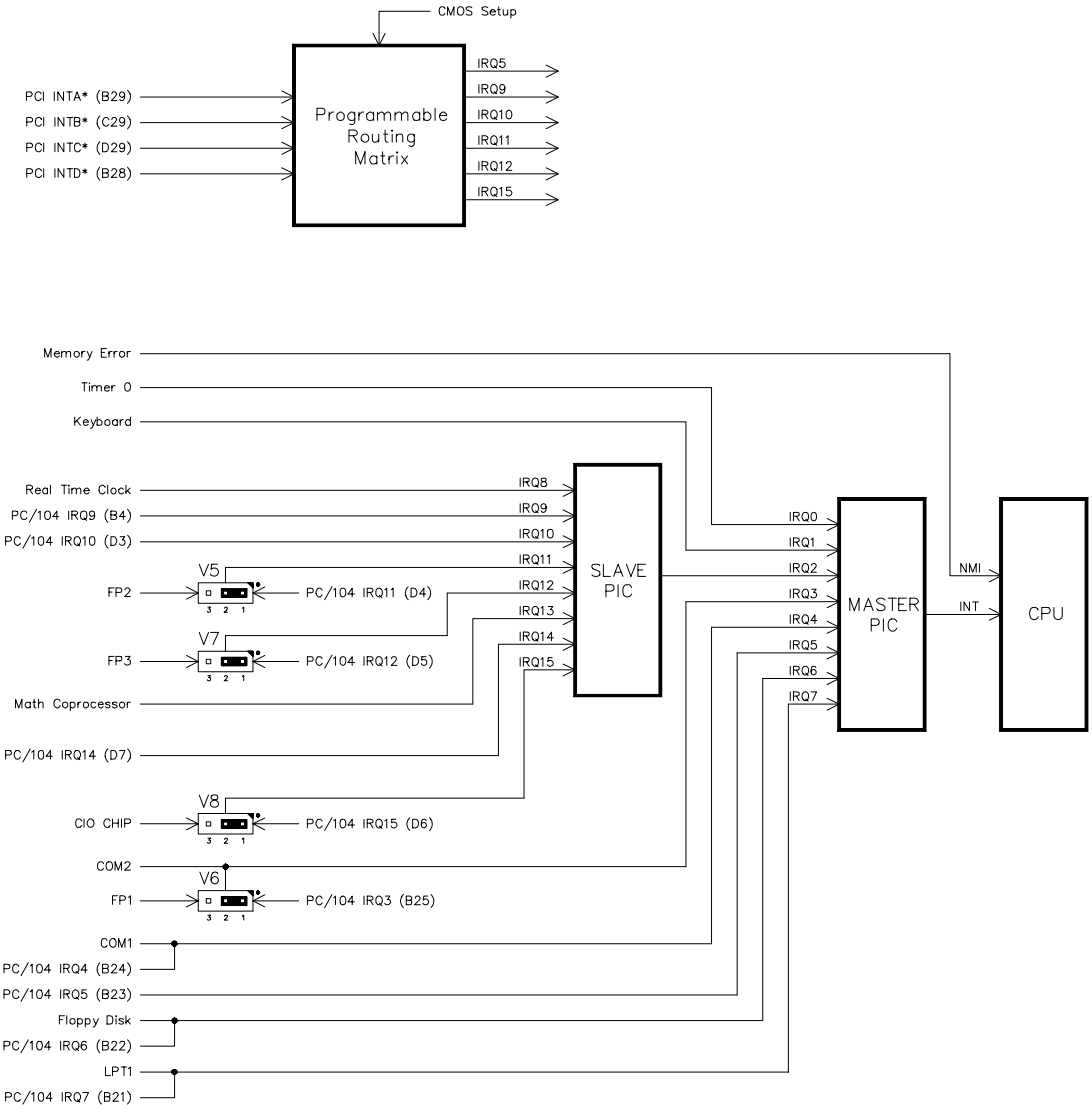


Figure 6. Interrupt Circuit Diagram

INTERRUPT CONFIGURATION JUMPERS

Table 8: Interrupt Configuration Jumpers

Jumper Block	Description	As Shipped
V5[1-2]	**Interrupt Configuration (IRQ11 / PC/104 interconnect)** In — Connects PC/104 IRQ11 (D4) to IRQ11 Out — Disconnects PC/104 from IRQ11	In
V5[2-3]	**Interrupt Configuration (IRQ11 / Front Plane 2 interconnect)** In — Connects Front Plane 2 (J13 pin 11) to IRQ11 Out — Disconnects FP2 from IRQ11	Out
V6[1-2]	**Interrupt Configuration (IRQ3 / PC/104 interconnect)** In — Connects PC/104 IRQ3 (B25) to IRQ3 Out — Disconnects PC/104 from IRQ3	In
V6[2-3]	**Interrupt Configuration (IRQ3 / Front Plane 1 interconnect)** In — Connects Front Plane 1 (J13 pin 9) to IRQ3 Out — Disconnects FP1 from IRQ3	Out
V7[1-2]	**Interrupt Configuration (IRQ12 / PC/104 interconnect)** In — Connects PC/104 IRQ12 (D5) to IRQ12 Out — Disconnects PC/104 from IRQ12	In
V7[2-3]	**Interrupt Configuration (IRQ12 / Front Plane 3 interconnect)** In — Connects Front Plane 3 (J13 pin 13) to IRQ12 Out — Disconnects FP3 from IRQ12	Out
V8[1-2]	**Interrupt Configuration (IRQ15 / PC/104 interconnect)** In — Connects PC/104 IRQ15 (D6) to IRQ15 Out — Disconnects PC/104 from IRQ15	In
V8[2-3]	**Interrupt Configuration (IRQ15 / CIO interconnect)** In — Connects CIO Interrupts to IRQ15 Out — Disconnects CIO from IRQ15	Out

PC/104 INTERRUPT SIGNALS

The following table describes the 11 PC/104 interrupt signals. Some of these interrupt signals are hardwired to specific IRQ inputs, and others are connected to jumpers V8 through V12 for custom configuration. Some interrupts are shared with the PCI Bus interface and on-board peripherals (which can be disabled if necessary.)

Table 9: PC/104 Interrupt Signals.

Interrupt Level	PC/104 Signal Name	PC/104 Pin Number	Notes
IRQ0	—	—	Doesn't exist on PC/104 bus
IRQ1	—	—	Doesn't exist on PC/104 bus
IRQ2	—	—	Doesn't exist on PC/104 bus
IRQ3	IRQ3	B25	This signal can be connected to interrupt IRQ3 by inserting jumper V6[1-2]. Also shared by on-board COM2 port.
IRQ4	IRQ4	B24	This signal is hardwired into interrupt IRQ4. Also shared by on-board COM1 port.
IRQ5	IRQ5	B23	This signal is hardwired into interrupt IRQ5. Also can be shared with the PCI bus.
IRQ6	IRQ6	B22	This signal is hardwired into interrupt IRQ6. Also shared by on-board floppy drive controller.
IRQ7	IRQ7	B21	This signal is hardwired into interrupt IRQ5. Also shared by on-board LPT1 port.
IRQ8	—	—	Doesn't exist on PC/104 bus
IRQ9	IRQ9	B4	This signal is hardwired into interrupt IRQ9. Also can be shared with the PCI bus.
IRQ10	IRQ10	D3	This signal is hardwired into interrupt IRQ10. Also can be shared with the PCI bus.
IRQ11	IRQ11	D4	This signal can be connected to interrupt IRQ11 by inserting jumper V5[1-2]. Also can be shared with the PCI bus.
IRQ12	IRQ12	D5	This signal can be connected to interrupt IRQ12 by inserting jumper V7[1-2]. Also can be shared with the PCI bus.
IRQ13	—	—	Doesn't exist on PC/104 bus
IRQ14	IRQ14	D7	This signal is hardwired into interrupt IRQ14
IRQ15	IRQ15	D6	This signal can be connected to interrupt IRQ12 by inserting jumper V8[1-2]. Also can be shared with the PCI bus.

PCI INTERRUPT SIGNALS

Table 10: PCI Interrupt Signals.

PCI Signal Name	PCI Pin Number	Interrupt Connection Options (Defined in CMOS Setup)
INTA*	B29	NONE, IRQ5, IRQ9, IRQ10, IRQ11, IRQ12, or IRQ15
INTB*	C29	NONE, IRQ5, IRQ9, IRQ10, IRQ11, IRQ12, or IRQ15
INTC*	—	NONE, IRQ5, IRQ9, IRQ10, IRQ11, IRQ12, or IRQ15
INTD*	B25	NONE, IRQ5, IRQ9, IRQ10, IRQ11, IRQ12, or IRQ15

CPU INTERRUPT REQUEST INPUTS

The seventeen standard IBM compatible interrupt inputs (IRQs) are shown below.

Table 11: Interrupt Request Inputs

Interrupt Signal Name	Interrupt Number	Typical Source of Interrupt on an IBM AT	As Shipped Configuration	Notes
NMI	—	Parity Check and IOCHCK from ISA Bus.	Hardwired	Internal signal, not available to the outside world.
IRQ0	08h	Timer 0	Hardwired	Internal signal, not available to the outside world.
IRQ1	09h	Keyboard	Hardwired	DOS/BIOS expects keyboard interrupts on this input. Comes from on-board keyboard circuits. Not available to the outside world.
IRQ2	0Ah	Slave Interrupt Controller	Hardwired	Internal signal, not available to the outside world.
IRQ3	0Bh	COM2	COM2	DOS/BIOS usually expects COM2 interrupts on this input. Other sources: • COM2 • PCI Bus • Front Plane Connector
IRQ4	0Ch	COM1	COM1	Shared with PC/104 Bus
IRQ5	0Dh	LPT 2	Hardwired	PC/104 Bus
IRQ6	0Eh	Floppy Disk	Hardwired	PC/104 Bus
IRQ7	0Fh	LPT1	Hardwired	DOS/BIOS usually expects LPT1 interrupts on this input. Other sources: • LPT1 • PC/104 Bus

Table 11: Interrupt Request Inputs

Interrupt Signal Name	Interrupt Number	Typical Source of Interrupt on an IBM AT	As Shipped Configuration	Notes
IRQ8	70h	Real Time Clock	Hardwired	Internal signal, not available to the outside world.
IRQ9	71h	Unassigned	Hardwired	PC/104 Bus
IRQ10	72h	Unassigned	Hardwired	PC/104 Bus
IRQ11	73h	Unassigned	Front Plane	IRQ11 can receive interrupts from the PC/104 Bus or from the Front-Plane connector J13 (FP2)
IRQ12	74h	Unassigned	Front Plane	IRQ12 can receive interrupts from the PC/104 Bus or from the Front-Plane connector J13 (FP3)
IRQ13	75h	Math Coprocessor	Hardwired	Internal signal, not available to the outside world.
IRQ14	76h	Hard Disk Drive	Hardwired	PC/104 Bus
IRQ15	77h	Unassigned		IRQ15 can receive interrupts from the PC/104 Bus or from the CIO chip.

4 External Connections

This chapter describes the external interfaces available on the VSBC CPU board.

CONNECTOR FUNCTIONS

Table 12: Connector Functions

Connector	Function
J1	IDE Channel 0
J2	IDE Channel 1
J3	PC/104 Auxillary Power (–5V & –12V)
J4	Keyboard
J5	IDE Channel 0 Drive Activity Light
J6	IDE Channel 1 Drive Activity Light
J7	Main Power Input
J8/J9*	COM1 and COM2 Ports
J10	PLD Reprogramming Port (Factory use Only)
J11	LPT1 Port
J12	Floppy Disk Interface
J13	Front Plane and CIO Port C Signals
J14	Opto-22 Interface
J15	Speaker, Power Good, Reset, LED
J16	Fan Power Output
J17	Keyboard

Note Connector J8/J9 is a single 20-pin connector.

CONNECTOR LOCATIONS

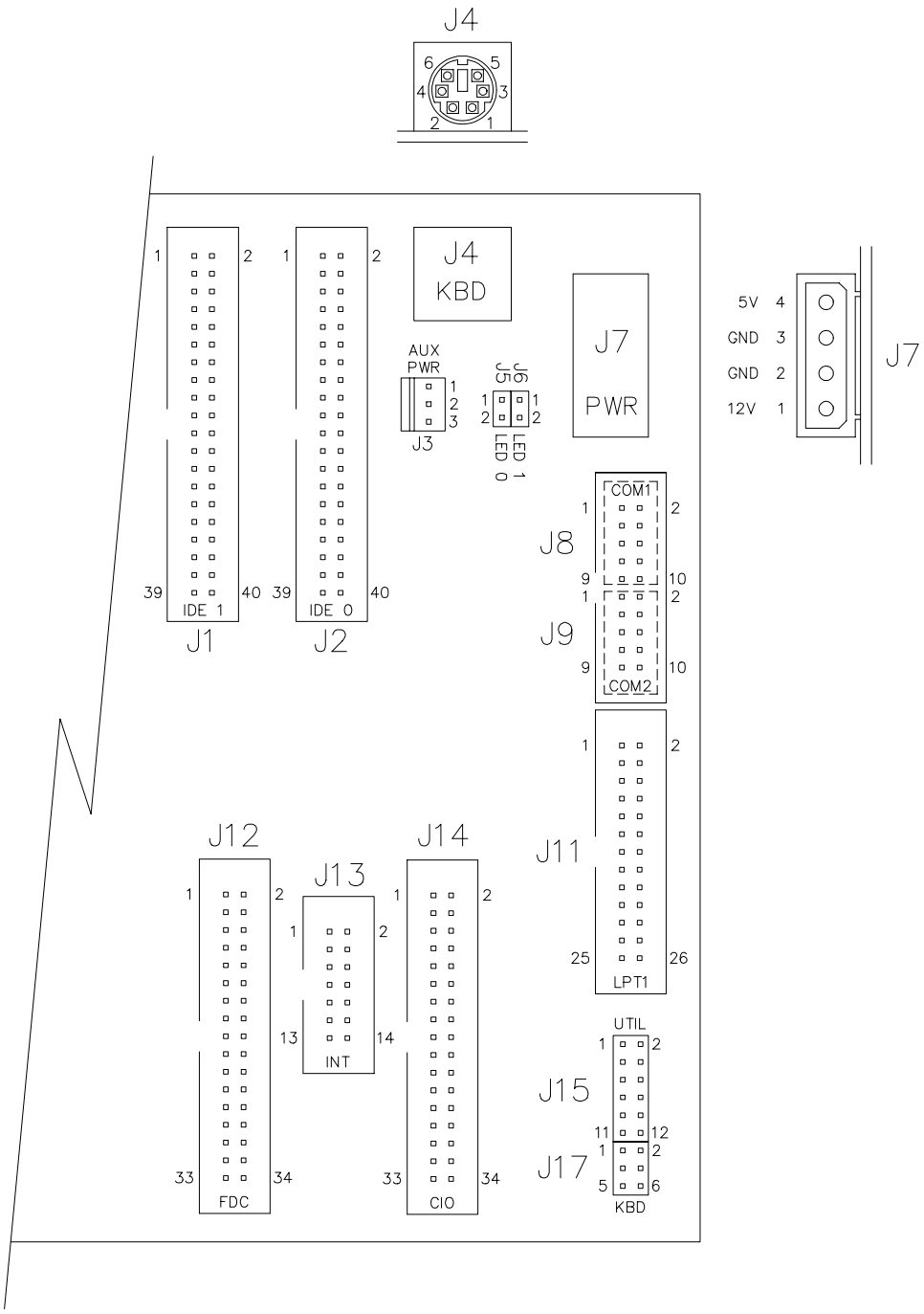


Figure 7. Connector Locations

MATING CONNECTORS AND CABLE ASSEMBLIES

Connections to the VSBC can be made using flat ribbon cable and mass-terminated mating connectors. To bring the connectors on the VSBC board out to standard PC/AT style pinouts, the VersaLogic cable assemblies listed below can be used.

Schematic diagrams for the cable assemblies are shown on the following pages.

Table 13: Mating Connectors and Cable Assemblies

Connector	Mating Connector	Cable Part #	Description	Connects to:
J1 & J2 (IDE)	3417-6640	VL-CBL-4001	1.5 ft. 40-pin IDC to two 40-pin IDC	IDE hard disk drive
J3 (POWER)	Molex 22-01-2035	—	—	Auxillary Power Input
J4 (KEYBOARD)	6-pin DIN PS/2 type connector	VL-CBL-0601	3 in. Mini DIN to standard AT Keyboard	Keyboard
J5 (IDE 0 LED)		—	—	Drive activity light
J6 (IDE 1 LED)		—	—	Drive activity light
J7 (POWER)	Molex 15-24-4048	—	—	Power supply
J8/J9	3421-6620	VL-CBL-2001	1 ft. 20-pin IDC to two DB-9M	External equipment (e.g., modem or other device)
J10	—	—	—	Factory use only
J11	3399-6626	VL-CBL-2601	1 ft. 26-pin socket/DB-25F	LPT1 Port
J12	3414-6634	VL-CBL-3403	1.5 ft. 34-pin/two 34-pin	Floppy Disk Interface
J13	3385-6614	—	—	External Interrupts
J14	3414-6634	VL-CBL-5001 VL-CBL-5002 VL-CBL-5003 VL-CBL-5004	1.5 ft. 50-pin/socket 3 ft. 50-pin/socket 3 ft. 50-pin/card edge 4 ft. 50-pin/socket	Opto-22 Interface
J15 (UTIL)	AMP 1-87456	—	—	Miscellaneous
J16	—	—	—	Factory use only
J17	—	—	—	Keyboard

J1, J2 – HARD DISK DRIVE CONNECTORS

Two IDE interfaces are available to connect up to four hard disk drives. Connector J2 is the Primary IDE controller and connector J1 is the Secondary IDE Controller.

Caution Cable length must be 18” or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 14: IDE Hard Disk Connector Pinout

J1, J2 Pin	Signal Name	IDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU
2	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7
4	HD8	DATA 8	Data bit 8
5	HD6	DATA 6	Data bit 6
6	HD9	DATA 9	Data bit 9
7	HD5	DATA 5	Data bit 5
8	HD10	DATA 10	Data bit a
9	HD4	DATA 4	Data bit 4
10	HD11	DATA 11	Data bit 11
11	HD3	DATA 3	Data bit 3
12	HD12	DATA 12	Data bit 12
13	HD2	DATA 2	Data bit 2
14	HD13	DATA 13	Data bit 13
15	HD1	DATA 1	Data bit 1
16	HD14	DATA 14	Data bit 14
17	HD0	DATA 0	Data bit 0
18	HD15	DATA 15	Data bit 15
19	Ground	Ground	Ground
20	NC	NC	No connection
21	NC	NC	No connection
22	Ground	Ground	Ground
23	HWR*	HOST IOW*	I/O write
24	Ground	Ground	Ground
25	HRD*	HOST IOR*	I/O read
26	Ground	Ground	Ground
27	NC	NC	No connection
28	HAEN	ALE	Address latch enable
29	NC	NC	No connection
30	Ground	Ground	Ground
31	HINT	HOST IRQ14	IRQ14
32	XI16*	HOST IOCS16*	Drive register enabled
33	HA1	HOST ADDR1	Address bit 1
34	NC	NC	No connection
35	HA0	HOST ADDR0	Address bit 0
36	HA2	HOST ADDR2	Address bit 2
37	HCS0*	HOST CS0*	Reg. access chip select 0
38	HCS1*	HOST CS1*	Reg. access chip select 1
39	NC	NC	No connection
40	Ground	Ground	Ground

J3 – AUXILLARY POWER CONNECTOR

Connector J3 is the auxillary power input used to supply –5V and –12V to the PC/104 Bus and to connector J15. Connect an external power supply to this connector only if you are using a PC/104 module which requires these negative voltages.

Table 15: Auxillary Power Connector Pinout

J3 Pin	Signal Name	Description
1	–5VCC	Power Input
2	Ground	Ground
3	–12VCC	Power Input

J4 – KEYBOARD CONNECTOR

Connector J4 provides a standard PS/2 style keyboard connection. These same signals are available on connector J17 for remote (bulkhead) mounting of a keyboard connector.

Table 16: Keyboard Connector Pinout

J4 Pin	Signal Name	Description
1	KBDATA	Keyboard Data
2	NC	No Connect
3	GND	Ground
4	KBPWR	+5V
5	KBCLK	Keyboard Clock
6	NC	No Connect

J5 – IDE 0 DRIVE ACTIVITY LIGHT CONNECTOR

Connector J5 provides a place to plug in a drive activity light which will indicate when either drive on the primary IDE controller accesses data.

Table 17: IDE 0 Drive Activity Light Connector Pinout

J5 Pin	Signal Name	Description
1	LED–	LED Cathode
2	LED+	LED Anode

J6 – IDE 1 Drive Activity Light Connector

Connector J6 provides a place to plug in a drive activity light which will indicate when either drive on the secondary IDE controller accesses data.

Table 18: IDE 1 Drive Activity Light Connector Pinout

J6 Pin	Signal Name	Description
1	LED–	LED Cathode
2	LED+	LED Anode

J7 – Main Power Connector

Power to the VSBC is supplied through this standard Molex connector.

Table 19: Main Power Connector Pinout

J7 Pin	Signal Name	Description
1	12VCC	+12 Volts
2	GND	Ground
3	GND	Ground
4	5VCC	+5 Volts

J8, J9 – SERIAL PORT CONNECTOR

Connector J8/J9 is a single header which provides signals for two serial I/O ports: COM1 and COM2. COM1 supports RS-232 operation only, and COM2 operates in RS-232 or RS-485 mode.

Table 20: J8, J9 RS-232 Serial Port Connector Pinout

J8, J9 Pin	Signal Name	RS-232 Signal Description	Signal Direction
1	DCD	Data Carrier Detect	In
2	DSR	Data Set Ready	In
3	RXD*	Receive Data	In
4	RTS	Request To Send	Out
5	TXD*	Transmit Data	Out
6	CTS	Clear To Send	In
7	DTR	Data Terminal Ready	Out
8	RI	Ring Indicator	In
9	Ground	Ground	—
10	N/C	—	—

Table 21: J9 RS-422/485 Serial Port Connector Pinout

J9 Pin	Signal Name	RS-422/485 Signal Description	Signal Direction
1	N/C	—	—
2	N/C	—	—
3	TD2+	Transmit Data Pos.	Out
4	TD2–	Transmit Data Neg.	Out
5	N/C	—	—
6	Ground	Ground	—
7	TD2/RD2–	Transmit/Receive Data Neg.	Out/In
8	TD2/RD2+	Transmit/Receive Data Pos.	Out/In
9	N/C	—	—
10	N/C	—	—

J11 – LPT1 Parallel Port Connector

The bi-directional parallel port at J11 can be used as a standard PC/AT compatible LPT1 port or as 17 general purpose TTL I/O signals.

Table 22: LPT1 Parallel Port Pinout

J3 Pin	Centronics Signal	Signal Direction
1	Strobe	Out
2	Auto feed	Out
3	Data bit 1	In/Out
4	Printer error	In
5	Data bit 2	In/Out
6	Reset	Out
7	Data bit 3	In/Out
8	Select input	Out
9	Data bit 4	In/Out
10	Ground	—
11	Data bit 5	In/Out
12	Ground	—
13	Data bit 6	In/Out
14	Ground	—
15	Data bit 7	In/Out
16	Ground	—
17	Data bit 8	In/Out
18	Ground	—
19	Acknowledge	In
20	Ground	—
21	Port Busy	In
22	Ground	—
23	Paper End	In
24	Ground	—
25	Select	In
26	No Connect	—

J12 – FLOPPY DISK DRIVE CONNECTOR

The VSBC CPU board supports a standard 34-pin PC/AT style floppy disk interface at connector J12. Up to two floppy drives can be attached to this port.

Caution Cable length must be 18” or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 23: Floppy Disk Interface Connector Pinout.

J12 Pin	Signal Name	Function
1	Ground	Ground
2	R/LC	Load Head
3	Ground	Ground
4	NC	No Connection
5	Ground	Ground
6	NC	No Connection
7	Ground	Ground
8	INDX*	Beginning Of Track
9	Ground	Ground
10	MTR1*	Motor Enable 1
11	Ground	Ground
12	DRV0*	Drive Select 0
13	Ground	Ground
14	DRE1*	Drive Select 1
15	Ground	Ground
16	MTR0*	Motor Enable 0
17	Ground	Ground
18	DIR	Direction Select
19	Ground	Ground
20	STEP*	Motor Step
21	Ground	Ground
22	WDAT*	Write Data Strobe
23	Ground	Ground
24	WGAT*	Write Enable
25	Ground	Ground
26	TRK0*	Track 0 Indicator
27	Ground	Ground
28	WPRT*	Write Protect
29	Ground	Ground
30	RDAT*	Read Data
31	Ground	Ground
32	HDSL	Head Select
33	Ground	Ground
34	DCHG	Drive Door Open

J13 – INTERRUPT / CIO CHANNEL 3 CONNECTOR

A 14-pin header connector, J13, provides external access to a variety of CIO Channel 3, Digital I/O and Interrupt signals

Table 24: Interrupt Connector Pinout.

J13 Pin	Signal Name	Function
1	PC0	Port C Data 0, Counter/Timer 3 Output
2	Ground	Ground
3	PC1	Port C Data 1, Counter/Timer 3 Count Input
4	Ground	Ground
5	PC2	Port C Data 2, Counter/Timer 3 Trigger Input
6	Ground	Ground
7	PC3	Port C Data 3, Counter/Timer 3 Gate Input
8	Ground	Ground
9	FPI1*	Front Plane Interrupt 1
10	Ground	Ground
11	FPI2*	Front Plane Interrupt 2
12	Ground	Ground
13	FPI3*	Front Plane Interrupt 3
14	Ground	Ground

PC0-PC3 — Port C I/O Lines. These TTL input/output signals are used to as wait and request lines for DIO Ports A and B, to provide external access to DIO Counter/Timer 3, or as four bits of parallel I/O accessed through Port C.

FPI1* — Front Plane 1 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V6[2-3] is inserted, a low level (or high-to-low transition) applied to the FPI1* pin will request an interrupt via IRQ3. In DOS configuration, this will cause an INT 0Bh resulting in a dispatch through the interrupt vector at 000:002Ch.

FPI2* — Front Plane 2 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V5[2-3] is inserted, a low level (or high-to-low transition) applied to the FPI2* pin will request an interrupt via IRQ11. In DOS configuration, this will cause an INT 0Bh resulting in a dispatch through the interrupt vector at 000:002Ch.

FPI3* — Front Plane 3 Interrupt. This TTL input signal is used as a general purpose interrupt request input. If jumper V7[2-3] is inserted, a low level (or high-to-low transition) applied to the FPI3* pin will request an interrupt via IRQ12. In DOS configuration this will cause an INT 74h resulting in a dispatch through the interrupt vector at 0000:01D0h.

J14 – DIGITAL I/O CONNECTOR

A 34-pin interface is included for connection to industry standard Opto 22 I/O racks. The open collector interface is also an excellent choice for general purpose TTL interfacing. A rack power output provides up to 500ma at +5V, and is protected by a self resetting circuit breaker. See chapter 6 for other operating modes.

Table 25: Digital I/O Connector Pinout

J14 Pin	Signal Name	Function
1	PA0	Port A Data 0
2	Ground	Ground
3	PA1	Port A Data 1
4	Ground	Ground
5	PA2	Port A Data 2
6	Ground	Ground
7	PA3	Port A Data 3
8	Ground	Ground
9	PA4	Port A Data 4
10	Ground	Ground
11	PA5	Port A Data 5
12	Ground	Ground
13	PA6	Port A Data 6
14	Ground	Ground
15	PA7	Port A Data 7
16	Ground	Ground
17	PB0	Port B Data 0, Counter/Timer 2 Output
18	Ground	Ground
19	PB1	Port B Data 1, Counter/Timer 2 Count Input
20	Ground	Ground
21	PB2	Port B Data 2, Counter/Timer 2 Trigger Input
22	Ground	Ground
23	PB3	Port B Data 3, Counter/Timer 2 Gate Input
24	Ground	Ground
25	PB4	Port B Data 4, Counter/Timer 1 Output
26	Ground	Ground
27	PB5	Port B Data 5, Counter/Timer 1 Count Input
28	Ground	Ground
29	PB6	Port B Data 6, Counter/Timer 1 Trigger Input
30	Ground	Ground
31	PB7	Port B Data 7, Counter/Timer 1 Gate Input
32	Ground	Ground
33	Power	+5V Rack Power
34	Ground	Ground

PA0-PA7 — Port A Data Lines. These TTL input/output signals transfer information between the CIO Port A and external devices. The signals can be configured as inputs, outputs, tri-state, or open-drain.

PB0-PB7 — Port B Data Lines. These TTL input/output signals transfer information between the CIO Port B and external devices. They may also be used to provide external access to CIO Counter/Timers 1 and 2. The signals can be configured as inputs, outputs, tri-state, or open-drain.

Power — +5V Power Output. When jumper V20 is installed, up to 500 mA can be drawn from this +5V output to power the Opto 22 interface rack or other external equipment. If the I/O rack is powered by a separate external supply, the power jumper on the I/O rack or the V20 jumper must be removed. This output is fused with a resettable polyfuse rated at 1A.

J15 – UTILITY CONNECTOR

Connector J15 is provided for connecting a variety of typical PC switches and indicators including power indicators, a reset switch, and an 8Ω speaker.

Table 26: Utility Connector Pinout.

J15 Pin	Signal Name	Function
1	TIMER 2 OUT	Speaker drive
2	Ground	Ground
3	Ground	Ground
4	Reset	Hardware reset input
5	Ground	Ground
6	LED	Software programmable LED output
7	Ground	Ground
8	12VCC	Voltage output
9	–12VCC	Voltage output
10	–5VCC	Voltage output
11	Ground	Ground
12	SYSRST*	Reset output

J16 – FAN POWER OUTPUT CONNECTOR

Power to a small CPU heatsink cooling fan can be obtained from this connector

Table 27: Fan Power Output Connector Pinout

J16 Pin	Signal Name	Description
1	5VCC	+5 Volts
2	GND	Ground
3	12VCC	+12 Volts

J17 – AUXILLARY KEYBOARD CONNECTOR

For applications where a round keyboard connector must be mounted remotely, J17 provides the same signals available on connector J4.

Table 28: Keyboard connector Pinout

J16 Pin	Signal Name	Description
1	5VCC	+5 Volts
2	GND	Ground
3	12VCC	+12 Volts

Register Descriptions 5

Introduction

This chapter lists all the user-programmable registers on the VSBC CPU board. Programming information is included for VersaLogic specific registers only. Programming information for the standard PC/AT registers can be found in the *The Programmer's PC Sourcebook* or *The Undocumented PC*. Information on the registers internal to the CPU chip can be found in the manufacturer's data book. See the listing in "Other References" on page vii for further information.

Register Summary

The tables in this section list all programmable registers on the VSBC CPU board. They are organized in the following groups:

Table 29: Programmable Registers

DIRECT MEMORY ACCESS — CHANNEL 1

Table 30: DMA 1 Controller Registers

Mnemonic	R/W	Address	Name
DMA0ADRA	R/W	0000h	DMA Channel 0 Current Address
DMA0CNTA	R/W	0001h	DMA Channel 0 Current Word Count
DMA1ADRA	R/W	0002h	DMA Channel 1 Current Address
DMA1CNTA	R/W	0003h	DMA Channel 1 Current Word Count
DMA2ADRA	R/W	0004h	DMA Channel 2 Current Address
DMA2CNTA	R/W	0005h	DMA Channel 2 Current Word Count
DMA3ADRA	R/W	0006h	DMA Channel 3 Current Address
DMA3CNTA	R/W	0007h	DMA Channel 3 Current Word Count
DMACSA	R/W	0008h	DMA Command/Status Register
DMARQA	R/W	0009h	DMA Request Register
DMAMASKA	R/W	000Ah	DMA Single Bit Mask Register
DMAMODEA	R/W	000Bh	DMA Mode Register
DMACBPA	R/W	000Ch	DMA Clear Byte Pointer
DMAMCA	R/W	000Dh	DMA Master Clear
DMACMA	R/W	000Eh	DMA Clear Mask Register
DMAWAMA	R/W	000Fh	DMA Write All Mask Register Bits

DIRECT MEMORY ACCESS — CHANNEL 2

Table 31: DMA 2 Controller Registers

Mnemonic	R/W	Address	Name
DMA0ADRB	R/W	00C0h	DMA Channel 0 Current Address
DMA0CNTB	R/W	00C2h	DMA Channel 0 Current Word Count
DMA1ADRB	R/W	00C4h	DMA Channel 1 Current Address
DMA1CNTB	R/W	00C6h	DMA Channel 1 Current Word Count
DMA2ADRB	R/W	00C8h	DMA Channel 2 Current Address
DMA2CNTB	R/W	00CAh	DMA Channel 2 Current Word Count
DMA3ADRB	R/W	00CCh	DMA Channel 3 Current Address
DMA3CNTB	R/W	00CEh	DMA Channel 3 Current Word Count
DMACSB	R/W	00D0h	DMA Command/Status Register
DMARQB	R/W	00D2h	DMA Request Register
DMAMASKB	R/W	00D4h	DMA Single Bit Mask Register
DMAMODEB	R/W	00D6h	DMA Mode Register
DMACBPB	R/W	00D8h	DMA Clear Byte Pointer
DMAMCB	R/W	00DAh	DMA Master Clear
DMACMB	R/W	00DCh	DMA Clear Mask Register
DMAWAMB	R/W	00DEh	DMA Write All Mask Register Bits
DMAWAXB	R/W	00DFh	DMA Write All Mask Register Bits X

DIRECT MEMORY ACCESS — PAGE REGISTERS

Table 32: DMA Page Registers

Mnemonic	R/W	Address	Name
DMA2PG	W	0081h	DMA Channel 2 Page Register
DMA3PG	W	0082h	DMA Channel 3 Page Register
DMA1PG	W	0083h	DMA Channel 1 Page Register
DMA0PG	W	0087h	DMA Channel 0 Page Register
DMA6PG	W	0089h	DMA Channel 6 Page Register
DMA7PG	W	008Ah	DMA Channel 7 Page Register
DMA5PG	W	008Bh	DMA Channel 5 Page Register
RAPREG	W	008Fh	Refresh Address Page Register

COM1 SERIAL PORT

Table 33: COM1 Serial Port Registers

Mnemonic	R/W	Address	Name
RBRA	R	03F8h	Receiver Buffer Register A
THRA	W	03F8h	Transmit Holding Register A
DLLA	R/W	03F8h	Divisor Latch (LSB) A
IERA	R/W	03F9h	Interrupt Enable Register A
DLMA	R/W	03F9h	Divisor Latch (MSB) A
IIRA	R	03FAh	Interrupt Identification Register A
LCRA	R/W	03FBh	Line Control Register A
MCRA	R/W	03FCh	Modem Control Register A
LSRA	R	03FDh	Line Status Register A
MSRA	R	03FEh	Modem Status Register A
SCRA	R/W	03FFh	Scratchpad Register A

COM2 SERIAL PORT

Table 34: COM2 Serial Port Registers

Mnemonic	R/W	Address	Name
RBRB	R	02F8h	Receiver Buffer Register B
THRB	W	02F8h	Transmit Holding Register B
DLLB	R/W	02F8h	Divisor Latch (LSB) B
IERB	R/W	02F9h	Interrupt Enable Register B
DLMB	R/W	02F9h	Divisor Latch (MSB) B
IIRB	R	02FAh	Interrupt Identification Register B
LCRB	R/W	02FBh	Line Control Register B
MCRB	R/W	02FCh	Modem Control Register B
LSRB	R	02FDh	Line Status Register B
MSRB	R	02FEh	Modem Status Register B
SCRB	R/W	02FFh	Scratchpad Register B

LPT1 PARALLEL PORT

Table 35: LPT1 Parallel Port Registers

Mnemonic	R/W	Address	Name
LPRD	R	03BCh	Line Printer Read Data Register
LPWD	W	03BCh	Line Printer Write Data Register
LPS	R	03BDh	Line Printer Status Register
LPRC	R	03BEh	Line Printer Read Control Register
LPWC	W	03BEh	Line Printer Write Control Register

CIO CONFIGURATION REGISTERS

Table 36: CIO Configuration Registers

Mnemonic	R/W	Address	Name
CIOCONTROL	R/W	00E4h	Control Port
CIOPORTA	R/W	00E5h	Port A Data Port
CIOPORTB	R/W	00E6h	Port B Data Port
CIOPORTC	R/W	00E7h	Port C Data Port

SIO CONFIGURATION REGISTERS

Table 37: SIO Configuration Registers

Mnemonic	R/W	Address	Name
SIOINDEX	W	03F0h	Internal Register Index
SIODATA	R/W	03F1h	Internal Register Data

FLOPPY DISK DRIVE CONTROLLER

Table 39: Floppy Disk Drive Controller Registers

Mnemonic	R/W	Address	Name
FDCMSR	R	03F4h	Main Status Register
FDCDR	R/W	03F5h	Data Register
FDCST0	R	03F5h	Status Register 0
FDCST1	R	03F5h	Status Register 1
FDCST2	R	03F5h	Status Register 2
FDCST3	R	03F5h	Status Register 3
FDCDCR	W	03F2h	Drive Control Register
FDCDRR	W	03F7h	Data Rate Register
FDCFDR	R	03F7h	Fixed Disk Register

IDE HARD DISK DRIVE CONTROLLER

Table 40: IDE Hard Disk Drive Controller Registers

Mnemonic	R/W	Address	Name
IDEDR	R/W	01F0h	Data Register
IDEER	R	01F1h	Error Register
IDEWP	W	01F1h	Write Precompensation Register
IDESC	R/W	01F2h	Sector Count Register
IDESN	R/W	01F3h	Sector Number Register
IDECNL	R/W	01F4h	Cylinder Number Register Low
IDECNH	R/W	01F5h	Cylinder Number Register High
IDEDH	R/W	01F6h	Drive/Head Register
IDEST	R	01F7h	Status Register
IDECMD	W	01F7h	Command Register
IDEDIR	R	03F7h	Digital Input Register
IDEFDR	W	03F6h	Fixed Disk Register

INTERRUPT CONTROLLER — MASTER

Table 41: Master Interrupt Controller Registers

Mnemonic	R/W	Address	Name
ICW1A	W	0020h	Initialization Command Word 1
ICW2A	W	0021h	Initialization Command Word 2
ICW3A	W	0021h	Initialization Command Word 3
ICW4A	W	0021h	Initialization Command Word 4
OCW1A	W	0021h	Operation Command Word 1 (Interrupt Mask)
OCW2A	W	0020h	Operation Command Word 2 (Priority & Finish Control)
OCW3A	W	0020h	Operation Command Word 3 (Mode Control)
ISRA	R	0020h	In-Service Register
IRRA	R	0020h	Interrupt Request Register
IPWA	R	0020h	Interrupt Poll Word
IMRA	R	0021h	Interrupt Mask Register

INTERRUPT CONTROLLER — SLAVE

Table 42: Slave Interrupt Controller Registers

Mnemonic	R/W	Address	Name
ICW1B	W	00A0h	Initialization Command Word 1
ICW2B	W	00A1h	Initialization Command Word 2
ICW3B	W	00A1h	Initialization Command Word 3
ICW4B	W	00A1h	Initialization Command Word 4
OCW1B	W	00A1h	Operation Command Word 1 (Interrupt Mask)
OCW2B	W	00A0h	Operation Command Word 2 (Priority & Finish Control)
OCW3B	W	00A0h	Operation Command Word 3 (Mode Control)
ISRB	R	00A0h	In-Service Register
IRRB	R	00A0h	Interrupt Request Register
IPWB	R	00A0h	Interrupt Poll Word
IMRB	R	00A1h	Interrupt Mask Register

COUNTER/TIMERS

Table 43: Counter / Timer Registers

Mnemonic	R/W	Address	Name
T0CNT	R/W	0040h	Timer 0 Count Load/Read
T1CNT	R/W	0041h	Timer 1 Count Load/Read
T2CNT	R/W	0042h	Timer 2 Count Load/Read
TCW	W	0043h	Timer Control Word

MISCELLANEOUS

Table 44: Miscellaneous PC/AT-Style Registers

Mnemonic	R/W	Address	Name
CSP	R/W	0061h	Control/Status Port
RTCIDX	W	0070h	Real Time Clock Index and NMI Mask
RTCDP	R/W	0071h	Real Time Clock Data Port

SPECIAL CONTROL REGISTER

SCR (READ/WRITE) 00E0H

D7	D6	D5	D4	D3	D2	D1	D0
LED	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WDOGEN

Table 45: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	LED	**Light Emitting Diode** — Controls the LED circuit on connector J15 LED = 0 Turns LED off. LED = 1 Turns LED on.
D6	—	**Reserved** — This bit has no function. Always reads as 0.
D5	—	**Reserved** — This bit has no function. Always reads as 0.
D4	—	**Reserved** — This bit has no function. Always reads as 0.
D3	—	**Reserved** — This bit has no function. Always reads as 0.
D2	—	**Reserved** — This bit has no function. Always reads as 0.
D1	—	**Reserved** — This bit has no function. Always reads as 0.
D0	WDOGEN	**Watchdog Enable** — Enables and disables the watchdog timer reset circuit. WDOGEN = 0 Disables the watchdog timer. WDOGEN = 1 Enables the watchdog timer.

WATCHDOG TIMER HOLD-OFF REGISTER

WDHOLD (WRITE ONLY) 00E1H

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the CPU board to reset the CPU if proper software execution fails or a hardware malfunction occurs. The watchdog timer is enabled/disabled by writing to bit D0 of SCR

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms). Writing a 5Ah to WDHOLD resets the watchdog timeout period, preventing the CPU from being reset for the next 250 ms.

MAP AND PAGING CONTROL REGISTER

MPCR (READ/WRITE) 00E3H

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	FPAGE	RPG4	RPG3	RPG2	RPG1	RPG0

Table 46: Map and Paging Control Register Bit Assignments

Bit	Mnemonic	Description
D7	—	**Reserved** — This bit has no function. Always reads as 0.
D6	—	**Reserved** — This bit has no function. Always reads as 0.
D5	FPAGE	**Flash Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the on-board ROM. FPAGE = 0 ROM Page Frame Disabled. FPAGE = 1 ROM Page Frame Enabled.
D4-D0	RPG4-RPG0	**ROM Page Select 4-0** — Selects which 64K block of ROM will be mapped into the ROM page frame.

RPG4	RPG3	RPG2	RPG1	RPG0	ROM Memory Range
0	0	0	0	0	000000h to 00FFFFh
0	0	0	0	1	010000h to 01FFFFh
0	0	0	1	0	020000h to 02FFFFh
0	0	0	1	1	030000h to 03FFFFh
0	0	1	0	0	040000h to 04FFFFh
0	0	1	0	1	050000h to 05FFFFh
0	0	1	1	0	060000h to 06FFFFh
0	0	1	1	1	070000h to 07FFFFh
0	1	0	0	0	080000h to 08FFFFh
0	1	0	0	1	090000h to 09FFFFh
0	1	0	1	0	0A0000h to 0AFFFFh
0	1	0	1	1	0B0000h to 0BFFFFh
0	1	1	0	0	0C0000h to 0CFFFFh
0	1	1	0	1	0D0000h to 0DFFFFh
0	1	1	1	0	0E0000h to 0EFFFFh
0	1	1	1	1	0F0000h to 0FFFFFh
1	0	0	0	0	100000h to 10FFFFh
1	0	0	0	1	110000h to 11FFFFh
1	0	0	1	0	120000h to 12FFFFh
1	0	0	1	1	130000h to 13FFFFh
1	0	1	0	0	140000h to 14FFFFh
1	0	1	0	1	150000h to 15FFFFh
1	0	1	1	0	160000h to 16FFFFh
1	0	1	1	1	170000h to 17FFFFh
1	1	0	0	0	180000h to 18FFFFh
1	1	0	0	1	190000h to 19FFFFh
1	1	0	1	0	1A0000h to 1AFFFFh
1	1	0	1	1	1B0000h to 1BFFFFh
1	1	1	0	0	1C0000h to 1CFFFFh
1	1	1	0	1	1D0000h to 1DFFFFh
1	1	1	1	0	1E0000h to 1EFFFFh
1	1	1	1	1	1F0000h to 1FFFFFh

CIO Chip 6

Introduction

The CIO Counter/Timer and Parallel I/O device is a general-purpose peripheral circuit that satisfies most counter/timer and parallel I/O needs encountered in system design, and is therefore helpful in real-time situations and for interrupt control.

Note The text in this section has been copied directly from the Zilog Technical Manual. Several functions on the CIO chip are not implemented at the hardware level on the VSBC, and some functions are not supported by VersaLogic. The table below describes these exceptions:

Non Supported Function	Notes
Hardware Interrupt Vectoring	Several conditions within the CIO chip can generate interrupts. These interrupts are sent to the VSBC interrupt controller on IRQ15 (via jumper V8[2-3]). In DOS configuration, this causes an INT 77h resulting in a dispatch through the interrupt vector at 0000:01DCh. To maintain IBM/AT interrupt compatibility, CIO generated hardware interrupt vectors are not implemented. Fortunately, the vector can be read from the Current Interrupt Vector register to help determine the source of the interrupt. All actions associated with an interrupt acknowledge cycle occur when an IP bit is cleared by writing to one of the Command and Status registers. A code example is provided on page 105 which illustrates this process.
Handshaking Port Operation	This function is operational without restriction, however it is not fully documented in this manual. Please consult the Zilog Technical Manual if you are interested in this feature.

FEATURES

The CIO device satisfies a wide range of applications because of its extensive list of features:

- Two independent 8-bit, double-buffered, bi-directional I/O ports, plus a 4-bit special-purpose I/O ports. The I/O ports feature programmable polarity, programmable direction (Bit mode), 1's catchers, and programmable open drain outputs.
- Flexible pattern-recognition logic, programmable as a 16-vector interrupt controller.
- Three independent 16-bit counter/timers, each with three output duty cycles (pulsed, one-shot, and square-wave) and up to four external access lines per channel (count input, output, gate, and trigger). The counter/timers are programmable as retriggerable or non-retriggerable.
- Registers are accessed in two steps using an Index register.

OVERVIEW

The CIO consists of three I/O ports (two general-purpose 8-bit ports and one special purpose 4-bit port), three 16-bit counter/timers, and an interrupt control logic block. A large number of programmable options allow you to tailor the configuration to suit specific applications.

I/O PORTS

There are three I/O ports: two general-purpose 8-bit ports (which are linkable into one 16-bit port), and one special-purpose 4-bit port.

PORTS A AND B

The two general-purpose 8-bit I/O ports, Ports A and B, are identical, except that Port B can be programmed to provide external access to Counter/Timers 1 and 2. Either port can be programmed to be a control port with the direction of each bit individually programmable.

Both ports include pattern-recognition logic, which allows interrupt generation when a specific pattern is detected. The reference pattern for the pattern-recognition logic is specified by the contents of three registers: the Pattern Polarity register, Pattern Transition register, and Pattern Mask register. The detailed characteristics of each bit path (for example, the direction of data flow or whether a path is inverting or non-inverting) are programmed using the Data Path Polarity register, Data Direction register, and Special I/O Control register.

For each port, the primary control and status bits are grouped in a single register, the Command and Status register. After the port is configured, this is the only register that needs to be accessed frequently. To facilitate initialization, the port logic is designed so that registers associated with an unrequired capability are ignored and do not have to be programmed.

PORT C

All bits on Port C can be used as parallel I/O lines or as Counter/Timer 3 signals.

Only the three bit path registers are needed: the Data Path Polarity register, the Data Direction register, and the special I/O Control register.

COUNTER/TIMERS

The three counter/timers are all identical. Each is composed of a 16-bit down-counter, a 16-bit Time Constant register (which holds the value loaded into the down-counter), a 16-bit Current Counter register (used to read the contents of the down-counter), and 8-bit registers for control and status (the Mode Specification and the C/T Command and Status registers).

Control signals for each counter/timer channel are available on connectors J13 and J14 (counter input, gate input, trigger input, and counter/timer output.) Three different counter/timer output duty cycles are available: pulse, one-shot, and square-wave. The operation of the counter/timers can be programmed independently as either retriggerable or non-retriggerable.

INTERRUPT CONTROL LOGIC

There are five registers (the Master Interrupt Control register, the Current Vector register, and the three Interrupt Vector registers) associated with the interrupt logic. In addition, each port and Counter/Timer Command and Status register includes three bits associated with the interrupt logic: Interrupt Pending (IP), Interrupt Under Service (IUS), and Interrupt Enable (IE).

Register Description

INTRODUCTION

This chapter provides brief description of the command, status and data registers contained in the CIO. Each description includes the register address, the operation of the individual bits, and the state of the register after a reset (hardware or software).

For simplicity, the descriptions assume that the data path polarity of each bit is programmed to be non-inverting.

CIO REGISTERS

Mnemonic	R/W	Index	Name	Page
CIOMIC	R/W	00h	Master Interrupt Control	74
CIOMCC	R/W	01h	Master Configuration Control	76
CIOAIV	R/W	02h	Port A Interrupt Vector	92
CIOBIV	R/W	03h	Port B Interrupt Vector	92
CIOCTIV	R/W	04h	Counter/Timer Interrupt Vector	92
CIOCDPP	R/W	05h	Port C Data Path Polarity	82
CIOCDD	R/W	06h	Port C Data Direction	83
CIOCSIC	R/W	07h	Port C Special I/O Control	83
CIOACS	R/W	08h	Port A Command and Status	80
CIOBCS	R/W	09h	Port B Command and Status	80
CIOCT1CS	R/W	0Ah	Counter/Timer 1 Command and Status	89
CIOCT2CS	R/W	0Bh	Counter/Timer 2 Command and Status	89
CIOCT3CS	R/W	0Ch	Counter/Timer 3 Command and Status	89
CIOPORTA	R/W	0Dh	Port A Data	86
CIOPORTB	R/W	0Eh	Port B Data	86
CIOPORTC	R/W	0Fh	Port C Data	87
CIOCT1CCM	R	10h	Counter/Timer 1 Current Count MS Byte	92
CIOCT1CCL	R	11h	Counter/Timer 1 Current Count LS Byte	92
CIOCT2CCM	R	12h	Counter/Timer 2 Current Count MS Byte	92
CIOCT2CCL	R	13h	Counter/Timer 2 Current Count LS Byte	92
CIOCT3CCM	R	14h	Counter/Timer 3 Current Count MS Byte	92
CIOCT3CCL	R	15h	Counter/Timer 3 Current Count LS Byte	92
CIOCT1TCM	R/W	16h	Counter/Timer 1 Time Constant MS Byte	91
CIOCT1TCL	R/W	17h	Counter/Timer 1 Time Constant LS Byte	91
CIOCT2TCM	R/W	18h	Counter/Timer 2 Time Constant MS Byte	91
CIOCT2TCL	R/W	19h	Counter/Timer 2 Time Constant LS Byte	91
CIOCT3TCM	R/W	1Ah	Counter/Timer 3 Time Constant MS Byte	91
CIOCT3TCL	R/W	1Bh	Counter/Timer 3 Time Constant LS Byte	91
CIOCT1MS	R/W	1Ch	Counter/Timer 1 Mode Specification	87
CIOCT2MS	R/W	1Dh	Counter/Timer 2 Mode Specification	87
CIOCT3MS	R/W	1Eh	Counter/Timer 3 Mode Specification	87
CIOCV	R	1Fh	Current Vector	93
CIOAMS	R/W	20h	Port A Mode Specification	78
CIOAHS	R/W	21h	Port A Handshake Specification	80
CIOADPP	R/W	22h	Port A Data Path Polarity	82
CIOADD	R/W	23h	Port A Data Direction	83
CIOASIC	R/W	24h	Port A Special I/O Control	83
CIOAPP	R/W	25h	Port A Pattern Polarity	85
CIOAPT	R/W	26h	Port A Pattern Transition	85
CIOAPM	R/W	27h	Port A Pattern Mask	85
CIOBMS	R/W	28h	Port B Mode Specification	78
CIOBHS	R/W	29h	Port B Handshake Specification	80
CIOBDPP	R/W	2Ah	Port B Data Path Polarity	82
CIOBDD	R/W	2Bh	Port B Data Direction	83
CIOBSIC	R/W	2Ch	Port B Special I/O Control	83
CIOBPP	R/W	2Dh	Port B Pattern Polarity	85
CIOBPT	R/W	2Eh	Port B Pattern Transition	85
CIOBPM	R/W	2Fh	Port B Pattern Mask	85

REGISTER ACCESS

The registers in the CIO chip are accessed in a two-step sequence:

1. Write the register index value to the Control port (00E7h)
2. Read or write the register data from/to the Control port (00E7h)

Since only one I/O port is used, internal logic must decide if data is meant for the Index register or an internal control register. Direct accesses of the data registers has no effect on the indexing mechanism.

STATE 0

- Data written to the Control port (00E7h) goes to the Index register. The logic switches to state 1.
- Data read from the Control port (00E7h) comes from the Index register. The logic remains in state 0.

STATE 1

- Data written to the Control port (00E7h) goes to the internal control register pointed to by the Index register. The logic reverts back to state 0.
- Data read from the Control port (00E7h) comes from the internal control register pointed to by the Index register. The logic reverts back to state 0.

For example, to read the Current Vector register:

```
OUTPUT   00E7h,1Fh   ;Write 1Fh to the Index register
INPUT    00E7h       ;Read the value of the Current Vector register
```

In state 1, many internal operations are suspended, Interrupt Pending (IP) cannot be set, and internal status is frozen. Therefore, to minimize interrupt latency and to allow continuous status updates, the CIO chip should not be left in State 1.

All data access must be performed as a two byte transaction. The data registers for Ports A, B, and C can be accessed using this indexed method, however, for higher throughput, the data registers can be directly addressed using the following I/O port addresses:

Table 47: Port A/B/C Direct Access Addresses

Register	Address
Port A Data Port	00E6h
Port B Data Port	00E5h
Port C Data Port	00E4h

Master Control Registers

The master control registers consist of the Master Interrupt Control register and Master Configuration Control register. These registers provide primary controls for the interrupt logic, port and counter/timer enable bits, port and counter/timer link bits and the RESET bit.

MASTER INTERRUPT CONTROL REGISTER

CIOMIC (READ/WRITE) 00H

D7	D6	D5	D4	D3	D2	D1	D0
MIE	DLC	NV	PAVIS	PBVIS	CTVIS	1	RESET

The Master Interrupt Control register contains the primary control bits for the interrupt control logic. When the CIO chip is reset, all bits in all device registers are forced to 0 except RESET, which is set to 1. All bits in the Master Interrupt Control register are Read/Write.

Table 48: Master Interrupt Control Register Bit Assignments

Bit	Mnemonic	Description
D7	MIE	**Master Interrupt Enable** — Provides a method to disable all interrupts. MIE also affects whether or not status is included when reading interrupt vectors. MIE = 0 — Inhibits the CIO from generating interrupts. Vector reads do not include status. MIE = 1 — Allows interrupt logic to operate normally. Vector reads always include status, independent of the state of the corresponding Vector Includes Status (VIS) bit.
D6	DLC	**Disable Lower Chain** — Daisy chain (interrupt) control bit. Since the daisy-chain is not implemented on the VSBC card, this bit has no effect. DLC = 0 — IEO operates normally. DLC = 1 — Interrupt Enable Out (IEO) output is forced Low, disabling interrupts from all lower-priority devices on the daisy-chain.
D5	NV	**No Vector** — Inhibits hardware vector generation during interrupt acknowledge cycle. Since CIO generated hardware interrupt vectors are not implemented on the VSBC, this bit should be set to 1 for normal operation. NV = 0 — If NV is written with 0, the interrupt vector is output as usual. NV = 1 — Interrupt vector disabled during an Interrupt Acknowledge cycle. This allows the vector to be provided by external hardware. It has no effect on the setting of the Interrupt Under Service (IUS) bit.
D4	PAVIS	**Port A Vector Includes Status** — Controls whether or not status information is included in the Port A interrupt vector. PAVIS = 0 — The value returned from the Port A Interrupt Vector register (CIOAIV) is constant. The data always reflects the value written to the Port A Base Interrupt Vector register. PAVIS = 1 — The value returned from the Port A Interrupt Vector register is variable. Vector is modified to include status, which indicates the cause of the interrupt. The state of this bit has no effect on the value returned when the Port A Interrupt Vector is register is read. When reading the vector, the MIE bit determines if status is included in the vector, (that is, no status is included if MIE = 0). See page 102 for further information.
D3	PBVIS	**Port B Vector Includes Status** — Controls whether or not status information is included in the Port B interrupt vector. This bit operates the same way that PAVIS does. See text above for details.
D2	CTVIS	**Counter/Timer Vector Includes Status** — Controls whether or not status information is included in the Counter/Timer vector. This bit operates the same way that PAVIS does. See text above for details.
D1	1	**Reserved** — This bit has no function. Always reads as 1.
D0	RESET	**Reset** — Resets the CIO chip. RESET = 1 — Places the CIO chip into a reset condition. Reads from all other registers will return 0 and writes to other registers are ignored. Refer to page 103 for further information. RESET = 0 — Normal operation

MASTER CONFIGURATION CONTROL REGISTER

CIOMCC (READ/WRITE) 01H

D7	D6	D5	D4	D3	D2	D1	D0
PBE	CT1E	CT2E	PCECT3E	PLC	PAE	LC1	LC0

The Master Configuration Control register contains the control bits used to enable different sections of the device after they are initially configured, as well as the bits used to link the ports together and the timers together. All bits are cleared to 0 by resetting the device. The register is read/write.

Table 49: Master Configuration Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PBE	**Port B Enable** — This bit allows Port B to be configured initially without setting its IP erroneously or having its I/O lines go low-impedance until it is safe to do so. PBE = 0 — Inhibits the Port B logic from issuing an interrupt request (its IP cannot be set); however, if IP was already set, clearing PBE inhibits READY/WAIT assertion, holds all1's catchers in a transparent condition, and forces the Port B I/O lines into a high-impedance state. PBE = 1 — Allows Port B to operate normally
D6	CT1E	**Counter/Timer 1 Enable** — Controls counter/timer 1. CT1E = 0 — Counter/Timer 1 is put into an initialized state: its IP cannot be set (however, if IP was already set, clearing CT1E does not clear IP), the Count In Progress (CIP) flag is cleared, Read Counter Control (RCC) is forced to 0, and all trigger inputs are ignored. CT1E = 1 — Counter/timer 1 functions normally.
D5	CT2E	**Counter/Timer 2 Enable** — Controls counter/timer 2. CT2E = 0 — Counter/Timer 2 is put into an initialized state: its IP cannot be set (however, if IP was already set, clearing CT1E does not clear IP), the Count In Progress (CIP) flag is cleared, Read Counter Control (RCC) is forced to 0, and all trigger inputs are ignored. CT2E = 1 — Counter/timer 2 functions normally.

Table 50: Master Configuration Control Register (Continued)

Bit	Mnemonic	Description
D4	PCECT3E	**Port C and Counter/Timer 3 Enable** — This bit enables both Port C and Counter/Timer 3. PCECT3E = 0 — Counter/Timer 3 is put into an initialized state: its IP cannot be set (however, if IP was already set, clearing CT1E does not clear IP), the Count In Progress (CIP) flag is cleared, Read Counter Control (RCC) is forced to 0, and all trigger inputs are ignored. Handshake logic for Ports A and B is forced into an idle state and the internal Acknowledge Input (ACKIN) signal is forced High. This allows the start-up of handshake operations to be precisely controlled. Inhibits Port C logic from issuing an interrupt request (its IP cannot be set); however, if IP was already set, clearing PBE inhibits READY/WAIT assertion, holds all1's catchers in a transparent condition, and forces the Port C I/O lines into a high-impedance state. PCECT3E = 1 — Counter/timer 3 and Port C function normally.
D3	PLC	**Port Link Control** — Unsupported. PLC = 0 — Ports A and B operate as two independent 8-bit ports. PLC = 1 — Unsupported
D2	PAE	**Port A Enable** — This bit allows Port A to be configured initially without setting its IP erroneously or having its I/O lines go low-impedance until it is safe to do so. PAE = 0 — Inhibits the Port A logic from issuing an interrupt request (its IP cannot be set); however, if IP was already set, clearing PBE inhibits READY/WAIT assertion, holds all 1's catchers in a transparent condition, and forces the Port A I/O lines into a high-impedance state. PAE = 1 — Allows Port A to operate normally
D1-D0	LC1-LC0	**Counter/Timer Link Controls** — These two bits specify if and how Counter/Timers 1 and 2 are linked. The Counter/Timers must be linked before they are enabled. **LC1 LC0 Mode** 0 0 Counter/Timers are independent 0 1 Counter/Timer 1's output (inverted) gates Counter/Timer 2 1 0 Counter/Timer 1's output (inverted) triggers Counter/Timer 2 1 1 Counter/Timer 1's output (inverted) is Counter/Timer 2's count input

PORT MODE SPECIFICATION REGISTER

CIOBMS (READ/WRITE) 20H
CIOAMS (READ/WRITE) 28H

D7	D6	D5	D4	D3	D2	D1	D0
PTS1	PTS0	ITB	SB	IMO	PMS1	PMS0	LPM/DTE

Each port Mode Specification register contains the bits that define the operating mode of its port and specify the operation of pattern match logic of the port. A reset forces all bits to 0.

Table 51: Port Mode Specification Register Bit Assignments

Bit	Mnemonic	Description
D7-D6	PTS1-PTS0	**Port Type Selects** — Unsupported. **PTS1 PTS0 Port Types** 0 0 Bit Port (no handshake) 0 1 Unsupported 1 0 Unsupported 1 1 Unsupported
D5	ITB	**Interrupt on Two Bytes** — Unsupported. ITB = 0 Normal operation. ITB = 1 Unsupported
D4	SB	**Single Buffer** — Unsupported. SB = 0 Normal operation SB = 1 Unsupported
D3	IMO	**Interrupt on Match Only** — Unsupported. IMO = 0 Normal operation IMO = 1 Unsupported
D2-D1	PMS1-PMS0	**Pattern Mode Specification Bits** — These two bits define the mode of operation of the pattern of match logic. **PMS1 PMS0 Pattern Mode** 0 0 Disable Pattern Match 0 1 AND Mode 1 0 OR Mode 1 1 OR-Priority Encoded Vector mode. The OR-Priority Encoded Vector mode must not be specified for ports configured as bit ports with the Latch on Pattern Match (LPM) bit set to 1 or for ports with handshake.
D0	LPM/DTE	**Latch On Pattern Match/Deskew Timer Enable** — This bit is a dual-function bit. The LPM function is active when the port is specified in bit mode. It must be cleared to 0 for input ports with handshake or for bit ports whose pattern match logic is in the OR-Priority Encoded Vector mode. LPM = 0 Pattern matches are still detected, but the data read back from the port follows the port pins. LPM = 1 Causes the port to latch the input data present at the port when a pattern match is detected. DTE = 0 Not supported. DTE = 1 Not supported.

Port Handshake Specification Registers

PORT A/B HANDSHAKE SPECIFICATION REGISTERS

CIOAHS (READ/WRITE) 28H
CIOBHS (READ/WRITE) 29H

D7	D6	D5	D4	D3	D2	D1	D0
HTS1	HTS0	RWS2	RWS1	RWS0	DTS3	DTS2	DTS1

Port handshake mode is not supported. All bits must be remain in their reset state (0).

PORT COMMAND AND STATUS REGISTERS

CIOACS (READ/PARTIAL WRITE) 08H
CIOBCS (READ/PARTIAL WRITE) 09H

D7	D6	D5	D4	D3	D2	D1	D0
IUS/ICB2	IE/ICB1	IP/ICB0	ERR	ORE	IRF	PMF	IOE

Each of these registers contain the primary command and status bits for its port. Other than the data bits themselves, these are the bits most often accessed in normal port operation. A reset forces ORE to 1 and all other bits to 0. All bits are readable and four are writable.

Table 52: Register Bit Assignments

Bit	Mnemonic	Description
D7 (Read)	IUS	**Interrupt Under Service** — This status bit is automatically set to 1 if its corresponding IP is the highest-priority interrupt request pending when an Interrupt Acknowledge sequence takes place. It can also be set directly by CPU command. The same and lower priority sources of interrupt are prohibited from requesting interrupts via the internal and external daisy-chains. The IUS can be cleared to 0 only by CPU command. This bit is read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D6 (Read)	IE	**Interrupt Enable** — This bit enables or disables the port's interrupt logic. While IE is cleared to 0, the port is unable to request an interrupt or to respond to an Interrupt Acknowledge. The normal operation of IP or IUS is not affected, the IP is simply masked off from the rest of the device. A 1 in IUS still affects the interrupt daisy-chain. If IE is programmed to be 1, the interrupt logic operates normally. This is bit read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D5 (Read)	IP	**Interrupt Pending** — IP is a status bit which, when set to 1, indicates that the port requires servicing due to a pattern match, a handshake, or an error. It is set to1 by the port logic (or by the CPU command). If IE is also 1 and no higher-priority interrupts are under service, then the INT line is pulled Low to request an interrupt. It is cleared to 0 either automatically or by a CPU command, depending on port configuration. This is bit read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D7-D5 (Write)	ICB2-ICB0	**Interrupt Command Bits** — These three bits control the port IP, IUS, and IE bits. **ICB2 ICB1 ICB0 Function** 0 0 0 Null Code 0 0 1 Clear IP and IUS 0 1 0 Set IUS 0 1 1 Clear IUS 1 0 0 Set IP 1 0 1 Clear IP 1 1 0 Set IE 1 1 1 Clear IE
D4 (Read)	ERR	**Interrupt Error** — This status bit is automatically set to 1 along with IP when, for a bit port with pattern match enabled, a second match occurs before a previous match is acknowledged (IP is still set). If the port Interrupt On Error (IOE) bit is 0, errors are ignored and this bit is held at 0. This bit can be cleared only by clearing the corresponding IP. This bit is a read-only bit; writes to it are ignored.
D3 (Read)	ORE	**Output Data Register Empty** — ORE is a status bit. It is forced to 1 unless OR-PEV pattern match mode is specified--in which case, ORE is forced to 0. This bit is a read-only bit; writes to it are ignored. RESET forces ORE to 1.

D2 (Read)	IRF	**Input Data Register Full** — IRF is a status bit used in conjunction port handshaking (an unsupported mode.) In normal operation, IRF is forced to 1. IRF is a read-only bit; writes to it are ignored.
D1 (Read)	PMF	**Pattern Match Flag** — The PMF is a status bit set to 1 when a pattern match is detected. If the port is a bit port, PMF is not latched. It reflects the state of the pattern match logic just before it is read. This bit is updated every second PCLK cycle while the CIO is in State 0. If the port pattern match logic is not enabled (PMS1 = PMS0 = 0), PMF is forced to 0. This is a read-only bit. Writes to it are ignored.
D0 (Read/ Write)	IOE	**Interrupt on Error** — While IOE is cleared to 0, error conditions in bit ports using pattern-recognition logic (a second match before a previous match is acknowledged) are ignored. However, if IOE is 1, such errors will cause IP to be set and will halt normal operation of the port until the error condition is dealt with.

Bit Path Definition Registers

The Bit Path Definition registers are used to specify the details of each bit path of each port. They define:

- whether a bit path in inverting or non-inverting
- if an output is normal or open-drain
- if a bit port input has a 1's catcher inserted in its path
- which direction the data is flowing for each bit of a bit port.

Each port has a set of these registers. The four most significant bits of each register do not exist in the registers associated with Port C (writes are ignored, reads return 1s).

DATA PATH POLARITY REGISTERS

CIOADPP (READ/WRITE) 22H
CIOBDPP (READ/WRITE) 2AH
CIOCDPP (READ/WRITE) 05H

D7	D6	D5	D4	D3	D2	D1	D0
DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0

The Data Path Polarity registers each define whether the bits in its port are inverting or non-inverting on a bit-by-bit basis.

Table 53: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	DP7-DP0	A 0 in a particular bit position of this register specifies the corresponding bit path of the port as non-inverting (that is, a High level at the port pin is 1). If a bit in this register is written with 1, the data path is programmed inverting (that is, a Low level at the pin is 1). A reset clears all bits to 0 (the port is non-inverting). The bits are read/write. Only the four LSB's of Port C are affected.

DATA DIRECTION REGISTERS

CIOADD (READ/WRITE) 23H
CIOBDD (READ/WRITE) 2BH
CIOCDD (READ/WRITE) 06H

D7	D6	D5	D4	D3	D2	D1	D0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Each of the Data Direction registers define the direction of data flow for the individual bits of its port if configured as a bit port.

Table 54: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	DD7-DD0	A 0 in a bit position of this register specifies the corresponding bit of the port as an output bit, while a 1 specifies it as an input. An input bit specification is overridden for bits in Port C used as outputs for handshake signals or REQUEST/WAIT line. A reset forces all bits in these registers to 0. All bits are read/write.

SPECIAL I/O CONTROL REGISTERS

CIOASIC (READ/WRITE) 24H
CIOBSIC (READ/WRITE) 2CH
CIOCSIC (READ/WRITE) 07H

D7	D6	D5	D4	D3	D2	D1	D0
SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Each of the Special I/O Control registers is a dual-function register which specifies special characteristics about its port's data path. Its exact function depends on the direction of data flow defined for the path.

Table 55: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	SC7-SC0	If a bit is an input bit, a 1 in this register's corresponding bit position invokes a 1's catcher. A 1's catcher functions automatically latching a 1 if its input goes to 1. It is cleared only by writing a 0 to the Input Data register. A 1's catcher is inserted into the input path after the bit's invert/non-invert logic. If the bit is programmed 0, it is a normal input bit. The 1's catcher is available only for input bit port bits. If a bit is an output bit, a 0 in the corresponding bit position of this register specifies the output as a normal output with both a pull-up and a pull-down transistor. A 1 in this register defined the output as open-drain; no pull-up transistor is provided. The value programmed in this register applies to all output modes, independent of utilization. A reset forces all bits to 0. All bits are read/write.

Pattern Definition Registers

These registers collectively specify the match pattern for the port. As the registers must be taken together to define the pattern, they are described differently than the previous registers. A reset forces all of these registers to 0. All are read/write.

PATTERN POLARITY REGISTER

CIOAPP (READ/WRITE) 25H
CIOBPP (READ/WRITE) 2DH

D7	D6	D5	D4	D3	D2	D1	D0
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

PATTERN TRANSITION REGISTER

CIOAPT (READ/WRITE) 26H
CIOBPT (READ/WRITE) 2EH

D7	D6	D5	D4	D3	D2	D1	D0
PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0

PATTERN MASK REGISTER

CIOAPM (READ/WRITE) 27H
CIOBPM (READ/WRITE) 2FH

D7	D6	D5	D4	D3	D2	D1	D0
PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

The pattern specified by the Pattern Definition registers is a logical (not a physical) specification--this concept is important in understanding the interaction between the pattern match logic and the invert/non-invert logic. An example which shows the logical (as opposed to the physical) nature of the specification is: a High level (VCC) on an input pin programmed as inverting matches a 0 specification. Similarly, an output written with a 1 matches a 1 specification even if it is programmed inverting and the output pin is at a low voltage level.

Table 56: Pattern Specification Definition

Mask Register	Transition Register	Polarity Register	Pattern Specification
0	0	0	Bit Masked Off (X)
0	1	0	Any Transition (↗ or ↘)
1	0	0	Zero (0)
1	0	1	One (1)
1	1	0	One to Zero Transition (↘)
1	1	1	Zero to One Transition (↗)

If the pattern match mode is OR-Priority Encoded Vector, the transition detection patterns should not be specified (PTn should be set to 0). If the AND mode is specified, no more than one bit should be specified to detect transitions.

PORT A AND B DATA REGISTERS

CIOPORTA (READ/WRITE) 0DH (also directly accessible at I/O Port 00E6h)
CIOPORTB (READ/WRITE) 0EH (also directly accessible at I/O Port 00E5h)

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Ports A and B each have a data path that is composed of three registers: an Input Data register, an Output Data register, and a Buffer register. Output data written to the data register is stored in the Output Data register. Reading the data register returns the contents of the Input Data register. The buffer register is used to buffer the input and output data if the port is configured as a port with handshake. If so enabled, it is used by the bit port to latch data when a pattern match is detected.

The individual bits of the port data registers map directly onto the port I/O pins (bit 0 of the Port A Data register corresponds to the PA0 pin, etc.).

PORT C DATA REGISTER

CIOPORTC (READ/WRITE) 0FH (also directly accessible at I/O Port 00E4h)

D7	D6	D5	D4	D3	D2	D1	D0
WP3	WP2	WP1	WP0	D3	D2	D1	D0

The Port C Data register consists of two registers: an Input Data register and an Output Data register. Output data written to the data register is stored in the Output Data register. Reading the data register returns the contents of the Input Data register. Because Port C is only four bits wide, the four least-significant bits of an 8-bit register are used for the Port C Data register. The four most-significant bits are used as a write protect mask for the four least-significant bits (bit D7 is the write protect mask for bit D3, etc.). Writing a 0 to the write protect mask bit enables writing to the corresponding bit in Port C. Writing a 1 inhibits writing the corresponding bit in Port C. Reading Port C always returns 1's in the upper four bits.

Note A reset does not effect the contents of the data registers.

COUNTER/TIMER CONTROL REGISTERS

Each counter/timer has a set of counter/timer Control registers, which perform several functions for the counter/timers.

- specify the mode of operation
- monitor the status
- provide control
- allow access to the down-counter so that it can be preset and read

COUNTER/TIMER MODE SPECIFICATION REGISTERS

CIOCT1MS (READ/WRITE) 1CH
CIOCT2MS (READ/WRITE) 1DH
CIOCT3MS (READ/WRITE) 1EH

D7	D6	D5	D4	D3	D2	D1	D0
C/SC	EOE	ECE	ETE	EGE	REB	DCS1	DCS0

Each Counter/Timer Mode Specification register contains the bits that define its counter/tier's mode of operation and specify the external control and status lines to provide for it. A reset forces all bits to 0. All bits are read/write.

Table 57: Register Bit Assignments

Bit	Mnemonic	Description
D7	C/SC	**Continuous/Single Cycle** — If C/SC is set to 1, then each time the down-counter reaches the count of 1, the time constant value is reloaded (on the next count) and the countdown sequence is repeated. If C/SC is 0 when the count of 1 is encountered (and, for square-wave outputs, if the output is 1), the counter is allowed to count down to 0 and the countdown sequence is terminated.
D6	EOE	**External Output Enable** — By programming this bit to be 1, the output of the counter/timer is provided on the I/O line of the port associated with that particular counter/timer. This bit should not be set to 1 unless the corresponding bit is available, (it is not being used as part of an input or output port). The bit must be programmed to be an output bit in the Data Direction register of its port.
D5	ECE	**External Count Enable** — When ECE is set to 1, the counter/timer is put into the counter mode. The I/O line of the port associated with the counter/timer is used as an external counter input. On each rising edge of the count input (when the data path is specified non-inverting), the down-counter is decremented. The bit must be available and it must be specified to be an input. (Even if the port bit is programmed as an output bit, the port pin, [if enabled] is used as the counter/timer input, allowing the CPU to write this input directly.)
D4	ETE	**External Trigger Enable** — When ETE is set to 1, the I/O line of the port associated with the counter/timer is used as a trigger to input the counter/timer. A rising edge (when the data path is specified non-inverting) on this line will cause the down-counter to be loaded. To guarantee that the counter/timer will be triggered on a particular rising edge of the clocking signal (PCLK/2 or counter input), the trigger rising edge must satisfy a setup time to the preceding falling edge of the clocking signal. As in the external count input, the bit of the port must be available for use by the counter/timer, and must be programmed as an input bit. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input [if enabled], allowing the CPU to write this input directly.)
D3	EGE	**External Gate Enable** — By setting EGE to 1, the I/O line of the port associated with the counter/timer is used as an external gate input to the counter/timer. If the external gate input is a 0 (assuming the data path is programmed non-inverting), the countdown sequence is suspended; forcing it to a 1 enables the countdown sequence to continue. To guarantee the enabling or disabling of the counter/timer for a particular rising edge of the clocking signal (PCLK/2 or counter input), the gate input must satisfy a setup time to the preceding falling edge of the clocking signal. Like external trigger input, the bit must be available and it must be programmed to be an input. (Even if the port bit is programmed as an output bit, the port pin is used as the counter/timer input if enabled. This allows the CPU to write this input directly.)

Bit	Mnemonic	Description
D2	REB	**Retrigger Enable Bit** — If REB is set to 0, triggers (internal or external) which occur during a countdown sequence are ignored. If REB is 1, each trigger causes the time constant value to be reloaded and a new countdown will start on the first half of the square-wave cycle.
D1-D0	DCS1-DCS0	**Output Duty Cycle Selects** — These two bits select the output duty cycle. **DCS1 DCS0 Output Duty Cycle** 0 0 Pulse Output 0 1 One-Shot Output 1 0 Square-Wave Output 1 1 **DO NOT USE**

COUNTER/TIMER COMMAND STATUS REGISTERS

CIOCT1CS (READ/PARTIAL WRITE) 0AH
CIOCT2CS (READ/PARTIAL WRITE) 0BH
CIOCT3CS (READ/PARTIAL WRITE) 0CH

D7	D6	D5	D4	D3	D2	D1	D0
IUS/ICB2	IEICB1	IP/ICB0	ERR	RCC	GCB	TCB	CIP

Each Counter/Timer Command and Status register contains the primary command and status bits for its counter/timer and (in most cases) will be the register most often accessed. A reset forces all bits to 0. The detailed bit descriptions will discuss whether or not a bit can be read or written.

Table 58: Register Bit Assignments

Bit	Mnemonic	Description
D7 (Read)	IUS	**Interrupt Under Service** — The operation is the same as the port IUS bit. This status bit is automatically set to 1 of its corresponding IP is the highest-priority interrupt request pending when an Interrupt Acknowledge sequence takes place. It can also be set directly by CPU command. As long as it is set, the same and lower priority sources of interrupt are inhibited from requesting interrupts via the internal and external daisy-chains. It can be cleared only by CPU command. This bit is read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D6 (Read)	IE	**Interrupt Enable** — The operation is the same as the port IE bit. This bit enables or disables the counter/timer's interrupt logic. While IE is cleared to 0, the port is unable to request an interrupt or to respond to an Interrupt Acknowledge. It does not affect the normal operation of IP or IUS, but simply masks IP off from the rest of the device. A 1 in IUS still affects the interrupt daisy-chain. If IE is programmed to be 1, the interrupt logic operates normally. This is bit read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D5 (Read)	IP	**Interrupt Pending** — The operation is similar to the port IP bit. IP is a status bit which, when set to 1, indicates that the counter/timer requires servicing. It is automatically set to1 each time the counter/timer reaches its terminal count (or by the CPU command). If IE is also 1 and no higher-priority interrupts are under service, then the INT line is pulled Low to request an interrupt. This bit is read/write. It is changed by writing to this register using the coded ICB2-ICB0 bits.
D7-D5 (Write)	ICB2-ICB0	**Interrupt Command Bits** — These three bits control the counter/timer IP, IUS, and IE bits. **ICB3 ICB2 ICB0 Function** 0 0 0 Null Code 0 0 1 Clear IP and IUS 0 1 0 Set IUS 0 1 1 Clear IUS 1 0 0 Set IP 1 0 1 Clear IP 1 1 0 Set IE 1 1 1 Clear IE
D4 (Read)	ERR	**Interrupt Error** — This status bit is set along with IP to indicate that an error has occurred. An error occurs for a counter/timer when ever terminal count is reached and IP is still set from previous terminal count. ERR can be cleared only by having software clear the IP it corresponds to. ERR is a read-only bit.
D3 (Read)	RCC	**Read Counter Control** — RCC is a command bit that enables the counter/timer to be read reliably while it is in a countdown sequence. Writing a 1 to RCC causes the contents of the Counter/Timer Current Count register (CRR), which normally follows the down-counter, to be frozen until the least-significant byte of the CCR is read. Reading the RCC bit indicates when the CCR is frozen. RCC can only be set directly and cannot be set unless the Counter/Timer is enabled in the Master Configuration Control register (CT1E, CT2E, or CT3E). RCC can be cleared automatically by reading the least-significant byte of the CRR or by disabling the counter/timer via the corresponding enable bit.

Table 58: Register Bit Assignments (Continued)

Bit	Mnemonic	Description
D2 (Read)	GCB	**Gate Command Bit** — GCB is a command bit that can be used to halt a countdown sequence. By writing GCB with a 0, the countdown sequence is halted. Returning to GCB to 1 allows the sequence to resume where it left off. The state of the GCB bit does not affect the operation of the trigger inputs. GCB is a read/write bit.
D1 (Read)	TCB	**Trigger Command Bit** — Writing a 1 to the TCB the counter/timer. It causes the down-counter to be loaded with the time constant value and a countdown sequence to be initiated. It can also retrigger the counter/timer if the Retrigger Enable bit (REB) is set to 1. TCB is a write-only bit. When read it always returns to 0. In this way, erroneous trigger commands are not issued when bit set or clear operations are performed on the other bits in this register.
D0 (Read/ Write)	CIP	**Count In Progress** — CIP is a status bit that indicates if a countdown sequence is on progress. It is automatically set to 1 when the counter/timer is triggered and the down-counter is loaded with the time constant value. It is automatically reset to 0 when the down-counter reaches a count of 0. The state of the gate inputs (internal and external) has no effect on this bit. CIP is read-only.

COUNTER/TIMER TIME CONSTANT REGISTERS

CIOCT1TCM (READ/WRITE) 16H
CIOCT1TCL (READ/WRITE) 17H
CIOCT2TCM (READ/WRITE) 18H
CIOCT2TCL (READ/WRITE) 19H
CIOCT3TCM (READ/WRITE) 1AH
CIOCT3TCL (READ/WRITE) 1BH

D7	D6	D5	D4	D3	D2	D1	D0
TC15/TC7	TC14/TC6	TC13/TC5	TC12/TC4	TC11/TC3	TC10/TC2	TC9/TC1	TC8/TC0

Each of the Time Constant registers is 16-bits and holds the value loaded into the down-counter of its counter/timer when a trigger is detected. It is accessed by the CPU as two consecutive 8-bit registers (Most Significant Byte and Least Significant Byte). These registers can be read and written at any time. However, care must be taken when writing them so that a trigger does not occur while the time constant value is changing. A reset does not effect the Time Constant register.

COUNTER/TIMER CURRENT COUNT REGISTERS

CIOCT1CCM (READ ONLY) 10H
CIOCT1CCL (READ ONLY) 11H
CIOCT2CCM (READ ONLY) 12H
CIOCT2CCL (READ ONLY) 13H
CIOCT3CCM (READ ONLY) 14H
CIOCT3CCL (READ ONLY) 15H

D7	D6	D5	D4	D3	D2	D1	D0
CC15/CC7	CC14/CC6	CC13/CC5	CC12/CC4	CC11/CC3	CC10/CC2	CC9/CC1	CC8/CC0

Each of the Counter/Timer Current Count registers (CCR) is 16-bit register used to read the contents of its counter/timer down-counter. The CCR follows the down-counter until the RCC bit in the Counter/Timer Command and Status register is written with a 1. The value present when the write occurs is held until the least-significant byte is read. Then, the CCR follows the down-counter again. The countdown sequence is not affected. The CCR is accessed as two consecutive 8-bit registers (Most Significant Byte and Least Significant Byte). They can be read at anytime, whether or not the value is frozen. Writes to the CCR are ignored. A reset forces the CCR to follow the down-counter (neither are forced to a specific value).

Interrupt Related Registers

These registers contain the interrupt vectors output during Interrupt Acknowledge sequences. Three vector registers are provided: one for Port A, one for Port B, and one shared by the three counter/timers. Another register is provided, which facilitates using this device in a polled environment.

INTERRUPT VECTOR REGISTERS

CIOAIV (READ/WRITE) 02H
CIOBIV (READ/WRITE) 03H
CIOCTIV (READ/WRITE) 04H

D7	D6	D5	D4	D3	D2	D1	D0
IVEC7	IVEC6	IVEC5	IVEC4	IVEC3	IVEC2	IVEC1	IVEC0

Each of the Interrupt Vector registers holds the interrupt vector returned when the source of the interrupt associated with its port is acknowledged. The interrupt vector value is user-defined by writing the desired 8-bit identification code to this register when identifying the CIO. A modified version of the value written to the Interrupt Vector register can be returned if the vector is programmed to include status. This does not affect the value written to the Interrupt Vector register.

The Interrupt Vector register is a read/write register. When read, the value returned always includes the status if MIE = 1 (whether or not the associated Vector Includes Status bit is 1). If MIE = 0, the unmodified vector is returned independent of the state of the VIS bit. A reset does not affect the Interrupt Vector register.

Table 59: Interrupt Vector Encoding if Vector Includes Status

Port Vector Status		Counter/Timer Status
OR-Priority Encoded Vector Mode	**All Other Modes**	
D3 D2 D1 x x x Number of highest priority bit with a match.	**D3 D2 D1** ORE IRF PMF Normal 0 0 0 Error*	**D2 D1** 0 0 Counter/Timer 3 0 1 Counter/Timer 2 1 0 Counter/Timer 1 1 1 Error

* The error status indicates that the highest-priority counter/timer with an interrupt pending also has its ERR flag set. The CPU must poll the Command and Status registers to determine which counter/timer has its ERR flag set.

CURRENT VECTOR REGISTER

CIOCV (READ) 1FH

D7	D6	D5	D4	D3	D2	D1	D0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

When the Current Vector register is read, it returns the interrupt vector that would have been output by the device during an Interrupt Acknowledge cycle if its IEI input had been High. The vector returned corresponds to the highest priority IP independent of the IUS. The order of priority (highest to lowest) is: Counter/Timer 3, Port A, Counter/Timer 2, Port B, Counter/Timer 1. If no enabled interrupts are pending, a pattern of all 1's is output. This is useful in a polled environment or when CPU does not read vectors. This register is a read-only register. Since a reset disables all interrupts, reading the Current Vector register after a reset will return all 1s.

I/O Port Operation

OVERVIEW

There are three I/O ports provided by the CIO device. Ports A and B are general-purpose ports; Port C is a 4-bit special-purpose port. All three ports can be programmed as bit ports.

In general, bit ports are used to provide status input lines and control output lines. When the I/O ports are configured as bit ports, data can be moved in either direction on an individual, pin-by-pin basis. There are up to twenty pins available for this kind of data handling by the three ports.

Another I/O Port function is to provide external access for the control of three independent counter/timers and distribution of their outputs. Port B provides access for Counter/Timers 1 and 2. Port C provides access to Counter/Timer 3.

Pattern-recognition capability is provided in Ports A and B. In general, it is possible to test data for specified patterns and to generate interrupt requests based on the match obtained.

PATTERN-RECOGNITION LOGIC OPERATION

Both Ports A and B can be programmed to generate interrupts when a specific pattern is recognized at the port. The pattern-recognition logic is independent of the port application, thereby allowing the port to recognize patterns in all of its configurations. The pattern can be independently specified for each bit as: 1, 0, 0-to-1 transition, 1-to-0 transition, or any transition. Individual bits can be masked off. Three modes of pattern-recognition operation are supported: AND, OR, and OR-Priority Encoded Vector (OR-PEV). A pattern match is defined as the simultaneous satisfaction of all non-masked bit specifications in the AND mode or the satisfaction of any non-masked bit specifications in either the OR or OR-PEV modes.

The pattern specified in the Pattern Definition register assumes that the data path is programmed to be non-inverting. If an input bit in the data path is programmed to be inverting, the pattern detected is the opposite of the one specified. Output bits used in the pattern of match logic are internally sampled before the invert/non-invert logic.

The operation of the pattern-recognition logic in the various port modes will be described in detail in the following sections.

BIT PORT OPERATION

Bit ports are used to provide the CPU with input lines to monitor status, and with output lines to provide control. There are up to twenty bits available for this type of data handling provided by the three ports of the CIO: eight each by Ports A and B and four by Port C.

Writing the data register of a bit port updates the value being output by all output bits in the port. Reading the data register of the bit port returns the state of all bits, outputs as well as inputs.

BIT PORT SIMPLE OPERATION

The port's Data Direction register specifies the direction of data flow for each bit of a bit port. A 1 specifies an input bit; a 0 specifies an output bit.

The Data Path Polarity register provides the capability of inverting the data path. A 1 specifies inverting, and a 0 specifies non-inverting. All discussions of the port operations assume that the path is programmed non-inverting.

The value returned when reading an input bit reflects the state of the input just prior to the read. A 1's catcher can be inserted into the input data path by programming a 1 to the corresponding bit position of the port's Special I/O Control register. When a 1 is detected at the 1's catcher input, its output is automatically set to 1 until is it cleared by software. The 1's catcher is cleared by writing a 0 to the corresponding bit in the data register. In all other cases, attempted writes to input ports are ignored. The 1's catcher is level-sensitive. If the input is still a one when it is cleared, the output will again be set to 1. Also, the input to the 1's catcher follows the invert/non-invert logic. If the bit is programmed inverting, a low voltage level at the pin will cause the 1's catcher output to go to a 1.

When Ports A and B include output bits, reading the data register returns the value being output. Reads of Port C returns the state of the pins. Outputs can be specified as open-drain by writing a 1 to the corresponding bit of the port's Special I/O Control register. Port C has the additional feature of bit-addressable writes. When writing to Port C, the four most-significant bits are used as a write protect mask for the least-significant bits (0-4, 1-5, 2-6, 3-7). With this feature, any combination of bits can be set or cleared (while other bits remain undisturbed), without first reading the register.

BIT PORT PATTERN-RECOGNITION OPERATION

Ports A and B contain pattern-recognition logic, which enables the port to detect a user-specified pattern and to generate an interrupt request when the pattern is detected. Pattern-recognition may be performed on all bits, including those used as I/O for the counter/timers. For input bits, the input to the pattern-recognition logic reflects the value on the pins (through the invert/non-invert logic) in all cases except for inputs with 1's catchers. In this case, the outputs of the 1's catcher is used. For output bits, this is the value being output before the invert/non-invert logic is used. When operating in the AND or OR mode, the transition from a no-match to a match state causes the interrupt. In the OR mode, if a second match occurs before the first match goes away, it does not cause a second interrupt. Bit ports specified in the OR-PEV mode generate interrupts as long as a match state exists. A transition from a no-match to a match state is not required. Since a match condition only lasts a short time when transition patterns are specified, care must be taken—no more than one bit should be programmed with a transition match specifications in a port operating in the AND mode.

The pattern-recognition logic of bit ports operates in two basic modes: Transparent and Latched. When the Latch on Pattern Match (LPM) bit is set to 0 (Transparent mode), the interrupt indicates that a specified pattern has occurred, but a read of the data register does not necessarily indicate the state of the port at the time interrupt was generated. In the Latched mode (LPM = 1), the state of all the port inputs at the time the match was detected is latched in the Buffer register and held until IP is cleared. In all cases, the Pattern Match Flag (PMF) in the port's Command and Status register indicates the state of the port at the time PMF is read. Only Transparent mode (LPM = 0) is supported when OR-PEV is specified. In all modes, the port's IP bit is set and an interrupt generated (if enabled) when the pattern match is detected. The IP can only be cleared by a command to the Port Command and Status register.

If a second match occurs while IP is already set, an error condition exists. If the Interrupt ON Error bit (IOE) is 0, the match is ignored. However, if IOE is 1 after the first IP is cleared, the IP is automatically set to 1 along with the Interrupt Error (ERR) flag. ERR is automatically cleared when the corresponding IP is cleared by software.

When a pattern-match is present in the OR-Priority Encoded Vector mode, IP is set to 1. The IP cannot be cleared until a match is no longer present. If the interrupt vector is allowed to include status, the vector returned during Interrupt Acknowledge indicates the highest-priority bit matching its specification at the time of the Acknowledge cycle. Bit 7 is the highest-priority bit and bit 0 is the lowest-priority bit. The bit initially causing the interrupt may not be the one indicated by the vector if a higher-priority bit matches before the Acknowledge. Once the Interrupt Acknowledge cycle is initiated, the vector is frozen until the corresponding Interrupt Under Service (IUS) is cleared. If an input that causes interrupts changes before the interrupt is serviced, the 1's catcher can be used to hold the value. Bits should not be specified with transition detection, because the match will no longer be valid at the time of the Interrupt Acknowledge. If no match is present at the time of the Acknowledge, the vector will indicate the lowest-priority bit (Bit 0).

Because a no-match-to-match transition is not required, the source of the interrupt must be cleared before IP is cleared or else a second interrupt is generated. No programmer error detection is performed in this mode and the Interrupt on Error bit should be 0.

One application of the OR-PEV pattern match mode is to use the CIO as a Programmable Interrupt Controller (PIC).

Counter/Timer Operation

COUNTER/TIMER ARCHITECTURE

The three independent 16-bit counter/timers each consist of a presettable 16-bit down-counter, a 16-bit Time Constant register, a 16-bit Current Counter register, an 8-bit Mode Specification register, an 8-bit Command and Status register, and the associated control logic that links these registers.

The flexibility of the counter/timers is enhanced by the provision of up to four lines per counter/timer (counter input, gate input, trigger input, and counter/timer input) for direct external control and status. Counter/Timer 1's external I/O lines are provided by the four most-significant bits of Port B. Counter/Timer 2's external I/O lines are provided by the four least-significant bits of Port B. Counter/Timer 3's external I/O lines are provided by the four bits of Port C. The utilization of these lines (Table 4-1) is programmable on a bit-by-bit basis via the Counter/Timer Mode Specification registers.

When external counter/timer I/O lines are to be used, the associated port lines must be vacant and programmed in the proper data direction. Lines used for counter/timer I/O have the same characteristics as simple input lines. They can be specified as inverting or non-inverting, and can be read and used with the pattern-recognition logic. They can also include the 1's catcher input.

Table 60: Counter/Timer External Access

Function	Counter/Timer 1	Counter/Timer 2	Counter/Timer 3
Counter/Timer Output	Port B Data 4	Port B Data 0	Port C Data 0
Counter Input	Port B Data 5	Port B Data 1	Port C Data 1
Trigger Input	Port B Data 6	Port B Data 2	Port C Data 2
Gate Input	Port B Data 7	Port B Data 3	Port C Data 3

COUNTER/TIMER SEQUENCE OF EVENTS

The following discussion assumes that the inputs and outputs are programmed non-inverting.

INITIALIZING THE COUNTER/TIMER

Before starting a counter/timer sequence:

First, the Counter/Timer Mode Specification register and the Counter/Timer Command and Status register of the desired counter/timer must be initialized. Initialization requires several things to be specified, for example, the external lines to be used, the output duty cycle, and whether the cycle is continuous or single-cycle.

Second, the Time Constant must be specified by writing the desired value to the Time Constant register. The Time Constant register is accessed as two 8-bit registers. The registers are readable as well as writeable, and can be accessed in any order. A 0 in the Time Constant register specifies a Time Constant of 65,536.

Third, if external access is going to be provided, the port to be used must be programmed as a bit port and the necessary bits must be programmed in the proper direction.

Finally, the Counter/Timer Enable bit in the Master Configuration Control register is set. This initialization sequence can best be understood by examining the function of the various enable bits. This bit, while cleared to 0, prevents spurious counter/timer operation:

- IPs can not be set
- Counter/Timers can not be triggered.
- The Read Current Count bit that freezes the value in the Current Count register will be held cleared to 0.
- The Counter/Timer output is forced to 0.

Clearing an enable bit will not clear an existing IP that is set—it will only inhibit the IP from being set again. Clearing the enable bit will clear the Read Counter Control bit, causing the Current Count register to follow the down-counter.

STARTING THE COUNTER/TIMER

The countdown sequence is initiated when the counter/timer is triggered and the down-counter is loaded with the contents of the Time Constant register. The down-counter is normally loaded on the rising edge of the external trigger input, or by writing a 1 to the Trigger Command Bit (TCB) of the Command and Status register. But, for Counter/Timer 2 only, triggering can occur on the falling edge of Counter/Timer 1's internal output if the counters are linked via the trigger input. Also, Counter/Timer 3 can be triggered by the handshake logic when it is used with the Pulsed Handshake.

The trigger functions as the logical OR of all the potential triggers. Since the trigger function is an OR function, and since it is rising-edge sensitive, any input remaining in its active state will mask off other trigger sources as it stays High.

Note In order to ensure the loading of a Trigger Constant on a particular rising edge of the clocking signal, sufficient setup time must be allowed—the trigger must occur prior to the immediately preceding falling edge of the clocking signal. (The clocking signal equals the count input if in Counter mode or PCLK/2 if in Timer mode.)

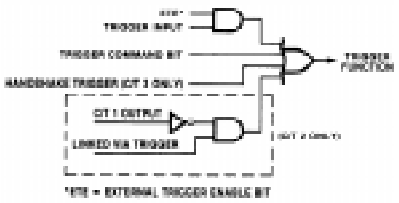


Figure 8. Trigger OR-Function Diagram

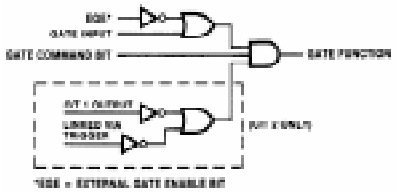


Figure 9. Gate AND-Function Diagram

COUNTDOWN SEQUENCE

The rate at which the down-counter counts is determined by the mode of the counter/timer. In the Timer mode (the External Count Enable [ECE] bit is 0), the down-counter is clocked internally by a signal that is half the frequency of the PCLK input to the chip. In the Counter mode (ECE is 1), the down-counter is decremented on the rising edge of the counter/timer's counter input.

Once the down-counter is loaded, the countdown sequence continues toward terminal count as long as all of the counter/timers' hardware and software gate inputs are High. The gate inputs are: the Gate Command bit of the Counter/Timer Command and Status register, and the external gate input if enabled in the External Gate Enable bit of the counter/timer Mode Specification register. Also, for Counter/Timer 2 use only, the counter/timer output (inverted) can be used as a gate if linked via the gate in the Counter/Timer Link Controls bits of the Master Configuration Control register. If any of the gate inputs go Low (0), the countdown halts. It resumes when all gate inputs are 1 again. The gate function does not affect the trigger function.

The gate functions as the logical AND of all the potential gates.

Note In order to ensure the enabling or disabling of the counter/timer on a particular rising edge of the clocking signal, sufficient setup time must be allowed. The gate signal must be valid prior to immediately preceding falling edge of the clocking signal.

The reaction to triggers occurring during a countdown sequence is determined by the state of the Retrigger Enable Bit (REB) in the Mode Specification register. If REB is 0, retriggers are ignored and the countdown continues normally. If REB is 1, each trigger causes the down-counter to be reloaded and the countdown sequence starts over again. If the output is programmed is the Square-Wave mode, a retrigger causes the sequence to start over from the initial load of the time constant.

The state of the down-counter can be determined in two ways: by reading the contents of the down-counter via the Current Count register or by testing the Count In Progress (CIP) status bit in the Command and Status register. The CIP status bit is set when the down-counter is loaded: it is reset when the down-counter reaches 0. The Current Counter register is a 16-bit register, accessible as two 8-bit registers, which mirrors the contents of the down-counter. This register can be read at any time. However, reading the register is asynchronous to the counter's counting, and the value returned can be guaranteed as valid only if the counter is stopped. The down-counter can be read reliably while it is counting by first writing a 1 to the Read Counter Control (RCC) bit in the counter/timer's Command and Status register. This freezes the value in the Current Count register until a read of the least-significant byte is performed. A read of RCC indicates if the CCR is holding a value, or if it is following the down-counter.

ENDING CONDITION

The Continuous/Single Cycle (C/SC) bit in the Mode Specification register controls operation of the down-counter when it reaches terminal count (the count following the count of 1). If C/SC is 0 when a terminal count is reached, the countdown sequence stops. If the C/SC bit is 1 each time the count-down counter reaches 1, the next cycle causes the time constant value to be reloaded. The time constant value may be changed by the CPU, and on reload, the new time constant value is loaded. This must be done with care.

Each time the counter reaches terminal count, its Interrupt Pending (IP) bit is set to 1, and if interrupts are enabled (IE = 1), an interrupt request is generated. If a terminal count occurs while IP is already set, an internal error flag is set. As soon as IP is cleared, it is forced to a 1 along with the Interrupt Error (ERR) flag. Errors that occur after the internal flag is set are ignored. ERR is cleared to 0 when the corresponding IP is cleared.

COUNTER/TIMER OUTPUT

There are three duty cycles available for the timer/counter output: pulse, one-shot, and square-wave. When the Pulse mode is specified, the output goes High for one cycle, beginning when the down-counter leaves the count of 1. In the One-shot mode, the output goes High when the counter/timer is triggered and goes Low when the down-counter reaches 0. When the square-wave output duty cycle is specified, the counter/timer goes through two full sequences for each cycle. The initial trigger causes the down-counter to be loaded and the normal count-down sequence to begin. When a 1 count is detected on the down-counter's clocking edge, the output goes High and the time constant value is reloaded. On the clocking edge, when both the down-counter and the output are 1's, the output is forced Low.

LINKED SEQUENCE

Counter/Timers 1 and 2 can be linked internally in three different ways. Counter/Timer 1's output (inverted) can be used as Counter/Timer 2's trigger, gate, or counter input. When linked, the counter/timers have the same capabilities as when used separately. However, when they are linked, they should be linked before they are enabled. The only restriction is that when Counter/Timer 1 drives Counter/Timers 2's count input, Counter/Timer 2 must be programmed with its external count input disabled (ECE = 0).

The initialization procedure, then, is the same as for individual counter/timers, except that the linking bits need to be appropriately set.

Interrupt Operation

OVERVIEW

Interrupts are generated whenever asynchronous CPU intervetion is required by a peripheral device. Two examples of interrupt request sources in the CIO are: a pattern match occurring in a bit port or a counter/timer reaching its terminal count.

PRIORITY HANDLING AND THE CIO

The CIO is designed to provide interrupt priority resolution in situations where there may be competing interrupt requestors.

The CIO has five potential sources of interrupts: the three counter/timers and Ports A and B. The priorities of these sources are fixed in the following order (highest to lowest): Counter/Timer 3, Port A, Counter/Timer 2, Port B, and Counter/Timer 1.

Interrupts generated by the CIO are routed to the VSBC interrupt controller on IRQ15 via jumper block V8[1-2].

THE FOUR INTERRUPT LOGIC FUNCTIONS

The CIO has the logic necessary to: generate interrupts, resolve priority when there is more than one interrupt requestor, inhibit preemptive interrupts by the lower-priority requestors, and clearly identify the exact source of interrupt.

GENERATING THE INTERRUPT REQUEST

Each source interrupt in the CIO contains three bits for the control and status of the interrupt logic: an Interrupt Pending (IP) bit, an Interrupt Under Service (IUS) bit, and an Interrupt Enable (IE) bit. IP is automatically set when an event requiring CPU intervention occurs. The setting of IP results in an Interrupt Request on IRQ15 via jumper block V8[1-2]. IP can also be set by a command. This is useful when debugging interrupt handler software.

The IE bit provides a means of masking off individual sources of interrupts within the CIO. When IE is set to 1, an interrupt request is generated normally. When IE is reset to 0, the IP is masked off. The IP bit is still set when an event occurs that would normally require service; however a hardware interrupt request is not generated.

The IUS status bit is set by the CPU as a result of the Interrupt Acknowledge cycle if, at the time of the Interrupt Acknowledge cycle, the corresponding IP is the highest-priority unmasked IP. When IUS is 1, it indicates that the corresponding IP has been recognized by the CPU and is being serviced. As long as IUS is set the corresponding IP is masked off and a hardware interrupt request is generated.

The Master Interrupt Enable (MIE) bit allows all sources of interrupts within the CIO to be disabled without having to individually clear each IE to 0. If MIE is reset to 0, all IPs are masked off and no interrupt can be requested or acknowledged.

IDENTIFICATION OF THE HIGHEST-PRIORITY INTERRUPT REQUEST

Since CIO hardware interrupt vectors are not supported on the VSBC, the Current Vector register facilitates the identification of the interrupting source. When read, the data returned is the same as the interrupt vector that would normally be provided during an Interrupt Acknowledge cycle based on the highest IP set. If no unmasked IPs are set, the value FFh is returned. The Current Vector register provides an easy way to poll all IPs in a single read.

The interrupt vector can include additional status information identifying the cause of the interrupt as well as the source identification.

The CIO contains three vector registers: one for Port A, one for Port B, and one shared by the three counter/timers. Unique identification information can be placed by the user in the Interrupt Vector register for each interrupt source. The base vector can be modified to include status information to pinpoint the cause of the interrupt. A Vector Includes Status (VIS) control bit controls whether or not the vector is modified with status information.

Each base vector has its own VIS bit and is controlled independently. When MIE = 1, reading the base vector register always includes status, independent of the state of the VIS bit. All the information obtained by the vector, including status, can thus be obtained with one additional instruction when VIS is set to 0. When MIE = 0, reading the vector register returns the unmodified base vector so that it can be verified.

Another register, the Current Vector register, facilitates the use of the CIO in a polled environment. When read, the data returned is the same as the interrupt vector that would normally be output as a hardware interrupt vector. If no unmasked IPs are set, the value FFh is returned.

The No Vector (NV) control bit of the Master Interrupt Control register, when set to 1, inhibits the generation of an interrupt vector during an INTAK cycle. The NV bit does not affect the setting of the IUS operation.

Table 61: Interrupt Vector Encoding if Vector Includes Status

Port Vector Status		Counter/Timer Status
OR-Priority Encoded Vector Mode	**All Other Modes**	
D3 D2 D1 x x x Number of highest priority bit with a match.	**D3 D2 D1** ORE IRF PMF Normal 0 0 0 Error*	**D2 D1** 0 0 Counter/Timer 3 0 1 Counter/Timer 2 1 0 Counter/Timer 1 1 1 Error

* The error status indicates that the highest-priority counter/timer with an interrupt pending also has its ERR flag set. The CPU must poll the Command and Status registers to determine which counter/timer has its ERR flag set.

INTERRUPT OPERATION

The IP bit is not set while the CIO Chip is in State 1 (refer to page 73 for a description of state conditions.) Therefore, to minimize interrupt latency, the CIO Chip should not be left in State 1.

The CIO Chip generates an interrupt request on INT 15 if:

- Interrupt requests are enabled (IE = 1 and MIE = 1)
- It has an interrupt pending (IP = 1)
- It does not have an interrupt under service (IUS = 0)
- No higher-priority interrupt is being serviced (IEI = 1)

To remove the interrupt request signal, the IP bit for the associated interrupt needs to be cleared.

CIO Initialization

INTRODUCTION

The CIO is reset by writing a 1 to the Reset bit (D0) in the Master Interrupt Control register. RESET disables all functions except a read or write to the Reset bit. In the reset state, the pointer always points to the Master Interrupt Control register. Writes to all other bits are ignored, and all reads return 01h. In this state, all control bits are forced to 0, all port I/O lines are tri-stated, and the interrupt output is not asserted.

Even if the state of the CIO is not known, the following sequence will reset it.

```
IN    CIOCTL      Insures state 0 or reset state
OUT   CIOCTL,0    Write pointer or clear reset
IN    CIOCTL      State 0
OUT   CIOCTL,0    Write pointer
OUT   CIOCTL,1    Write reset
OUT   CIOCTL,0    Clear reset
```

ENABLE BITS OPERATION

As the different functions of the CIO are being initially programmed, it is possible for erroneous interrupt requests to be generated, or for an illegal combination of modes to be temporarily specified. To alleviate this problem without imposing severe restrictions on the sequence of events required to initialize the device, five internal enable control bits are provided: Port A Enable, Port B Enable, Counter/Timer 1 Enable, Counter/Timer 2 Enable, and one enable shared by Counter/Timer 3 and Port C. While these bits are cleared to 0, the corresponding logic sections are in an initialization mode. All of the registers can be read and written, but the normal operation of the sections is inhibited. The Port A and Port B Enables, when cleared to 0, force their respective I/O lines into a high-impedance state, hold the 1's catchers in a reset condition, inhibit request/wait generation, and prevent the setting of their Interrupt Pending (IP) bits (the states of IP and Interrupt Under Service (IUS) are not affected). Additionally, output data can be written (the first data output is valid when the output drivers go active), but the data direction for these bits must be properly specified before the data is written. The Port C Enable operates in the same way, and, until set to 1, the handshake logic for Ports A and B is forced into an idle state. The Counter/Timer Enables, when set to 0, terminate any countdown sequence in progress, inhibit the counter/timer from being triggered, and force the counter output to 0. While the enable is 0, the Read Counter Control (RCC) bit in the Counter/Timer Command and Status register is forced to 0. Independent enable bits are provided for the different sections of the device so that the individual sections can be reconfigured without disturbing the status of the unchanged sections. By using these enable bits, the device can be initialized in any sequence as long as the desired configuration for a section is specified before its enable bit is set to 1. When ports or counter/timers are to be linked, the bits which specify linking must be programmed before the functions are enabled. In this case two writes are required to the Master Configuration Control register.

Programming

Programming the CIO Entails loading control registers with bits to implement the desired operation. As discussed above, individual enable bits are provided for the various major blocks so that erroneous operations do not occur while the port is being initialized. Before the ports are enabled: IPs cannot be set, REQUEST and WAIT cannot be asserted, and all output remain high impedance; the handshake lines are ignored until Port C is enabled; and the counter/timers cannot be triggered until their enable bits are set.

INTERRUPT CODE EXAMPLE

The following code example demonstrates the generation of an interrupt when a specific bit pattern (55h) is detected on Port B. It is assumed that a hardware loopback cable is installed causing values written to Port A to "come back in" on Port B.

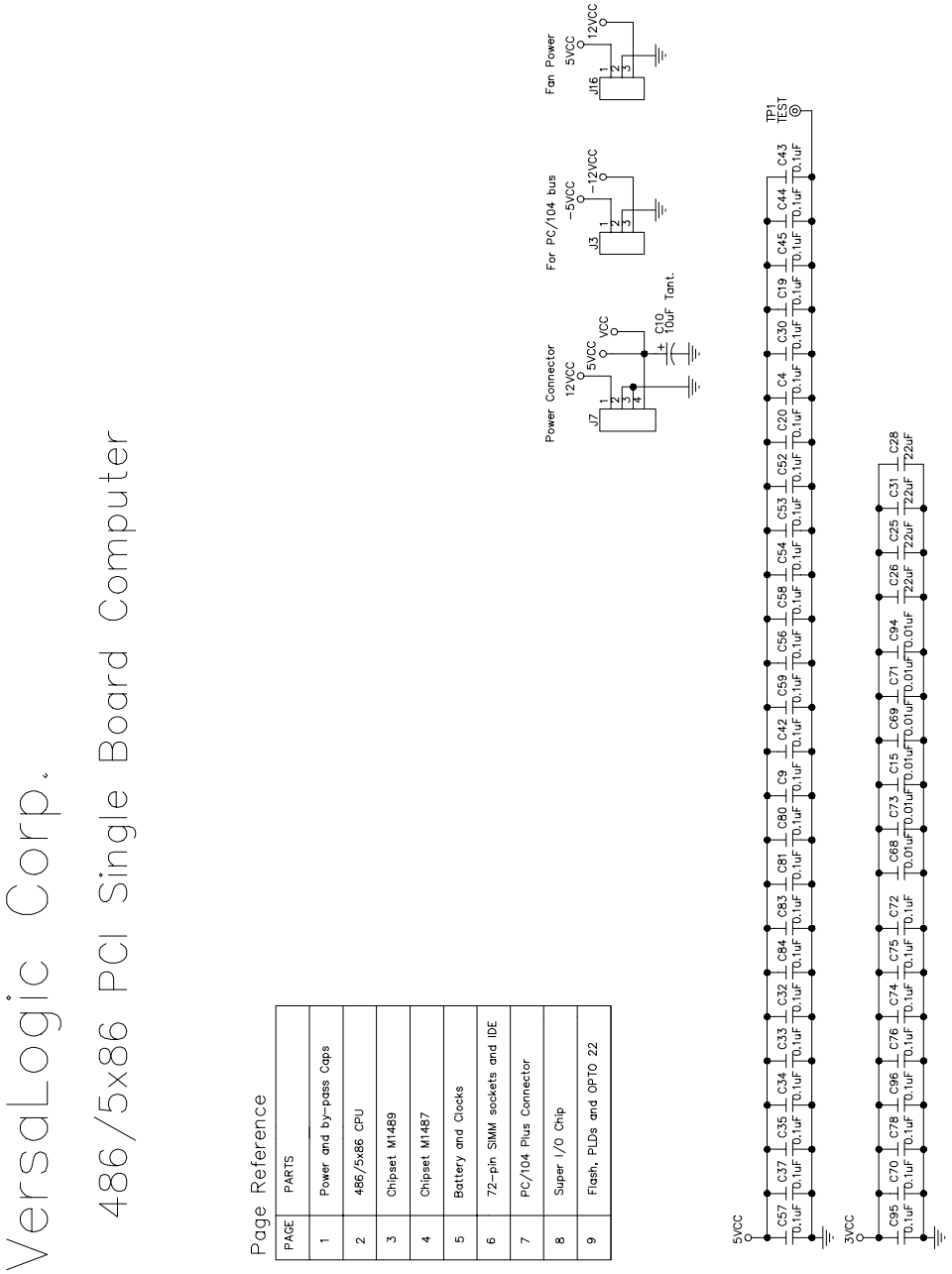
```
// ========================================================================
//  VersaLogic Test Program for I/O to the Z8536 Chip
// ========================================================================

#include <dos.h>
#include <stdio.h>

void main(void)
{
    unsigned char in_val1, in_val2;  /* temp. values */

/* Configure all Ports A,B, & C */

printf ("\nStart configuration sequence\n");
    outportb(0xE7, 0x00);  // Dummy write to Port E7 to clear reset
    in_val1 = inportb(0xE7);

printf ("Make Port A bits outputs\n");
    outportb(0xE7, 0x23);  // Set all Port A bits to output
    outportb(0xE7, 0x00);
    outportb(0xE7, 0x23);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 23h and E7, 00h; returned value = %x\n", in_val1);

printf ("Make Port B bits inputs\n");
    outportb(0xE7, 0x2B);  // Set all Port B bits to input
    outportb(0xE7, 0xFF);
    outportb(0xE7, 0x2B);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 2Bh and E7, FFh; returned value = %x\n", in_val1);

printf ("Enable ports A,B, & C\n");
    outportb(0xE7, 0x01);  // Enbale ports A,B, & C
    outportb(0xE7, 0x94);
    outportb(0xE7, 0x01);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 01h and E7, 94h; returned value = %x\n", in_val1);
printf ("End of configuraition... \n");

// End configuration

// Initilize Port B for pattern matching
printf ("Write to Port B Mode register\n");
    outportb(0xE7, 0x28);  //
    outportb(0xE7, 0x0B);
    outportb(0xE7, 0x28);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 28h and E7, 0Bh; returned value = %x\n", in_val1);

// Setup pattern to match as 55h, through the next 3 registers
printf ("Write to Port B pattern polarity\n");
    outportb(0xE7, 0x2D);  //
    outportb(0xE7, 0x55);
    outportb(0xE7, 0x2D);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 2Dh and E7, 55h; returned value = %x\n", in_val1);

printf ("Write to Port B pattern transition\n");
    outportb(0xE7, 0x2E);  //
    outportb(0xE7, 0x00);
    outportb(0xE7, 0x2E);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 2Eh and E7, 00h; returned value = %x\n", in_val1);

printf ("Write to Port B pattern mask\n");
    outportb(0xE7, 0x2F);  //
    outportb(0xE7, 0xFF);
    outportb(0xE7, 0x2F);  // Test if values are written to Z8536
```

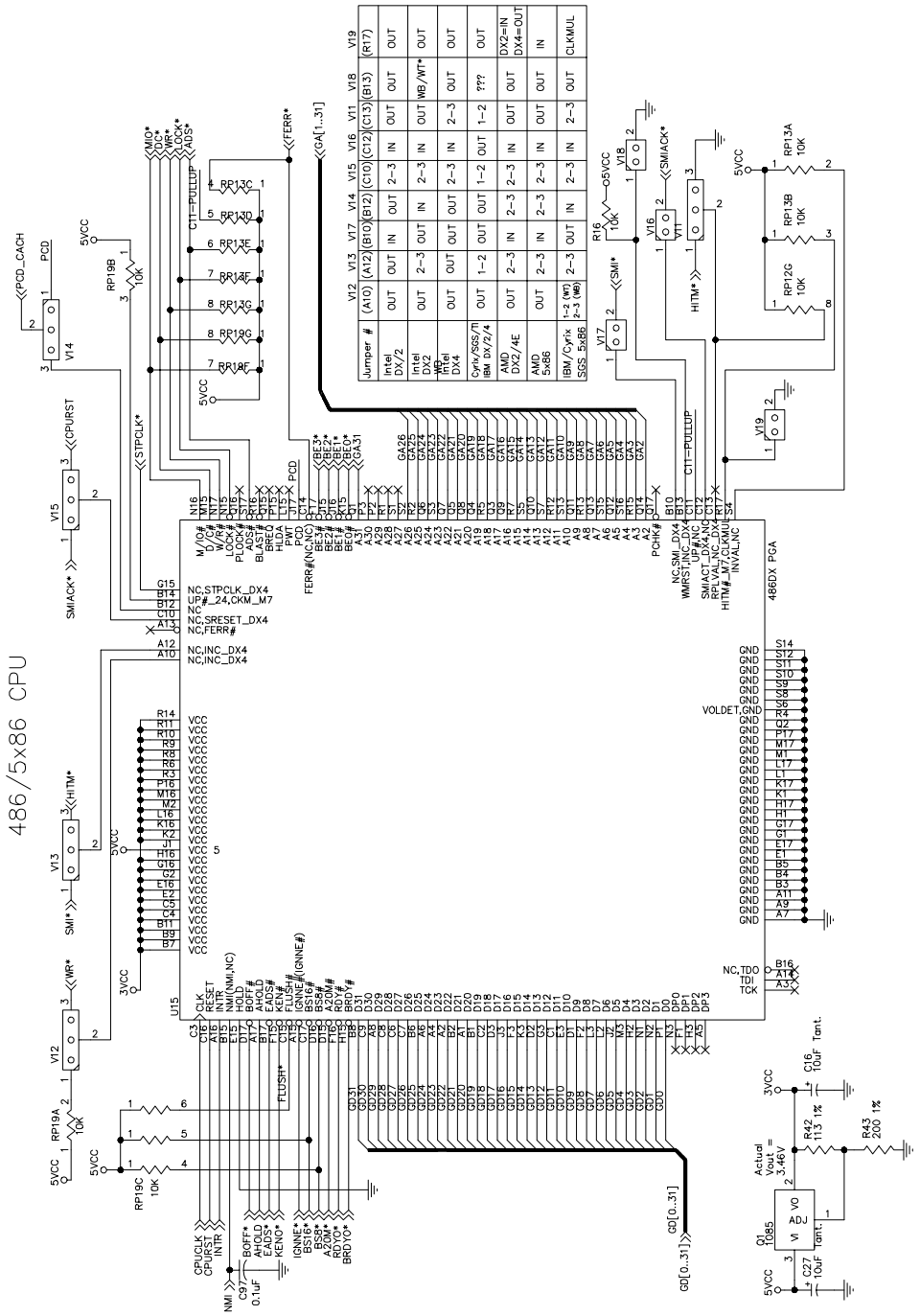
```
    in_val1 = inportb(0xE7);
printf ("Output E7, 2Fh and E7, FFh; returned value = %x\n", in_val1);

// Write to Interrupt enable bit
printf ("Write Port B Command and Status register, clear IP & IUS\n");
    outportb(0xE7, 0x09);  //
    outportb(0xE7, 0x20);
    outportb(0xE7, 0x09);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 09h and E7, 20h; returned value = %x\n", in_val1);

printf ("Write Port B Command and Status register, set IE\n");
    outportb(0xE7, 0x09);  //
    outportb(0xE7, 0xC0);
    outportb(0xE7, 0x09);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 09h and E7, C0h; returned value = %x\n", in_val1);

// Set value for Int. vector register
printf ("Write Port B Int. vector register\n");
    outportb(0xE7, 0x03);  //
    outportb(0xE7, 0xAA);
    outportb(0xE7, 0x03);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 03h and E7, AAh; returned value = %x\n", in_val1);

// Set Master Interrupt Enable
printf ("Set master interrupt enable\n");
    outportb(0xE7, 0x00);  //
    outportb(0xE7, 0x80);
    outportb(0xE7, 0x00);  // Test if values are written to Z8536
    in_val1 = inportb(0xE7);
printf ("Output E7, 00h and E7, 80h; returned value = %x\n", in_val1);

// Output Zero from Port A to Port B, should not cause an interrupt
printf ("Ports A/B value=0x00\n");
    outportb(0xE6, 0x00);
    in_val1 = (0x00FF & inportb(0xE5));
printf ("Output E6, 00h; Read in from E5 = %x\n", in_val1);

// Read current value for Vector register, should be FFh for no interrupt
printf ("Check value of 'Current Vector Register' before sending 55h\n");
    outportb(0xE7, 0x1F);
    in_val1 = inportb(0xE7);
printf ("Output E7, 1Fh; returned value = %x\n", in_val1);

// Output value 55h from Port A to Port B, should cause an interrupt
printf ("Ports A/B value=0x55\n");
    outportb(0xE6, 0x55);
    in_val1 = (0x00FF & inportb(0xE5));
printf ("Output E6, 55h; Read in from E5 = %x\n", in_val1);
```

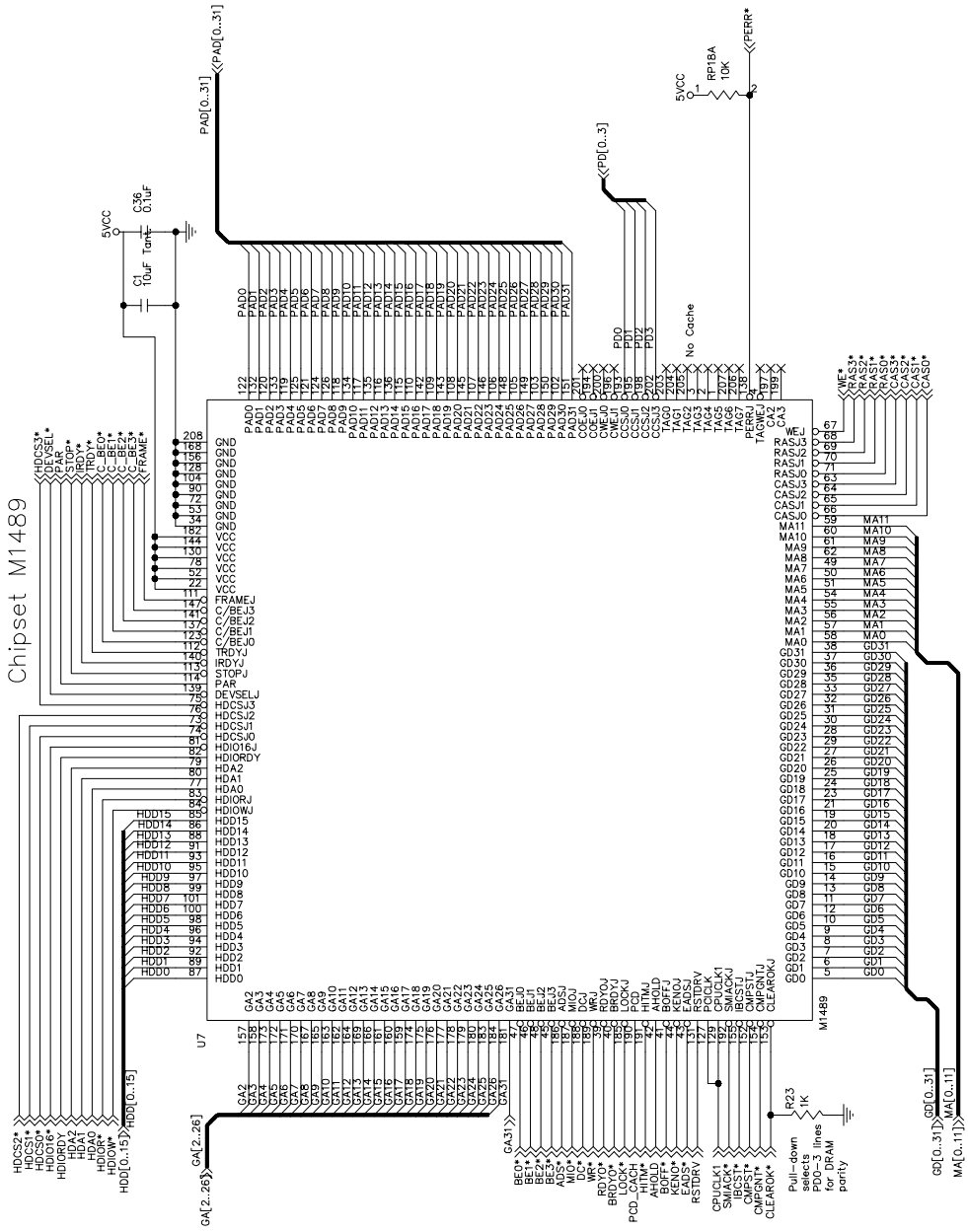
```
    // Should generate an Interrupt, with AAh in indexed register 1Fh
    printf ("Check value of 'Current Vector Register' after sending 55h\n");
        outportb(0xE7, 0x1F);
        in_val1 = inportb(0xE7);
    printf ("Output E7, 1Fh; returned value = %x\n", in_val1);

    // Interrupt pending (IP) bit (bit5) of index register 09h should be set
    printf("Check value of Port B command and status, is bit 5 set?\n");
        outportb(0xE7, 0x09);
        in_val1 = inportb(0xE7);
    printf ("Output E7, 09h; returned value = %x\n", in_val1);

    // To clear IP bit, write A0h to indexed register 09h
    printf ("Write Port B Command and Status register, clear IP\n");
        outportb(0xE7, 0x09);  //
        outportb(0xE7, 0xA0);
        outportb(0xE7, 0x09);  // Test if values are written to Z8536
        in_val1 = inportb(0xE7);
    printf ("Output E7, 09h and E7, A0h; returned value = %x\n", in_val1);

    // Current vector register should be FF again
    printf ("Check value of 'Current Vector Register' after clearing IP for port B\n");
        outportb(0xE7, 0x1F);
        in_val1 = inportb(0xE7);
    printf ("Output E7, 1Fh; returned value = %x\n", in_val1);


    /* ----------  End of test ----------- */
        in_val1 = inportb(0xE7);      // put state machine into state 1
        outportb(0xE7, 0x01);         // Disable ports A,B, & C
        outportb(0xE7, 0x00);

}
```

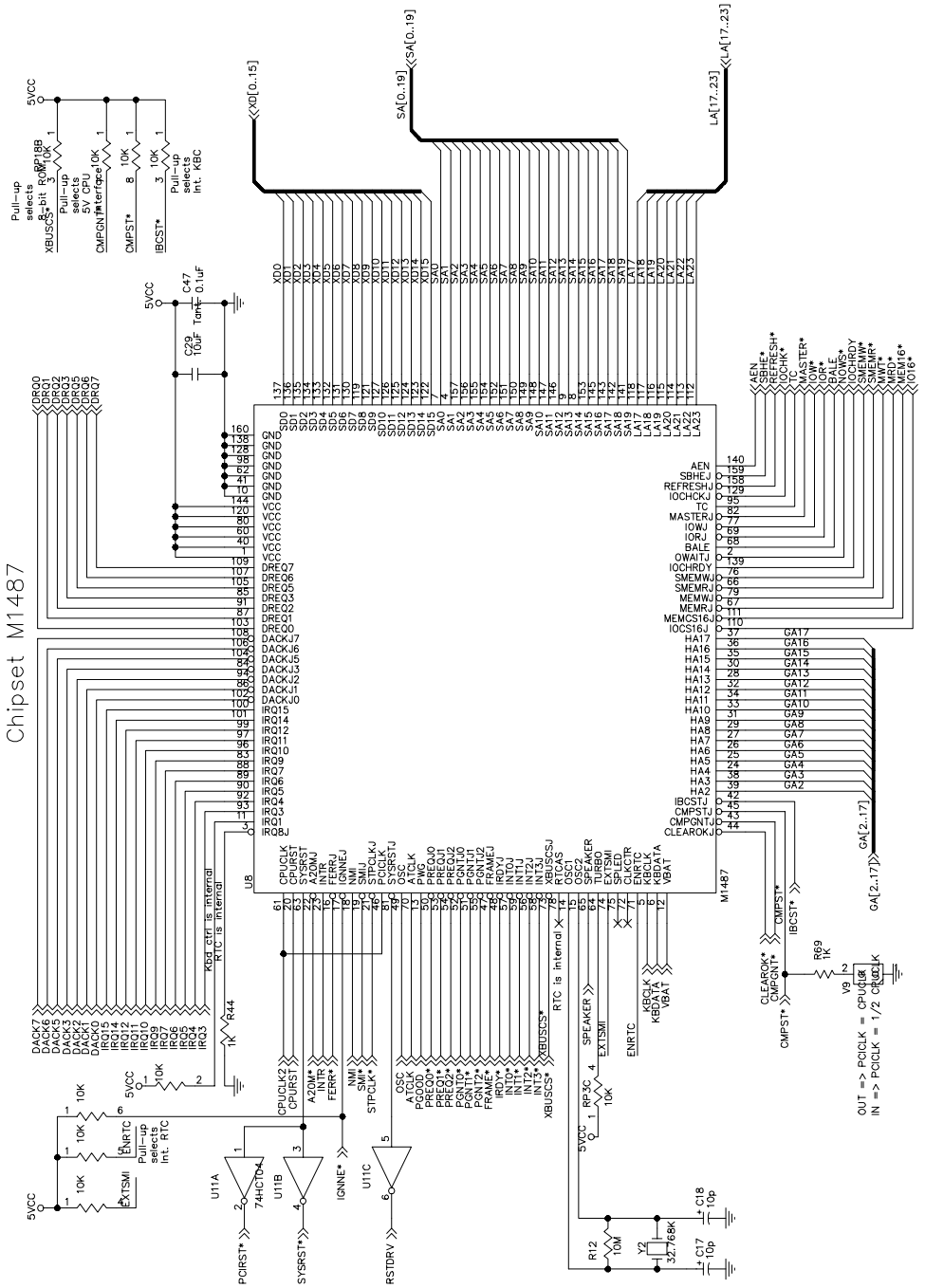
Appendix A — Schematic

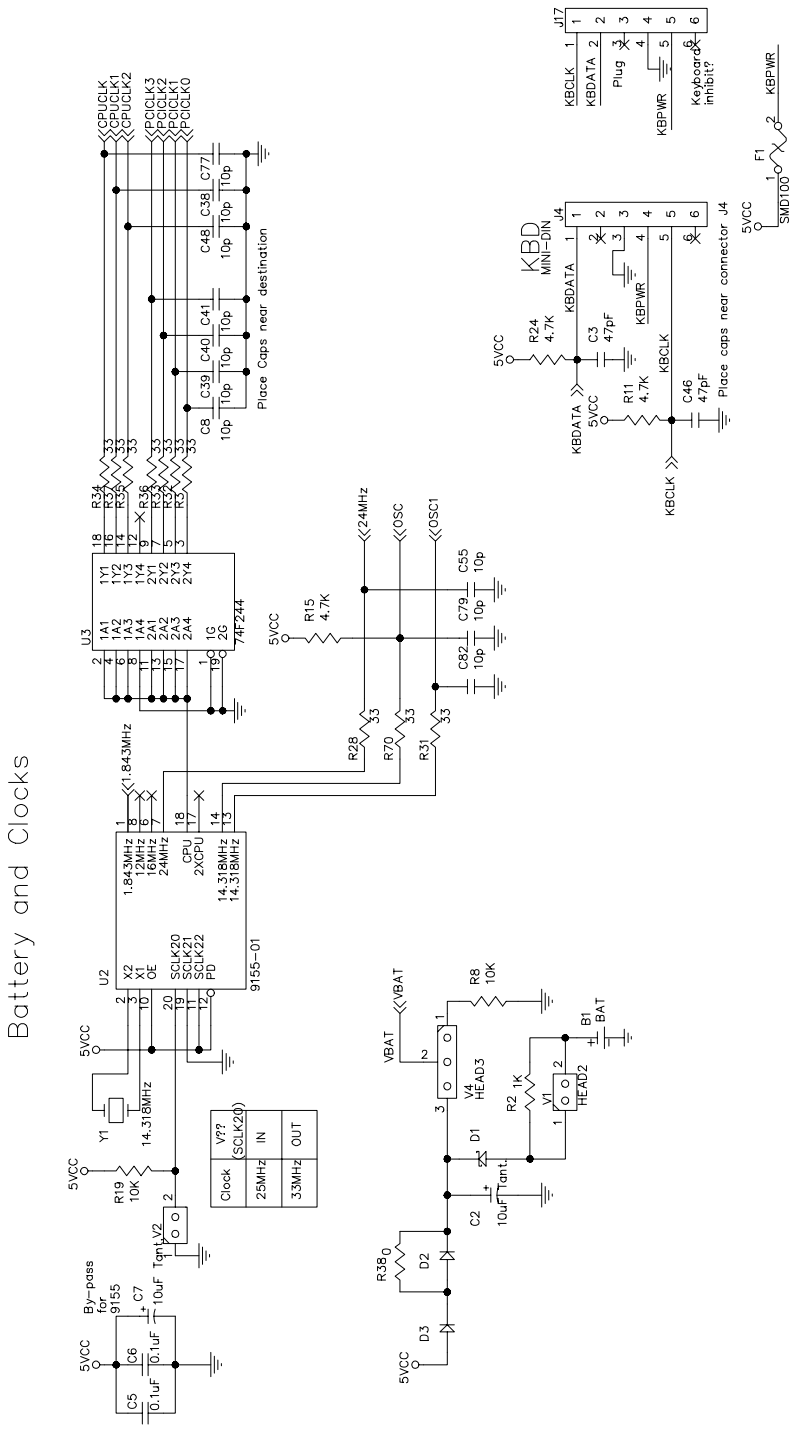
Rev. 3.00

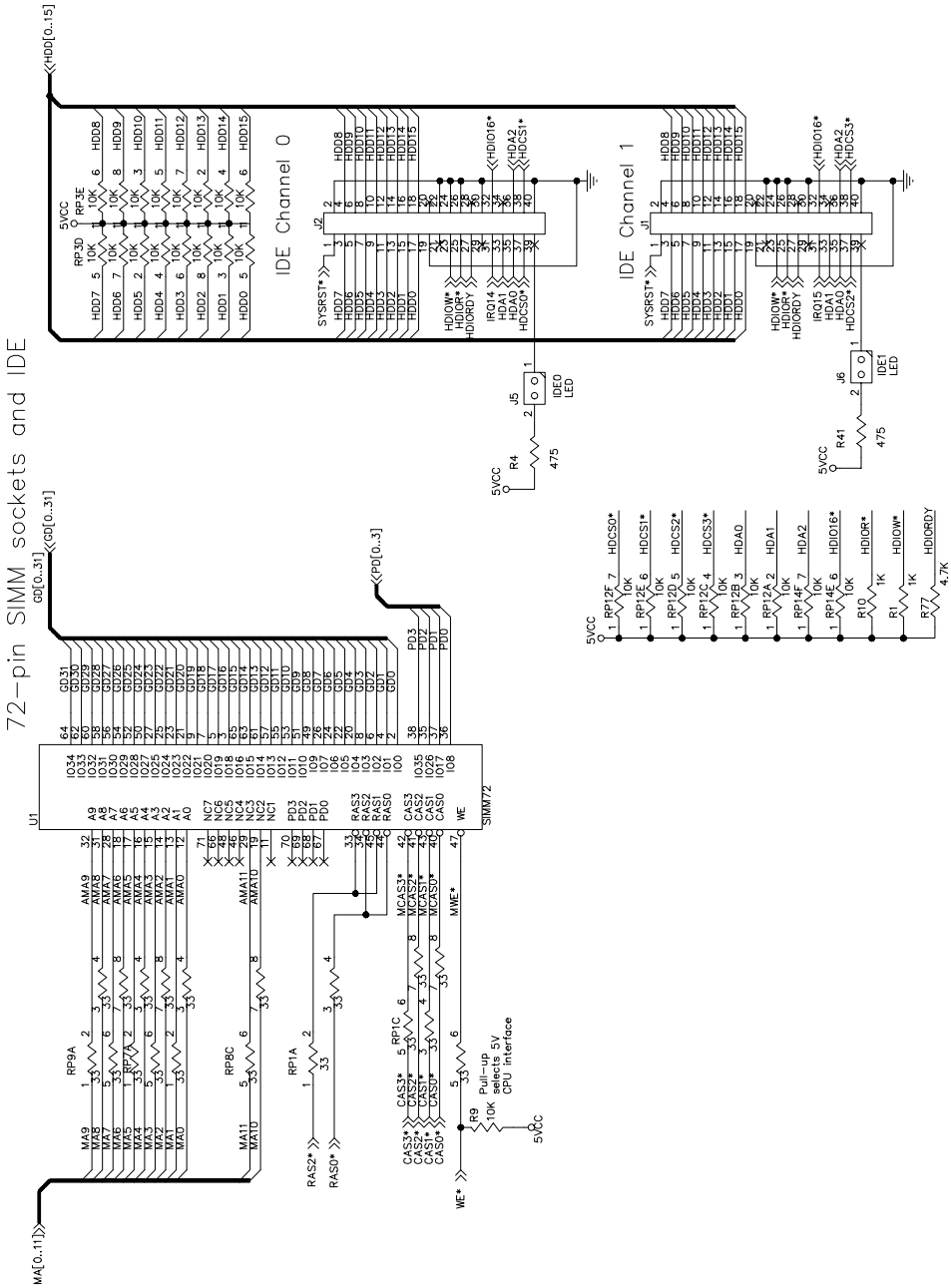


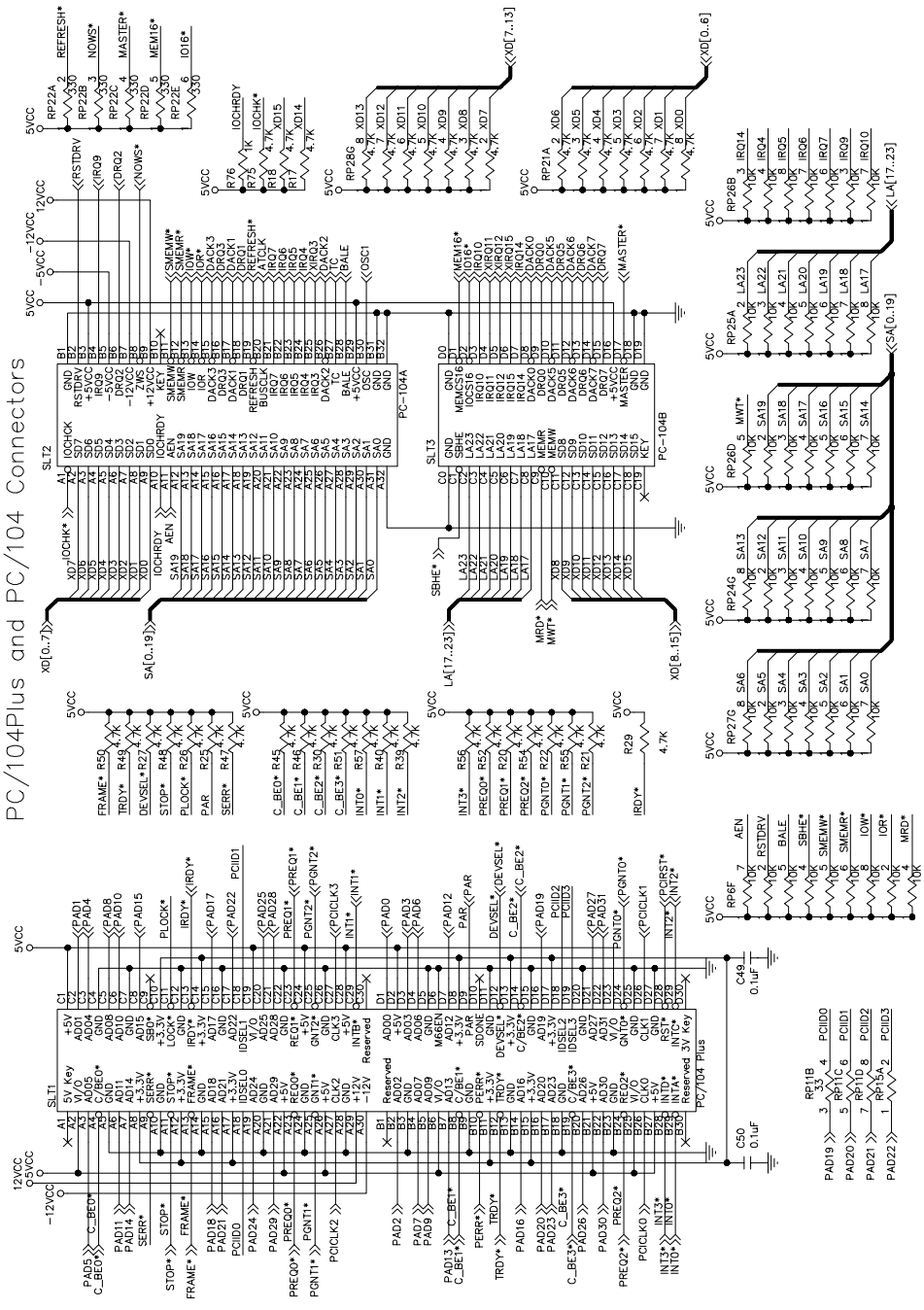

486/5x86 CPU
Jumper # V12 V13 V17 V14 V15 V16 V11 V18 V19
Intel DX/2 (A10) (A12) (B10) (B12) (C10) (C12) (C13) (B13) (R17)
Intel DX2 OUT 2-3 OUT IN 2-3 IN OUT OUT OUT
WB Intel DX4 OUT OUT OUT OUT 2-3 IN 2-3 OUT OUT
Cyrix/SGS/TI IBM DX/2/4 OUT 1-2 OUT OUT 1-2 OUT 1-2 ??? OUT
AMD DX2/4E OUT 2-3 IN 2-3 2-3 IN OUT OUT DX2=IN DX4=OUT
AMD 5x86 OUT 2-3 IN 2-3 2-3 IN OUT OUT IN
IBM/Cyrix 5x86 1-2 (WT) 2-3 (WB) 2-3 OUT IN 2-3 IN 2-3 OUT CLKMUL
5VCC
3VCC
PCD_CACH
PCD
CPURST
STPCLK*
SMIACK*
HITM*
SMI*
WR*
M/IO*
D/C*
W/R*
LOCK*
ADS*
FERR*
GA[1..31]
GD[0..31]
CPUCLK
CPURST
INTR
NMI
FLUSH*
BOFF*
AHOLD
EADS*
KEN0*
IGNNE*
BS16*
A20M*
RDY0*
BRDY0*
RP19A 10K
RP19B 10K
RP19C 10K
RP19D 10K
RP19E 10K
RP19F 10K
RP19G 10K
RP13A 10K
RP13B 10K
RP13C 10K
RP13D 10K
RP13E 10K
RP13F 10K
RP12G 10K
C11=PULLUP
R16 10K
C9 0.1uF
C16 10uF Tant.
C27 10uF Tant.
R42 113 1%
R43 200 1%
Actual Vout = 2.46V
Q1 1085
VO
ADJ
VI
U15
CLK
RESET
INTR
NMI(NMI,NC)
HOLD
BOFF#
AHOLD
EADS#
KEN#
FLUSH#
IGNNE#(IGNNE#)
BS16#
A20M#
RDY#
BRDY#
NC,INC_DX4
NC,STPCLK_DX4
UP#_24,CKM_M7
NC
NC,SRESET_DX4
NC,FERR#
NC,SM_DX4
WMRST,INC_DX4
SMIACT_DX4,NC
RPLVAL,NC_DX4
HITM#_M7,CLKMUL
INVAL,NC
NC,TDO
TDI
TCK
VOLDET
486DX PGA

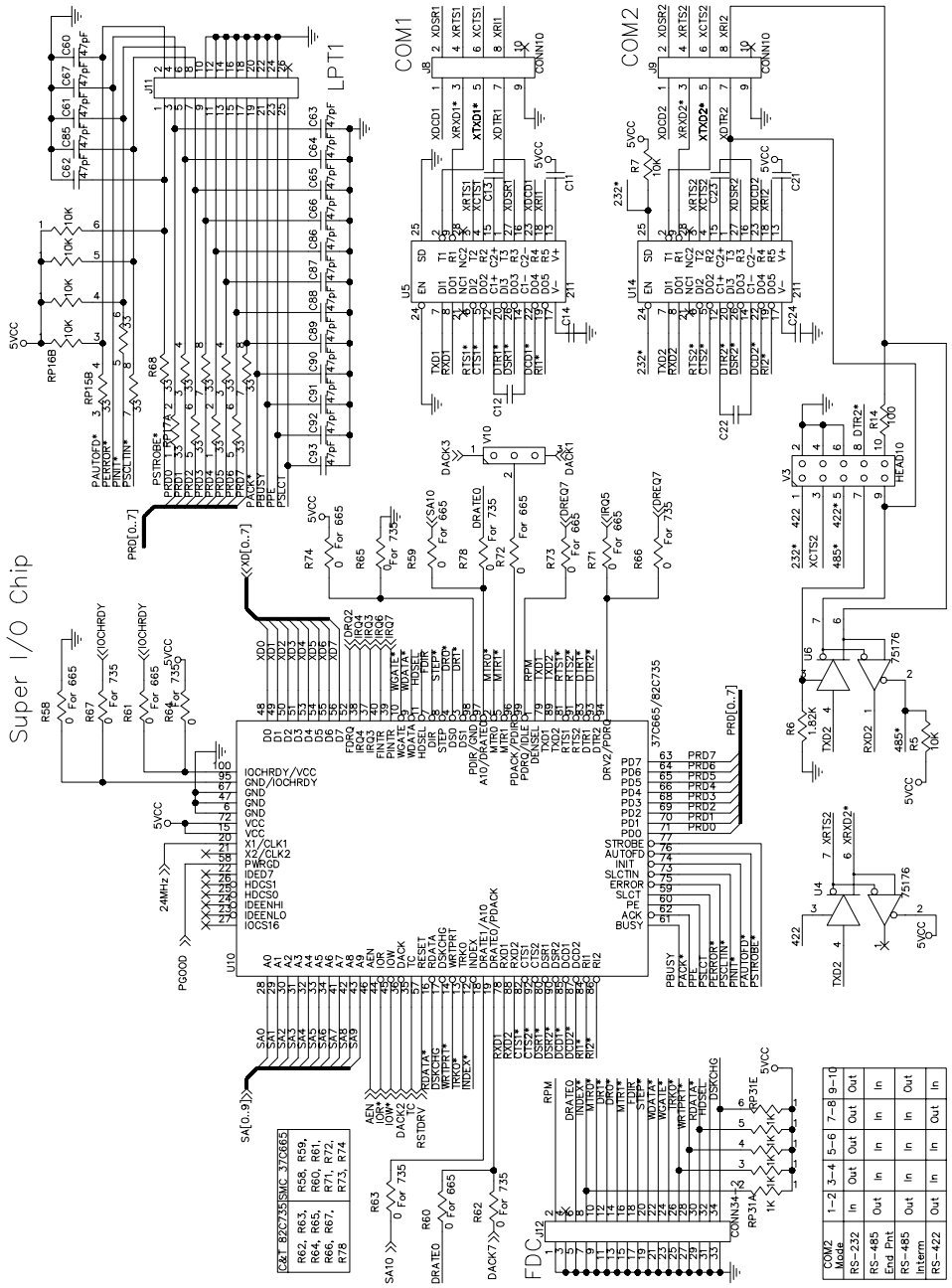

Chipset M1489
U7
M1489
5VCC
C1
10uF Tant
C36
0.1uF
RP18A
10K
R23
1K
PAD[0..31]
FD[0..3]
PERR*
No Cache
Pull-down selects PD0-3 lines for DRAM parity
HDD[0..15]
GA[2..26]
GD[0..31]
MA[0..11]

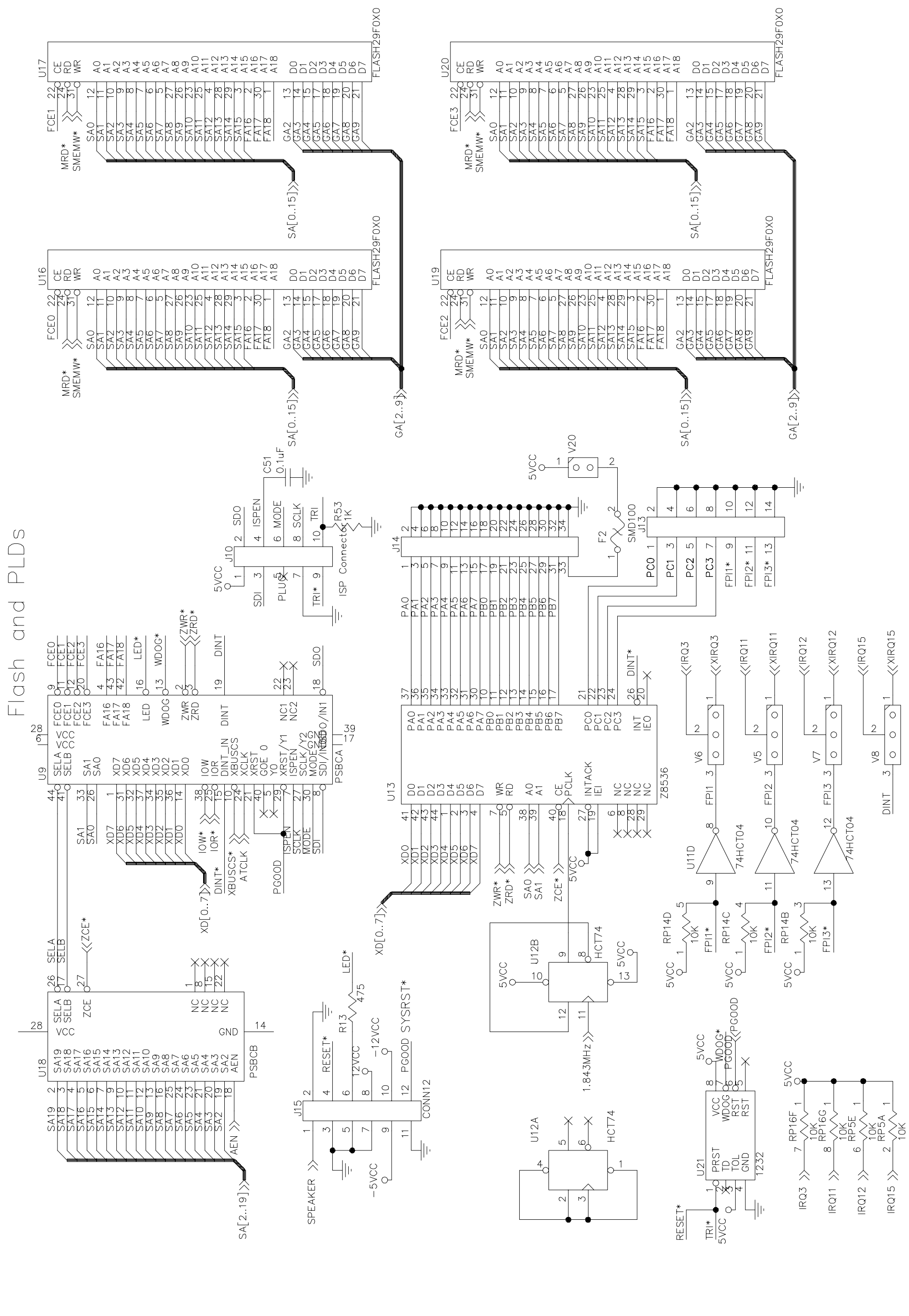

Chipset M1487
U8
M1487
XD[0..15]
SA[0..19]
LA[17..23]
GA[2..17]
5VCC
Pull-up selects 8-bit ROM
Pull-up selects 5V CPU Interface
Pull-up selects Int. KBC
Pull-up selects Int. RTC
Kbd ctrl is internal
RTC is internal
C47 0.1uF
C29 10uF
R44 1K
R69 1K
R12 10M
Y2 32.768K
C18 10p
C17 10p
U11A 74HCT04
U11B
U11C
RP3C 10K
V9
OUT => PCICLK = CPUCLK
IN => PCICLK = 1/2 CPUCLK


Battery and Clocks
CPUCLK
CPUCLK1
CPUCLK2
PCICLK3
PCICLK2
PCICLK1
PCICLK0
Place Caps near destination
U3
74F244
R34
R35
R36
R33
R32
R37
33
C8
C39
C40
C41
C48
C38
C77
10p
R15
4.7K
5VCC
24MHz
OSC
OSC1
C55
C79
C82
R28
R70
R31
U2
9155-01
1.843MHz
12MHz
16MHz
24MHz
14.318MHz
CPU
2XCPU
SCLK20
SCLK21
SCLK22
PD
X2
X1
OE
Y1
14.318MHz
R19
10K
Tant.
V2
By-pass
for
9155
C7
10uF
C6
0.1uF
C5
0.1uF
Clock
25MHz
33MHz
IN
OUT
V??
(SCLK20)
VBAT
R8
10K
V4
HEAD3
V1
HEAD2
R2
1K
D1
C2
10uF Tant.
B1
BAT
R38 0
D2
D3
KBD
MINI-DIN
J4
KBDATA
KBCLK
R24
4.7K
C3
47pF
R11
4.7K
C46
47pF
Place caps near connector J4
J17
Plug
KBPWR
Keyboard
inhibit?
F1
SMDT00
KBPWR

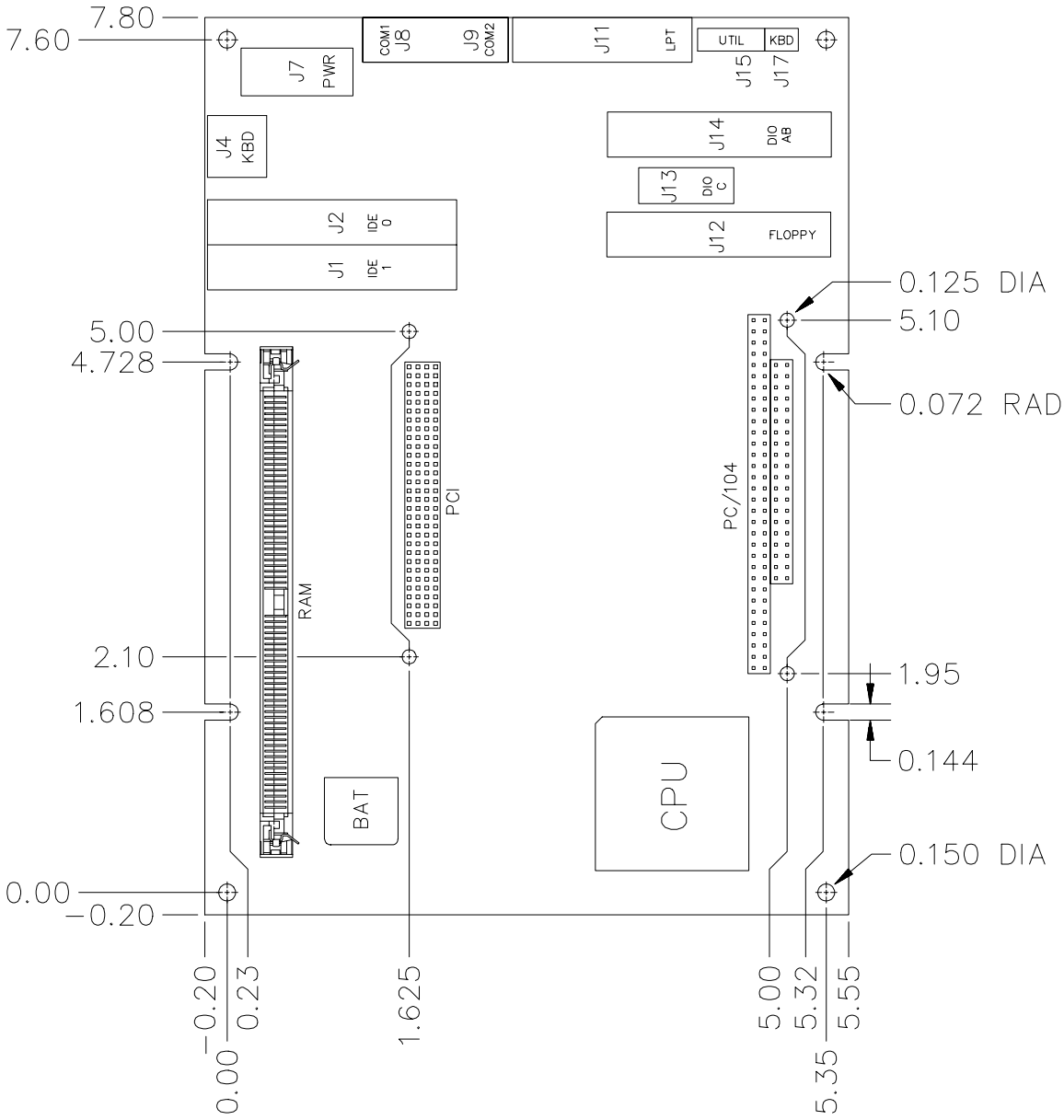

72-pin SIMM sockets and IDE
IDE Channel 0
IDE Channel 1
SIMM72
Pull-up selects 5V CPU interface
IDE0 LED
IDE1 LED


PC/104Plus and PC/104 Connectors
SLT1
PC/104 Plus
SLT2
SLT3
PC-104A
PC-104B
5VCC
12VCC
-12VCC
-5VCC
RP22A
RP22B
RP22C
RP22D
RP22E
REFRESH*
NOWS*
MASTER*
MEM16*
IO16*
RSTDRV
IRQ9
DRQ2
IOCHRDY
IOCHK*
RP28G
RP21A
XD[7..13]
XD[0..6]
RP25A
RP26B
RP26D
RP24G
RP27G
RP29F
LA[17..23]
SA[0..19]
XD[0..15]
SBHE*
MRD*
MWT*
MEMW*
MEMR*
IOW*
IOR*
AEN
BALE
SMEMW*
SMEMR*
RP11B
C49
C50
0.1uF
PCIID0
PCIID1
PCIID2
PCIID3


Super I/O Chip
LPT1
COM1
COM2
FDC
37C665/82C735
C&T 82C735/SMC 37C665
R62, R63, R64, R65, R66, R67, R78
R58, R59, R60, R61, R72, R73, R74
COM2 Mode
RS-232
RS-485
End Pnt
RS-485
Interm
RS-422
1-2
3-4
5-6
7-8
9-10
In
Out


Flash and PLDs
FLASH29F0X0
U16
U17
U19
U20
U9
U13
Z8536
U18
U21
1232
J15
CONN12
J10
ISP Connector
J14
J13
V20
SMD100
U11D
74HCT04
U12A
U12B
HCT74
1.843MHz

Appendix B — Physical Dimensions



Not to scale. All dimensions in inches.

Figure 10. VSBC Physical Dimensions

Index