TOP View

BOTTOM View

GENERAL DESCRIPTION

TD1205P Tracker module feature the SIGFOX™ high efficiency Gateway which offer high interference immunity performances on ISM band. It includes GNSS, Accelerometer and Hall-Effect sensors in order to provide a high efficiency tracking solution in 30x28x10.5mm size including antennas.

BOARD FEATURES

- 2.3V to 3.6V Power supply
- 2.8 µA Idle state consumption
- 30x38x10.5mm size with antenna
- Green and Red LED indications

KEY SIGFOX MODEM FEATURES

- SIGFOX™ transceiver certified
- 145 dB maximum link budget
- (G)FSK, 4(G)FSK, GMSK, OOK modulation
- Receive sensitivity =-126 dBm
- 20µA RX (windowed mode)
- 50 mA TX @ radiated +16 dBm

KEY SENSORS FEATURES

- **GNSS Receiver with active antenna**
  - Multi-GNSS supported: GPS/GLONASS
  - SBAS augmentation services
  - 12 µA Backup / 29 mA Acquisition
  - 56-channels engine with high sensitivity
  - -162 dBm Tracking / -148 dBm Cold start
- **Ultra-low power 3D Accelerometer**
  - Up to ±16g full scale
- **Ultrasensitive Hall-Effect**
  - Magnet pole independence
  - Operation point down to 20 Gauss
  - 2.8 µA consumption

APPLICATIONS

- SIGFOX™ transceiver (fully certified)
- Geolocation and Tracking
- Universal Timing and Synchronization
- People and pets geolocation
- Sensor Network

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Description

Telecom Design's TD1205P devices are high performance, low current SIGFOX™ gateways, RF transceiver and GPS receiver with integrated antennas.

The combination of a powerful radio transceiver, a state-of-the-art ARM Cortex M3 baseband processor and a high-efficiency GPS receiver achieves extremely high performance while maintaining ultra-low active and standby current consumption. The TD1205P device offers an outstanding RF sensitivity of –126 dBm while providing an exceptional output power of up to +14 dBm with unmatched TX efficiency.

The TD1205P device versatility provides the gateway function from a local Narrow Band ISM network to the long-distance Ultra Narrow Band SIGFOX™ network at no additional cost.

Moreover the fully integrated on-board GPS receiver combines outstanding sensitivity with ultra-low power which allows you to achieve excellent accuracy and Time-To-First-Fix performance. Combining the SIGFOX™ network possibilities with accurate geolocation will give you access to a brand new world of embedded applications.

The TD1205P also embeds an ultra-low power 3D accelerometer with motion and free fall detection to further extend application range.

Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. Eventually the integrated antennas for both SIGFOX™ and GPS make the TD1205P a turnkey solution which does not require any additional design.

TABLE OF CONTENTS

1 General Description

1.1 Simplified Block Diagram

1.1.1 Block Diagram
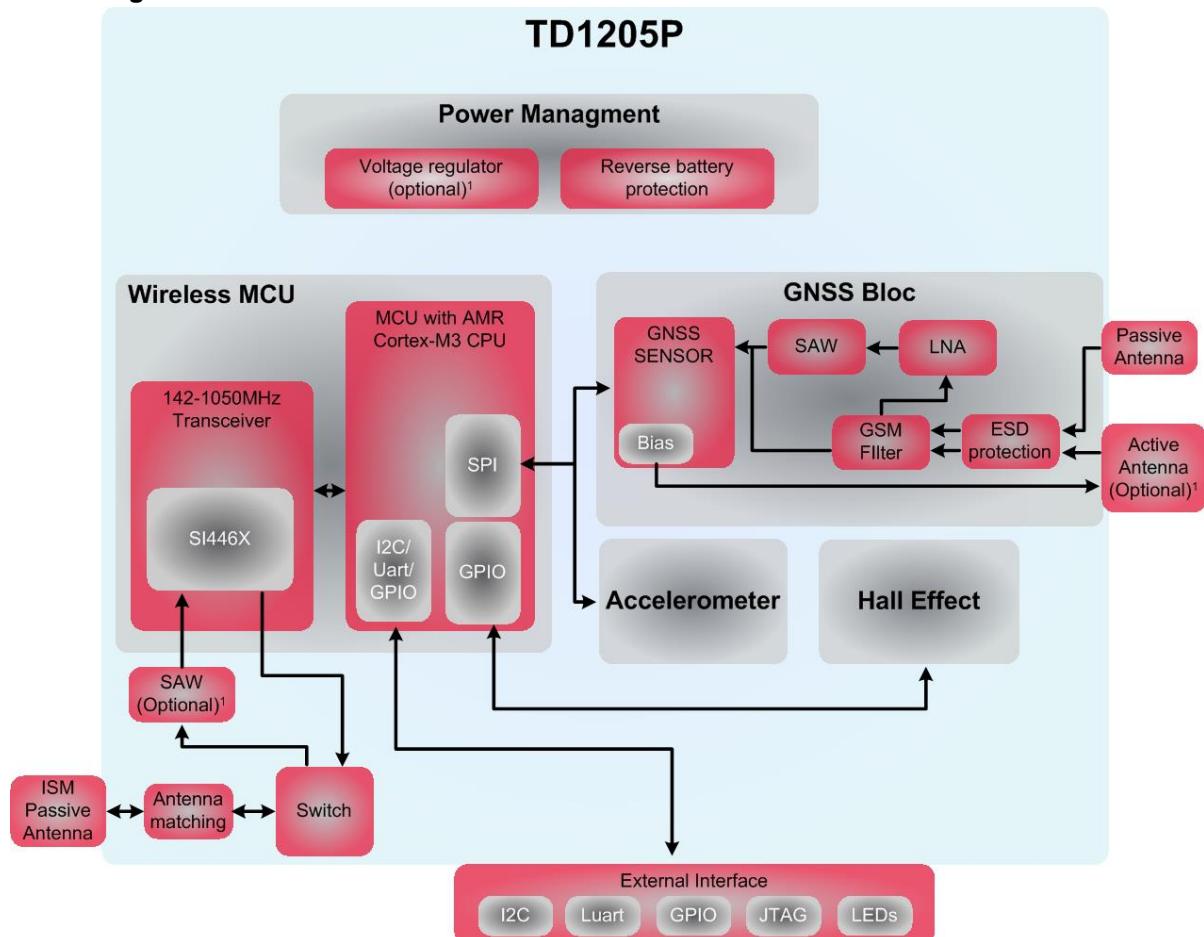
Figure 1. TD1205P block diagram

1.1.2 TD1205P Options

RX SAW filter, Voltage regulator and active GPS antenna are option and can be only used like specific requests. For any more information, please contact Telecom Design.

1.2 Pin Diagram
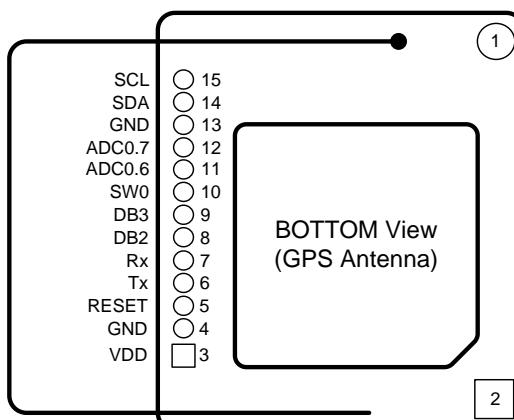
Figure 2. TD1205P pin diagram

1.3 Pin Description
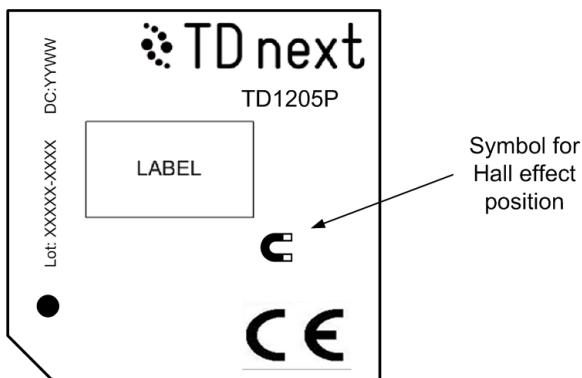
Table 1. Pin definition

Pin	Pin Name	I/O	Principal function	Remarks	MCU pin name
1	BAT -	GND	Battery Negative Input		-
2	BAT +	VDD	Battery Positive Input		-
3	VDD	VDD	Supply Voltage Input	Not required if a battery is used on BATx pins	-
4	GND	GND	Ground		-
5	RESET	I	Active Low RESET input signal		-
6	TX	O	Low-Power UART Data Transmit data	See note 1	PC6
7	RX	I	Low-Power UART Data Receive data	See note 1	PC7
8	DB2	I/O	Serial Debug SWDIO (SWD Data I/O) Signal	See note 1	PF1
9	DB3	I	Serial Debug SWDCLK (SWD Clock) Signal	See note 1	PF0
10	SW0	I/O	SWDO (SWD trace) Output Signal	See note 1	PC15
11	ADC0.6	I/O	ADC analog input #6	See note 1	PD6
12	ADC0.7	I/O	ADC analog input #7	See note 1	PD7
13	GND	I/O	Ground		-
14	SDA	I/O	Master Slave I²C serial data	See note 1	PE0
15	SCL	I/O	Master Slave I²C serial clock	See note 1	PE1

Notes:

This pin may be configured to perform various functions. To obtain a list of the possible alternate functionalities, please refer to the EZR32LG230 datasheet.

1.4 Package Marking

Figure 3. Package marking

Lot : XXXXX-XXXX : TD Next Lot No

DC : YYWW : Date code

Label : Label with QR code and SIGFOX^{TM} ID

1.5 Definition of Test Conditions

1.5.1 Production Test Conditions:

- T_A = + 25°C

- V_{DD} = +3.3 VDC

- Production test schematics (unless noted otherwise)

- All RF input and output levels referred to the pins of the TD1205P module

1.5.2 Qualification Test Conditions:

- T_A = -30 to +75°C (Typical T_A = 25°C)

- V_{DD} = +2.3 to 3.6 VDC (Typical V_{DD} = 3.3 VDC)

- Using TX/RX Split Antenna reference design or production test schematic

- All RF input and output levels referred to the pins of the TD1205P module

2   Electrical Specifications

2.1   ESD Notice

TD1205P modules are ESD sensitive devices, appropriate precautions should be taken during TD1205P assembly in the final product.

Mechanical impact and harsh tools must be avoided during TD1205P assembly in the final product.

2.2   Absolute Maximum Rating

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX VRF-peak on RF pin. Caution: ESD sensitive device.

Table 2. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage	0	3.6	V
V_{Bat+} to V_{Bat-}	Supply Voltage of External Battery	0	3.6	V
V_{DIN}	Voltage on Digital Inputs	0	V_{DD}	V
V_{AIN}	Voltage on Analog Inputs	0	V_{DD}	V
P_{IN_ISM}	RX Input Power	-	+10	dBm
P_{IN_GPS}	GPS Input Power	-	+15	dBm
T_A	Operating Ambient Temperature Range	-30	+75	°C
T_{STG}	Storage Temperature Range	-40	+125	°C
T_{SOL}	Maximum soldering Temperature	-	260	°C

2.3 DC Power characteristics

Table 3. DC Power Supply Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range[2]		2.3	3.3	3.6	V
I_{Sleep}	Power Saving Mode[2]	Sleep current using the 32 kHz crystal	-	2.8	-	µA
I_{Wakeup}	Standby Mode with Hall Effect	10% duty cycle Hall Effect activation	-	4.5	-	µA
I_{Active}	Active CPU Mode	CPU performing active loop @ 14 MHz	2.55	3.0	3.45	mA
I_{RX}	Active CPU Mode + RX Mode Current[2]		-	13	16	mA
I_{TX_max}	Active CPU Mode + TX Mode Current[2]	+16 dBm radiated output power 868 MHz, 3.3 V	-	50	-	mA
V_{V_IO}	Vsupply for optional external active antenna		$0.8V_{DD}$	$0.95V_{DD}$	-	V
I_{V_IO}	Output Current for optional external active antenna		-	-	6	mA
I_{ACQ}	GPS Acquisition		-	29	-	mA
I_{TRA}	GPS Tracking		-	23	-	mA
I_{BCKP}	GPS Backup		-	12	-	µA
IHE_{DC}	Consumption of Hall Effect	Standard TD1205P utilization	-	1	-	µA
I_{green}	Green Led		-	320	-	µA
I_{red}	Red Led		-	700	-	µA

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.
2. Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.

2.4 RF Power characteristics

2.4.1 Transmitter RF Characteristics

The table below give TX RF performance of TD1205P. This module offer performance higher than +14dBm in order to overcome casing influence. It is the responsibility of the user to respect ETSI standard requirement, especially about maximum authorized radiated output power. The desired output power can be set like AT command (cf. TDnext RF Modules Reference Manual) or using the SDK C API.

Table 4. Transmitter RF Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TX}	TX Frequency Range[2]		868.0	-	869.7	MHz
Δf	Modulation Deviation Range[3]	868.0-869.7 MHz	-	1.5	-	MHz
F_{RES}	Modulation Deviation Resolution[3]	868.0-869.7 MHz	-	24.8	-	Hz
F_{ERR}	Frequency Error[2]	868.0-869.7 MHz, 3.3V, -20°C 868.0-869.7 MHz, 3.3V, 25°C 868.0-869.7 MHz, 3.3V, 55°C	-3 -2 -3	- - -	+3 +2 +3	kHz
P_{TX}[2]	Maximum Radiated power	V_{DD} = 3.3 V, 25°C, 50mA	-	16	-	dBm
P_{TP}	Transient Power[2]	868.0-869.7 MHz, 25°C, 3.3 V, BR=4.8kbps, FD=2.5kHz, cable loss 0.2 dB, antenna gain 2 dBi	-	-	3	dBm
P_{ACP}	Adjacent Channel Rejection[2]	BR=4.8kbps, FD=2.5kHz, Offset=+/-25kHz	-	-55	-	dB
P_{OB_TX}	Spurious Emissions[2]	868.0-869.7 MHz, 3.3 V, 25°C, BR 4.8kbps, dev 2.5kHz, <30MHz <1GHz >1GHz	- - -	-82 -70 -48	- - -	dBm

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
2. *Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
3. *Guaranteed by component specification.*

2.4.2 Receiver RF Characteristics

Table 5. Receiver RF Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{RX}	RX Frequency Range[2]		868.0	-	869.7	MHz
F_{RES}	Synthesizer Frequency Resolution[3]	868.0-869.7 MHz	-	24.8	-	Hz
BI	Blocking[2,4]	Offset=+/-2MHz Offset=+/-10MHz	-	68 82	-	dB
P_{OB_RX}	Spurious Emissions[2]	From 9 kHz to 1 GHz From 1 GHz to 6 GHz	-	-84 -70	-	dBm
P_{RX}	GFSK RX Sensitivity[3] BER<0.1%, BT=0.5	FDA=0.25 kHz, BR=0.5 kbps FDA=9.6 kHz, BR=2.4 kbps FDA=20 kHz, BR=40 kbps FDA=50 kHz, BR=100 kbps FDA=62.5 kHz, BR=125 kbps FDA=250 kHz, BR=500 kbps FDA=1.25 kHz, BR=1 Mbps	-	-126 -110 -110 -106 -105 -97 -88	-	dBm
P_{RX_OOK}	OOK RX Sensitivity[3] BER<0.1%, BT=0.5, PN15 data	BW=350kHz, BR=4.8kbps BW=350kHz, BR=40kbps BW=350kHz, BR=120kbps	-	-109 -104 -99	-	dBm
RES_{RSSI}	RSSI Resolution[3]		-0.5	-	+0.5	dB

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
2. *Guaranteed by qualification. Qualification test conditions are listed in the "Qualification Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
3. *Guaranteed by component specification.*
4. *The typical blocking values were obtained while seeking for EN 300-220 Category 2 compliance only. The typical value specified in the component datasheet are -75 dB and -84 dB at 1 and 8 MHz respectively, with desired reference signal 3 dB above sensitivity, BER = 0.1%, interferer is CW, and desired is modulated with 2.4 kbps, ∆F = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz. The RF component manufacturer provides a reference design featuring a SAW filter which is EN 300-220 Category 1 compliant. Please contact Telecom Design for more information on EN 300-220 Category 1 compliance.*

2.5   Digital characteristics

Table 6. All Digital I/O DC & AC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IOIL}	Input Low Voltage[2]		-	-	$0.3V_{DD}$	V
V_{IOIH}	Input High Voltage[2]		$0.7V_{DD}$	-	-	V
V_{IOOH}	Output High Voltage[2] VDD=3.0V	6 mA, Std Drive Strength 20 mA, High Drive Strength	$0.95V_{DD}$ $0.9V_{DD}$	- -	- -	V
V_{IOOL}	Output Low Voltage[2] VDD=3.0V	6 mA, Std Drive Strength 20 mA, High Drive Strength	-	-	$0.05V_{DD}$ $0.1V_{DD}$	V
I_{IOLEAK}	Input Leakage Current[2]	High Impedance I/O connected to GND or V_{DD}	-25	-	+25	nA
R_{PU}	I/O Pin Pull-Up Resistor[2]		-	40	-	kΩ
R_{PD}	I/O Pin Pull-Down Resistor[2]		-	40	-	kΩ
R_{IOESD}	Internal ESD Series Resistor[2]		-	200	-	Ω
$t_{IOGLITCH}$	Pulse Width of Pulses to be Removed by the Glitch Suppression Filter[2]		10	-	50	ns
t_{IOOF}	Output Fall Time[2]	0.5 mA / C_L = 12.5 to 25 pF 2 mA / C_L = 350 to 600 pF	$20+0.1C_L$ $20+0.1C_L$	-	250 250	ns
V_{IOHYST}	I/O Pin Hysteresis (V_{IOTHR+} - V_{IOTHR-})[2]	V_{DD} = 2.3 to 3.6 V	$0.1V_{DD}$	-	-	V

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
2. *Guaranteed by component specification.*

2.6 ADC and DAC characteristics

2.6.1 ADC Characteristics

Table 7. ADC DC & AC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADCIN}	Input Voltage Range[2]	Single Ended mode Differential mode	0 $-V_{REF}/2$	- -	V_{REF} $V_{REF}/2$	V
$V_{ADCCMIN}$	Common Mode Input Range[2]		0	-	V_{DD}	V
I_{ADCIN}	Input Current[2]	2 pF Sampling Capacitors	-	100	-	nA
$CMRR_{ADC}$	Analog Input CMRR[2]		-	65	-	dB
I_{ADC}	Average Active Current[2]	10ksps/s, 12 bit, Internal 1.25V ref Warmup Mode = 0 Warmup Mode = 1 Warmup Mode = 2	- - -	67 63 64	- - -	μA
I_{ADCREF}	Current Consumption of Internal Voltage Reference[2]		-	65	-	μA
C_{ADCIN}	Input Capacitance[2]		-	2	-	pF
R_{ADCIN}	Input ON Resistance[2]		1	-	-	MΩ
$R_{ADCFILT}$	Input RC Filter Resistance[2]		-	10	-	kΩ
$C_{ADCFILT}$	Input RC Filter/Decoupling Capacitance[2]		-	250	-	fF
f_{ADCCLK}	ADC Clock Frequency[2]		-	-	13	MHz
$t_{ADCCONV}$	Conversion Time[2]	6 bit 10 bit 12 bit	7 11 13	- - -	- - -	ADC CLK Cycles
t_{ADCACQ}	Acquisition Time[2]	Programmable	1	-	256	ADC CLK Cycles
$t_{ADCACQVDD3}$	Required Acquisition Time for $V_{DD}/3$ Reference[2]		2	-	-	μs
$t_{ADCSTART}$	Startup Time of Reference Generator and ADC Core	NORMAL Mode[2] KEEPADCWARM Mode[2]	- -	5 1	- -	μs
$V_{ADCOFFSET}$	Offset Voltage after calibration[2]	single ended mode differential mode	- -	0.3 0.3	- -	mV
$TGRAD_{ADCTH}$	Thermometer Output Gradient[2]	In mV/°C unit In ADC Codes/ °C unit	- 	-1.92 -6.3	- 	mV/°C C/°C
DNL_{ADC}	Differential Non-Linearity (DNL) [2]		-0.7		+0.7	LSB
INL_{ADC}	Integral Non-Linearity (INL)[2]	End Point Method	-1.2		+0.2	LSB
MC_{ADC}	No Missing Codes[2]		11.999[3]	12	-	bits
$GAIN_{ED}$	Gain Error Drift[2]	1.25V Reference 2.25V Reference	- -	0.01[4] 0.01[4]	0.033[5] 0.03[5]	%/°C
		1.25V Reference 2.25V Reference	0.07[5] -	0.2[4] 0.2[4]	- 0.62[5]	LSB/°C

Notes:

1. *All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.*
2. *Guaranteed by component specification.*

3. On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbor codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

4. Typical numbers given by abs(Mean) / (85 - 25).

5. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

2.6.2 ADC Characteristics

Table 8. DAC DC & AC Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DACOUT}	Output Voltage Range[2]	V_{DD} voltage reference, Single Ended	0	-	V_{DD}	V
V_{DACCM}	Output Common Mode Voltage Range[2]		0	-	V_{DD}	V
I_{DAC}	Active Current Including References for 2 Channels [2]	500 ksps/s 12 bit 500 ksps/s 12 bit 100 ksps/s 12 bit NORMAL	- - -	400 200 38	- - -	µA
SR_{DAC}	Sample Rate[2]		-	-	500	ksps
f_{DAC}	DAC Clock Frequency[2]	Continuous Mode Sample/Hold Mode Sample/Off Mode	- - -	- - -	1000 250 250	kHz
$CYC_{DACCONV}$	Clock Cycles per Conversion [2]		-	2	-	DAC CLK Cycles
$t_{DACCONV}$	Conversion Time[2]		2	-	-	µs
$t_{DACSETTLE}$	Settling Time[2]		-	5	-	µs
SNR_{DAC}	Signal to Noise Ratio (SNR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	- -	58 59	- -	dB
$SNDR_{DAC}$	Signal to Noise-Pulse Distortion Ratio (SNDR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	- -	57 54	- -	dB
$SFDR_{DAC}$	Spurious-Free Dynamic Range(SFDR)[2]	500 ksps, 12 bit, single ended internal 1.25V reference internal 2.5V reference	- -	62 56	- -	dB
$V_{DACOFFSET}$	Offset Voltage after calibration[2]	single ended mode	-	2	-	mV
DNL_{DAC}	Differential Non-Linearity[2]		-1	-	+1	LSB
INL_{DAC}	Integral Non-Linearity[2]		-5	-	5	LSB
MC_{DAC}	No Missing Codes[2]		-	12	-	bits

Notes:

1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in the "Production Test Conditions:" section in "1.5 Definition of Test Conditions" on page 10.

2. Guaranteed by component specification.

2.7 SENSORS characteristics

2.7.1 Accelerometer Characteristics

Table 9. Accelerometer mechanical characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FS	Measurement range		±2	-	±16	g
So	Sensitivity		1	-	12	mg/digit
TCSo	Sensitivity change vs temperature	FS=±2g	-	0.01	-	%/°C
TyOff	Typical zero-g level offset accuracy	FS=±2g	-	±40	-	mg
TCOff	Zero-g level change vs temperature	Max delta from 25°C	-	±0.5	-	mg/°C
An	Acceleration noise density	FS=±2g	-	220	-	µg/sqrt(Hz)

Notes:
1. *Guaranteed by component specification.*

2.7.2 Hall Effect Characteristics

Table 10. Hall Effect Magnetic Characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B_{OPS}	Operate point of South pole		20	28	40	G
B_{OPN}	Operate point of North pole		-40	-28	-20	G
B_{RPS}	Release point of South pole		10	20	-	G
B_{RPN}	Release point of North pole		-	-20	-10	G
B_{HYS}	Hysteresis	$|B_{OPx} - B_{RPx}|$	5	8	-	G

Notes:
1. *Guaranteed by component specification.*

It is recommended to use circular magnet with Br superior at 1000mT in order to active Hall effect with maximum distance between magnet and hall effect of 10 mm. The magnet must be place like is illustrated on Figure 4.
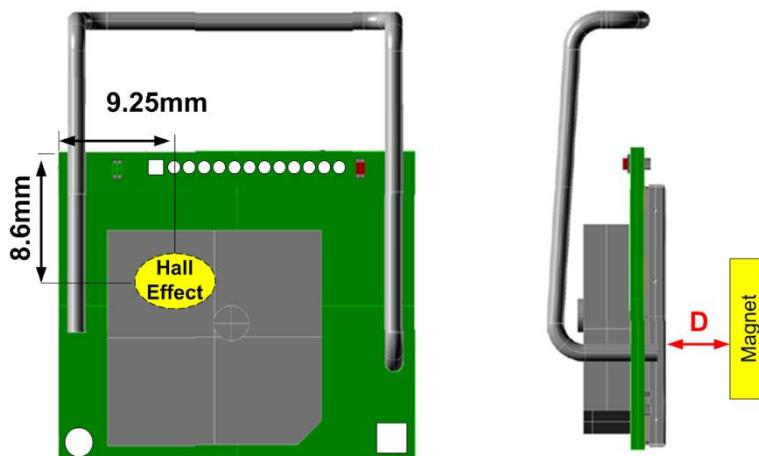

Figure 4. Hall effect position

2.8 Indicative energy requirements

The following tables show indicative energy requirements for key-point functionalities of a TD1205P module based on Telecom Design's software library. All indicated values are for V_{DD} = 3.0V.

Table 11. Indicative Average current of TD1205P blocs

Name	Function	Conditions	Period	Typ	Units
I_{dle}	Idle state	Polling Hall effect function included	NA	3.5	µA
LAN	LAN RF Reception	Windowed mode per sec	1 per sec	20	µA
LC SFX	Sigfox™ Transmission Low consumption mode	Transmission of 12 payload bytes per day	1 per day	3.6	µA
HP SFX	Sigfox™ Transmission High power mode	Transmission of 12 payload bytes per day	1 per day	6.2	µA
MOV	3D movement detection	Accelerometer	1 per hour	4	µA
GPS	GPS position acquisition	Cold start fix obtained in 30 seconds	1 per day	10	µA

Table 12. Indicative battery life for typical user case

The following table shows indicative battery life for some typical user-cases based on the TD1205P module with passive antenna GPS and Sigfox™ Transmission Low consumption mode.

User case					Average consumption (µA)	Annual consumption (mAh)	Battery	Lifetime
LC SFX Nbr/day	HP SFX Nbr/day	LAN Hour/day	GPS Nbr/day	MOV Nbr/day				
1	0	0	0	0	7.1	62	CR2	7 years
							CR123A	12 years
0	1	0	0	0	9.7	85	CR2	6 years
							CR123A	9 years
1	0	12	0	0	17.1	150	CR2	3 years
							CR123A	5 years
0	1	12	0	0	19.7	173	CR2	2.8 years
							CR123A	4.8 years
1	0	0	1	5	18	158	CR2	3 years
							CR123A	5 years
0	1	0	1	5	20.5	180	CR2	2.5 years
							CR123A	4.5 years

Notes:
1. Assuming a 3V battery with 0.16% discharge per month.
2. With a 12-byte payload and +14dBm output power.
1. Assuming a 30 seconds cold start fix. Transmission of longitude, latitude and altitude information.
2. Assuming a 5 second hot start fix and 12 long-distance movements per day. Transmission of longitude, latitude and altitude information.

3   Functional Description

The TD1205P devices are high-performance, low-current, wireless SIGFOX™ gateways, RF transceiver, GPS receiver, accelerometer and Hall Effect sensors with integrated antennas. The wide operating voltage range of 2.3–3.6 V and low current consumption make the TD1205P an ideal solution for geolocation battery-powered applications.

The TD1205P operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to downconvert the 2-level FSK/GFSK or OOK/ASK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering, demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the baseband CPU by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 0.123 kbps to 1 Mbps. The TD1205P operates in the frequency bands of 868.0–869.7 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The power amplifier (PA) supports output power up to +14 dBm with very high efficiency, consuming only 30 mA at +10 dBm. The integrated power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure.

As both the local Narrow Band ISM network and the long-distance Ultra Narrow Band SIGFOX™ network can be addressed seamlessly, the TD1205P device provides a natural gateway function at no additional cost. Thus, the same TD1205P module can be used both for local RF communication with peer modules, and also connect to the wide-area SIGFOX™ RF network.

Featuring an AES encryption engine and a DMA controller, the powerful 32-bit ARM Cortex-M3 baseband processor can implement highly complex and secure protocols in an efficient environmental and very low consumption way. This unique combination of a powerful 32-bit ARM Cortex-M3 CPU including innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of intelligent peripherals allows any application to connect to the SIGFOX™ network.

The application shown in Figure 1 shows the minimum interconnection required to operate the TD1205P module. Basically only a battery supply has to be connected between pin 1 and pin 2. Pins 3 to 9 can be used to flash new software into the TD1205P module and pins 6 to 9 give access to several peripherals such as UART, ADC, Low-Energy Timer or GPIO.
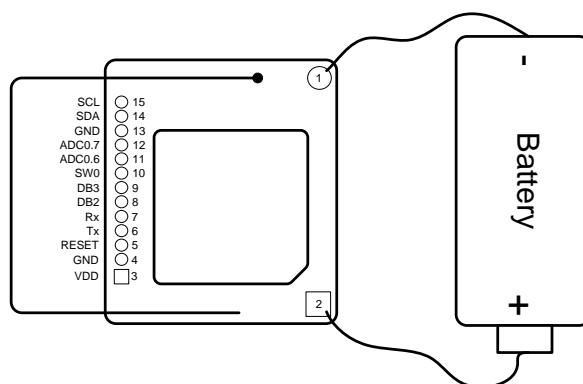

Figure 5. Typical Application

4 Module Interface

4.1 Low-Power UART (Universal Asynchronous Receiver/Transmitter)

The TD1205P communicates with the host MCU over a standard asynchronous serial interface consisting of only 2 pins: TX and RX. The TX pin is used to send data from the TD1205P module to the host MCU, and the RX pin is used to receive data into the TD1205P module coming from the host MCU.

This interface allows two-way UART communication to be performed in low energy modes, using only a few µA during active communication and only 150 nA when waiting for incoming data.

This serial interface is designed to operate using the following serial protocol parameters:

■ LVTTL electrical level

■ 9600 bps

■ 8 data bits

■ 1 stop bit

■ No parity

■ No hardware/software flow control

This interface operates using LVTTL signal levels to satisfy the common interface to a low power host MCU. If an EIA RS232-compliant interface voltage level is required, an RS232 level translator circuit must be used. It is also possible to use a common USB/UART interface chip to connect to an USB bus.

Over this serial interface, the TD1205P device provides a standard Hayes "AT" command set used to control the module using ASCII readable commands and get answers, as well as to send or receive data.

The list of available commands with their corresponding arguments and return values, a description of their operation and some examples are detailed into the "*TDnext RF Modules Reference Manual*".

4.2 I²C bus

As a convenience, the TD1205P module is equipped with a popular I²C serial bus controller that enables communication with a number of external devices using only two I/O pins: SCL and SDA. The SCL pin is used to interface with the I²C clock signal, and the SDA pin to the I²C data signal, respectively. When not used for I2C bus, these 2 pins can be configured to perform other functions using "AT" configuration commands, please refer to the "*TDnext RF Modules Reference Manual*" for details.

The TD1205P module is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode (Sm), fast-mode (Fm) and fast-mode plus (Fm+) speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. Both 7-bit and 10-bit addresses are supported, along with extensive error handling capabilities (clock low/high timeouts, arbitration lost, bus error detection).

The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TDnext RF Modules Reference Manual*".

4.3 Timer/Counter

The TD1205P provides an interface to an integrated timer/counter using the ADC0.6, ADC0.7, SDA or SCL pins. These pins can be configured as either a capture input or a compare / PWM output to the 16-bit internal timer/counter. When not used for timer/counter operation, these pin can be configured to perform other functions using "AT" configuration commands, please refer to the "*TDnext RF Modules Reference Manual*" for details.

The timer consists in a counter that can be configured to up-count, down-count, up/down-count (continuous or one-shot).

The timer also contains 2 output channels, that can be configured as either an output compare or single/double slope PWM (Pulse-Width Modulation) outputs routed to the ADC0.6, ADC0.7, SDA or SCL pins.

The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TDnext RF Modules Reference Manual*".

4.4 ADC (Analog to Digital Converter)

The TD1205P provides an interface to an integrated low-power SAR (Successive Approximation Register) ADC, capable of a resolution of up to 12 bits at up to 1 Msps or 6 bits at up to 1.86 Msps. The ADC0 pin provides the external interface to the ADC. When not used for ADC operation, this pin can be configured to perform other functions using "AT" configuration commands, please refer to the "*TDnext RF Modules Reference Manual*" for details.

Along with the ADC0 analog input channel, the ADC also provides an internal temperature, VDD, and GND input channel that may be used to get a digital representation of analog temperature or voltage values. It is also possible to loopback the analog output of the integrated DAC (see section 4.5, "DAC (Digital to Analog Converter)").

The internal ADC provides an optional input filter consisting of an internal low-pass RC filter or simple internal decoupling capacitor. The resistance and capacitance values are given in the electrical characteristics for the device, named $R_{ADCFILT}$ and $C_{ADCFILT}$ respectively.

The reference voltage used by the ADC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, V_{DD}, a 5 V internal differential bandgap or unbuffered $2V_{DD}$.

Additionally, to achieve higher accuracy, hardware oversampling can be enabled. With oversampling, each selected input is sampled a number of times, and the results are filtered by a first order accumulate and dump filter to form the end result. Using 16x oversampling minimum, it is thus possible to achieve result resolution of upt to 16 bits.

The operation of this interface is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TDnext RF Modules Reference Manual*".

4.5 DAC (Digital to Analog Converter)

The TD1205P provides an interface to an integrated DAC that can convert a digital value to a fully rail-to-rail analog output voltage with 12-bit resolution at up to 500 ksps. The DAC may be used for a number of different applications such as sensor interfaces or sound output. The analog DAC output is routed to the SWO pin. When not used for ADC operation, this pin can be configured to perform other functions using "AT" configuration commands, please refer to the "*TDnext RF Modules Reference Manual*" for details.

The reference voltage used by the DAC can be selected from several sources, including a 1.25 V internal bandgap, a 2.5 V internal bandgap, or V_{DD}.

The internal DAC provides support for offset and gain calibration, and contains an automatic sine generation mode as well as a loopback output to the ADC (see section 4.4, "ADC (Analog to Digital Converter)").

4.6 GPIO (General Purpose Input/Output)

All the TX, RX, DB2, DB3, SWO, ADC0.6, ADC0.7, SDA and SCL pins can be configured individually as tristate (default reset state), push-pull, open-drain, with/without pull-up or pull-down resistor, and with a programmable drive strength (0.5 mA/2 mA/6 mA/20 mA).

When configured as inputs, these pins feature an optional glitch suppression filter and full (rising, falling or both edges) interrupt with wake-up from low-power mode capabilities. Of course, the pin configuration is retained even when using these low-power modes.

The operation of the GPIOs is controlled by the mean of Hayes "AT" commands sent over the UART interface. To obtain a list of the available commands with their corresponding arguments and return values, a description of their operation and some examples, please refer to the "*TDnext RF Modules Reference Manual*".

4.7 RST (Reset)

The TD1205P module features an active-low RST pin. This pin is held high by an internal pull-up resistor, so when not used, this pin can be left floating.

4.8 Debug

The TD1205P module devices include hardware debug support through a 3-pin serial-wire debug interface. The 3 pins DB2, DB3 and SDO are used for this purpose. The DB2 pin is the ARM Cortex-M3's SWDIO Serial Wire data Input/Output. This pin is enabled after a reset and has a built in pull-up. The DB3 pin is the ARM Cortex-M3's SWCLK Serial Wire Clock input. This pin is enabled after reset and has a built-in pull down. Additionally, the SWO pin can be used as a trace output that is completely independent of the CPU. When not used for debug operation, these 3 pins can

be configured to perform other functions using "AT" configuration commands, please refer to the "*TDnext RF Modules Reference Manual*" for details.

Although the ARM Cortex-M3 supports advanced debugging features, the TD1205P devices only use two port pins for debugging or programming. The systems internal and external state can be examined with debug extensions supporting instruction or data access break- and watch points.

For more information on how to enable the debug pin outputs/inputs the reader is referred to Section 28.3.4.1 (p. 457), the ARM Cortex-M3 Technical Reference Manual and the ARM CoreSight™ Technical Reference Manual.

4.9 VDD & GND

The TD1205P provides a VDD and GND pin in addition to battery supply. These pins are only provided for programming convenience and can be left open when a battery supply is provided.

4.10 LEDs

A green and a red led are available on the TD1205P.

4.11 Battery Supply

As a stand-alone solution, the TD1205P only required a 2.3V to 3.6V battery supply to work.

4.12 Integrated antennas and packaging

The TD1205P includes integrated antennas for both RF transmission and GPS reception. These antennas are both already matched to obtain best possible performance. Therefore care must be taken when adding a package around the module for the antennas could become improperly matched. Please make sure the distance between packaging and both RF and GPS antenna is greater than 1cm to obtain best possible performance.

5   Bootloader
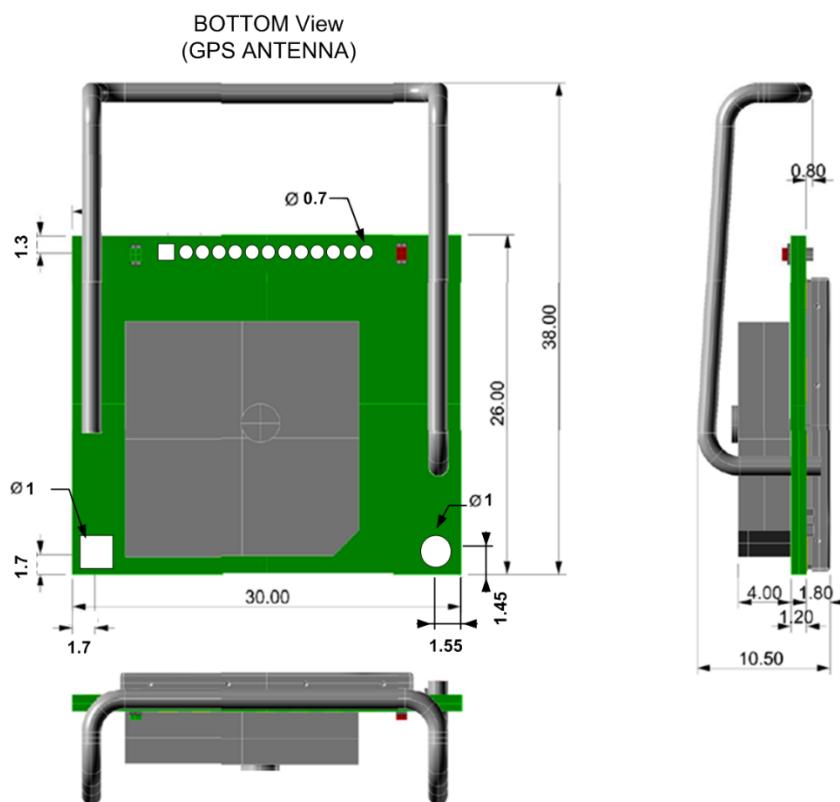
The TD1205P module contains an integrated bootloader which allows reflashing the module firmware either over the RX/TX UART connection, or over the air using the built-in RF transceiver.

The bootloader is automatically activated upon module reset. Once activated, the bootloader will monitor the UART/RF activity for a 200 ms period, and detect an incoming update condition.
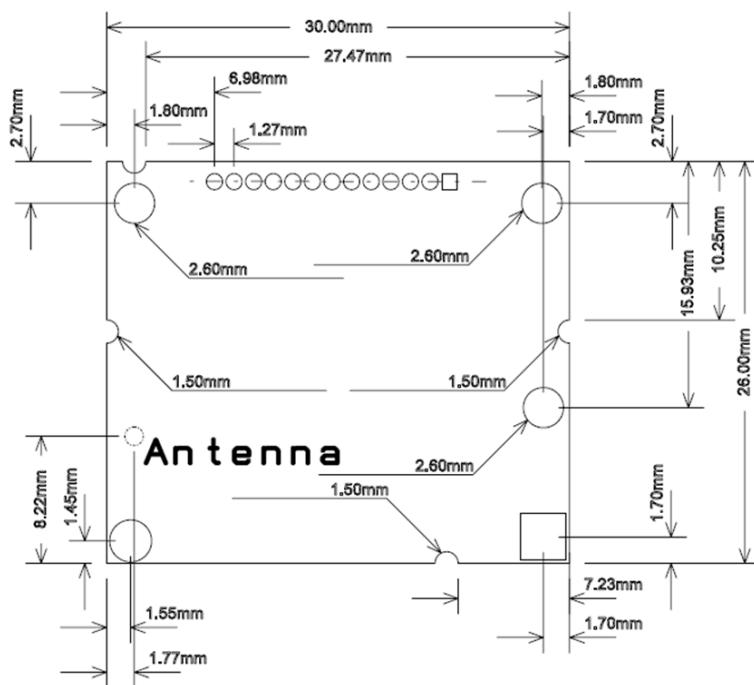
If the update condition is met, the TD1205P will automatically proceed to flash the new firmware with safe retry mechanisms, or falls back to normal operation.

6   Package Outline

Figure 6 and Figure 7 illustrates the package details and PCB size for the TD1205P.

Figure 6. TD1205P Package

Figure 7. TD1205P PCB size

Notes:

1. *All dimensions are shown in millimeters (mm) unless otherwise noted.*
2. *All tolerances are 0.05mm for dimensions less than 2mm and 0.1mm for dimensions more than 2mm*

7 Integration recommendations

Figure 8 depicts the rules defined to enclose TD1205P module while maintain performances. It is also recommended to not exceed a casing thickness of 2.5mm.

The following recommendations are:
- Radiated performances:
  - o 7mm minimum distance between antenna and casing
  - o 7mm minimum distance between PCB and Battery
- Hall effect sensor requirement:
  - o 5mm maximum distance between metal protection of TD1205P and casing
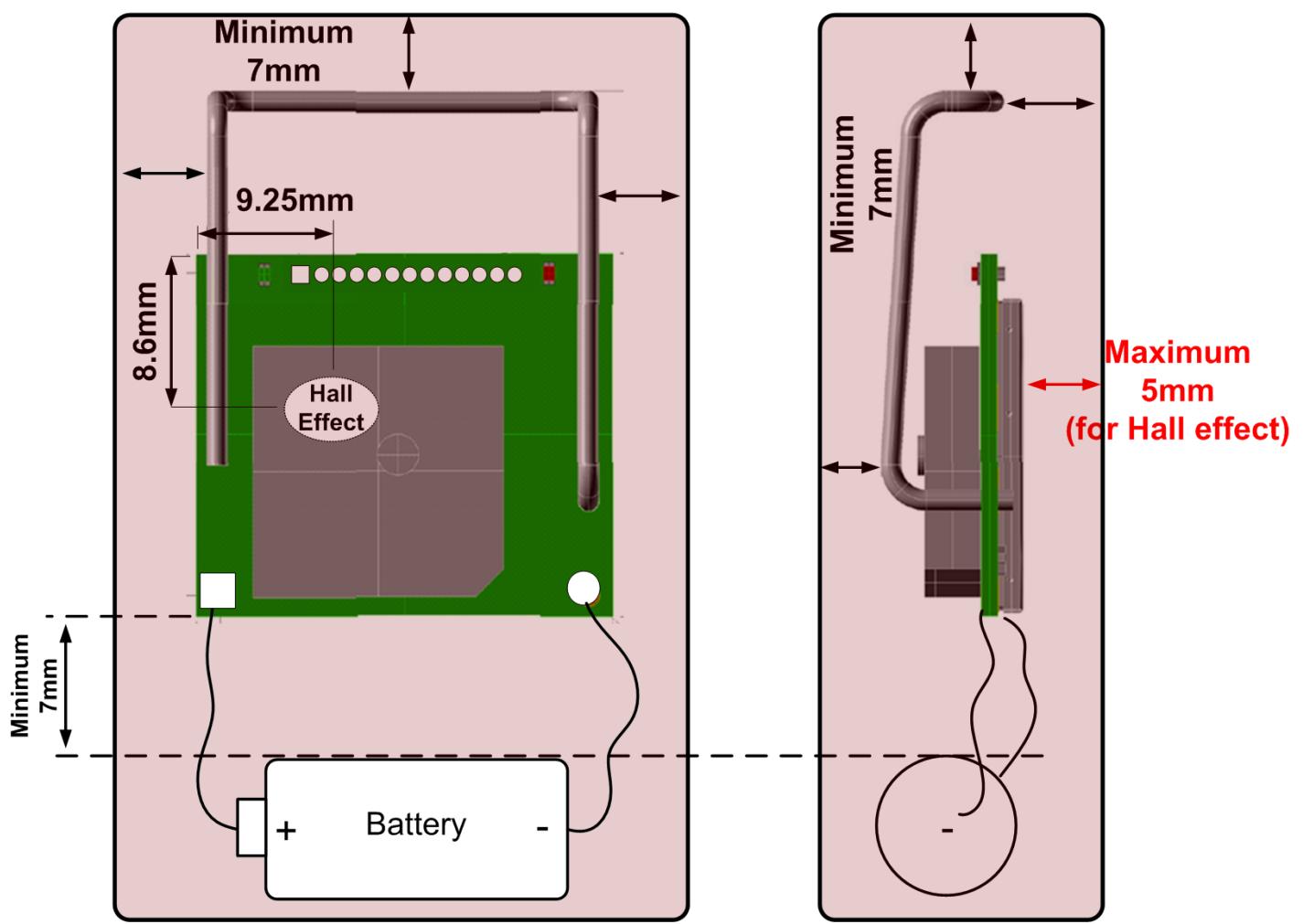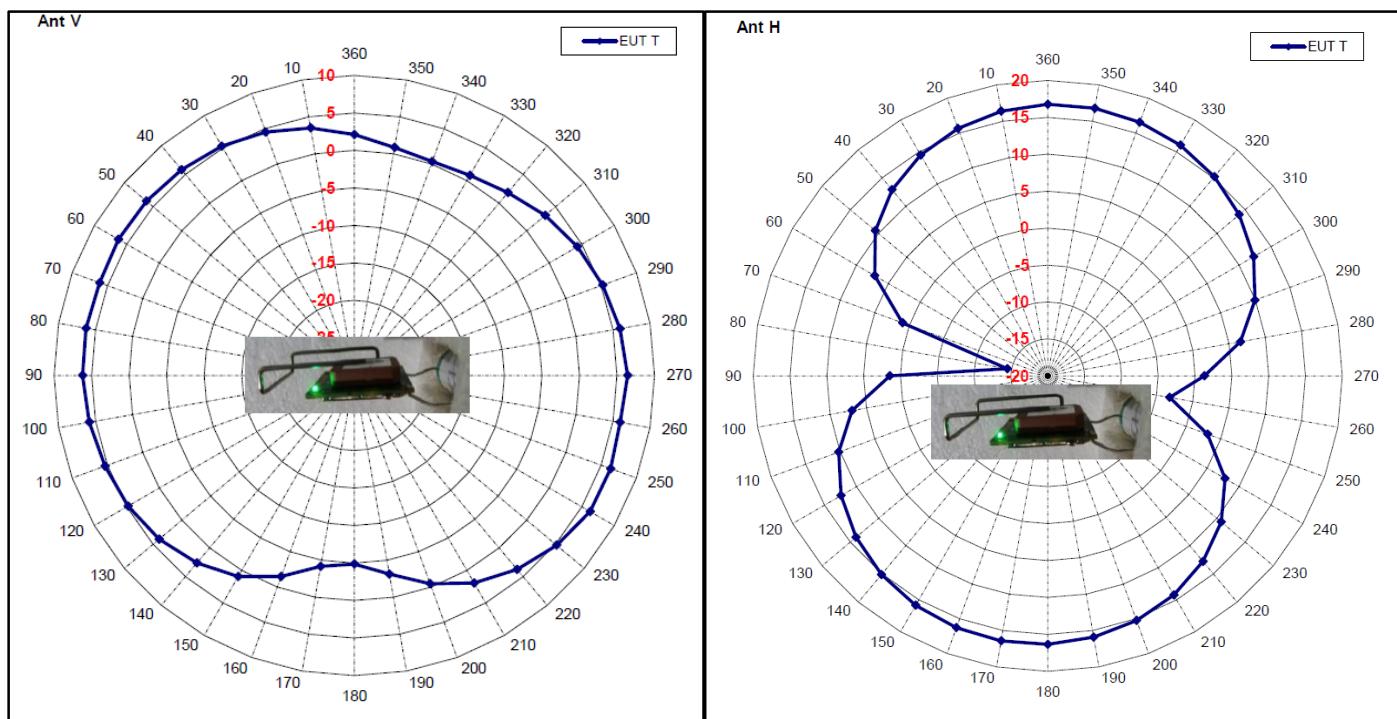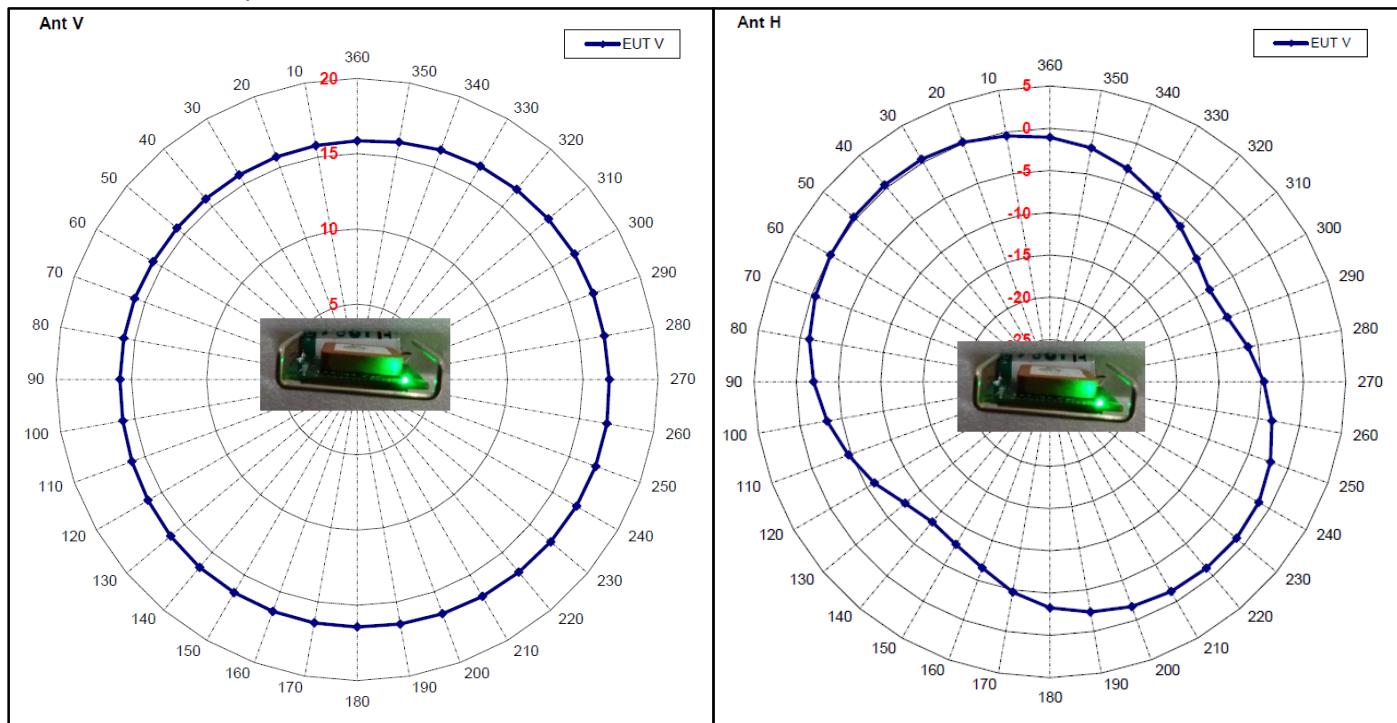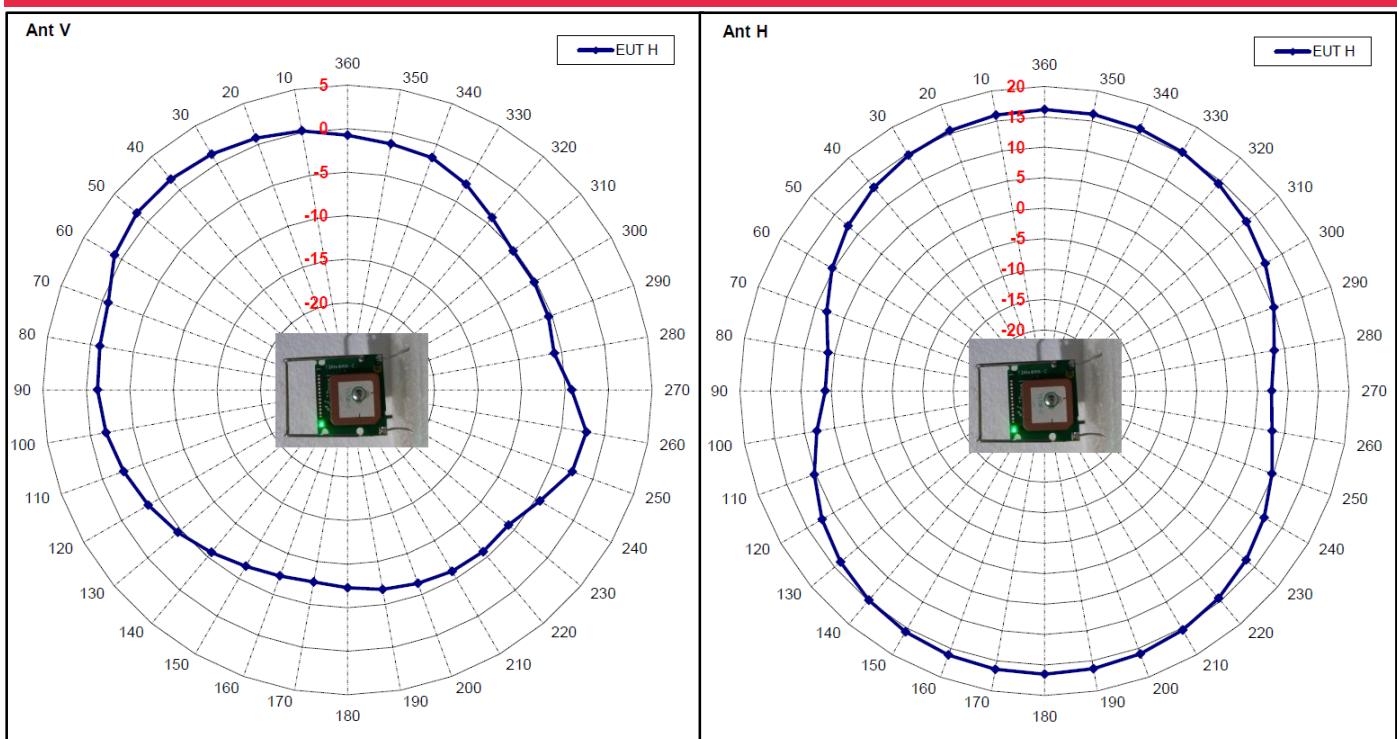
Figure 8. TD1205P PCB size

8   Radiation Pattern

PA set to maximum power.

9 Production Information

9.1 Ordering Information
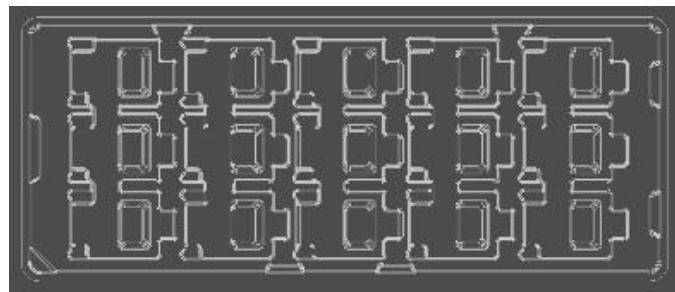
Part number	Ordering Code	Description	Operating Temperature
TD1205P	PROD0767C	ISM SIGFOX™ gateway with GPS	-30° to +75°C

9.2 Related Products
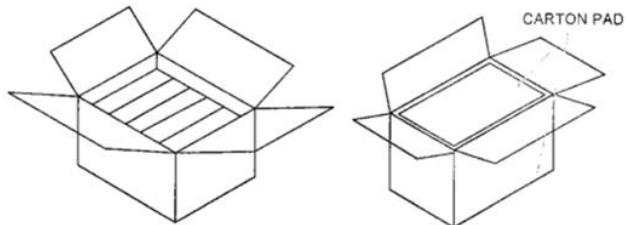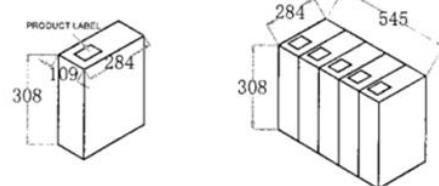
TD next Interface Board	Ordering Code	Description
TDnext: TDNx004	PROD0849	TD1205P PCB adapter

9.3 Shipping packaging
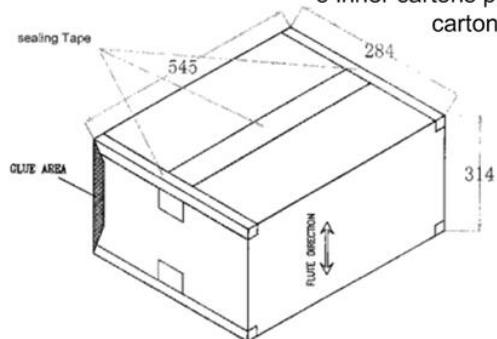
15 pieces per sealed ESD bag
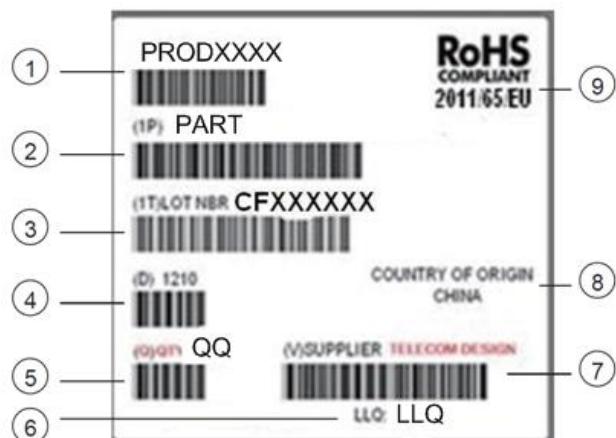
8 sealed ESD bag per inner carton

5 inner cartons per shipping carton

9.4   Product Label

Item	Function
1	TD Model
2	Product Description
3	TD PO
4	Manufactured Year and Week
5 / 6	Packed Quantity
7	Customer Name
8	Country Of Origin
9	RoHS Compliant

DOCUMENT CHANGE LIST

Revision 1.0

■ TD1205P datasheet

Revision 1.1

■ Figure 2 and Figure 5 revised

Revision 1.2

■ Related products added

Revision 1.3

■ Figure 4 updated

■ Figure 6 updated

■ Figure 8 updated

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