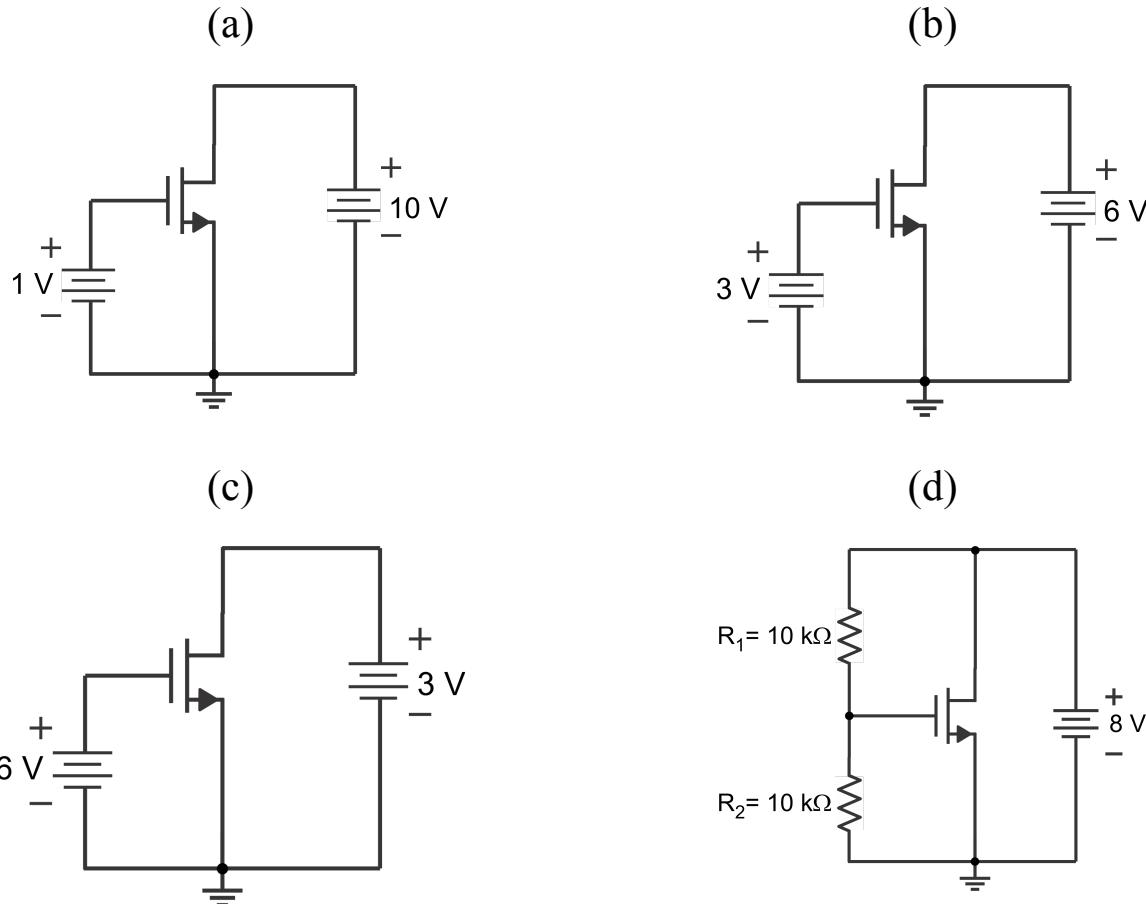
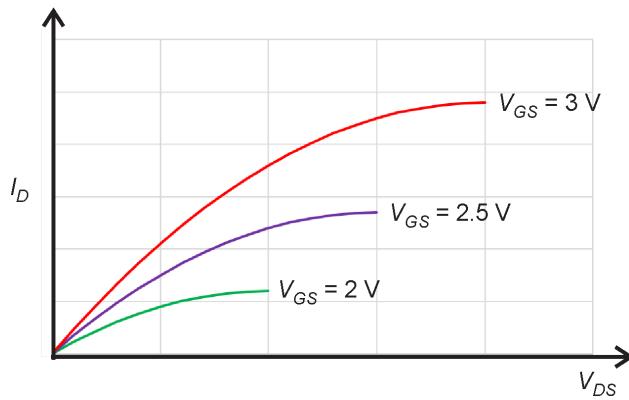


- 1) **MOSFET Circuits at DC:** For the following n-channel MOSFET circuits, the FET parameters are  $V_{TN} = 2.6V$  and  $k_n = 0.12 A/V^2$ .

For each circuit, find the mode of operation (cutoff, non-saturated or saturated). List the values for  $V_{GS}$ ,  $V_{DS}$ ,  $I_D$ .



- 2) **Non-Saturated Mode Plot:** Using the equation for the N-channel MOSFET operating in non-saturated mode, plot the curves for  $I_D$  (y-axis) versus  $V_{DS}$  (x-axis) when  $V_{GS} = 2V$ ,  $2.5V$  and  $3V$ . Use a value for  $k_n = 0.12 A/V^2$  and  $V_{TN} = 1V$ . You may use any software app for the plot, such as Excel, Desmos, Matlab, etc. For each value in  $V_{GS}$ , plot  $V_{DS}$  over the range from  $V_{DS} = 0 V$  to  $V_{DS} = (V_{GS}-V_{TN})$ . Your plot should look similar to the following.

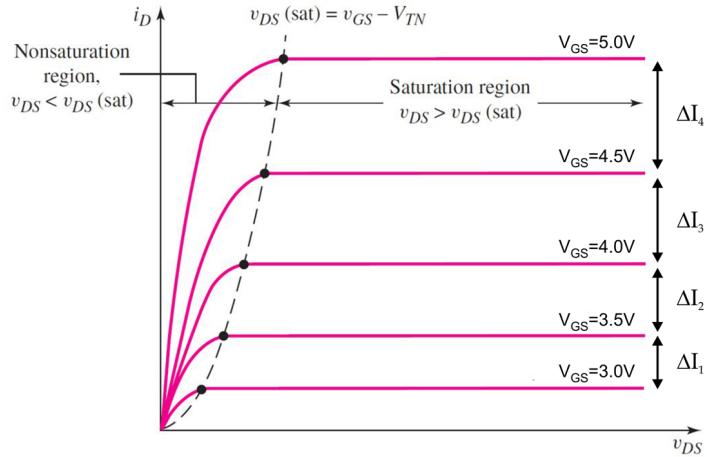


**Submit your  $I_D$  versus  $V_{DS}$  plot with values on each axis clearly visible.**

- 3) **PSPICE SIMULATION:** Using a PSPICE simulator, such as CircuitLab or OrCAD, create a circuit that can plot the  $I_D$ - $V_{DS}$  characteristics of an NMOS enhancement-mode transistor.

The  $I_D$ - $V_{DS}$  characteristic requires that the drain voltage source and gate voltage source to be swept over a range of values. Set the “Primary Sweep” as the Drain Voltage and the “Secondary Sweep” as the Gate Voltage. Sweep the Drain voltage from 0 to 10V in steps of 0.1V. Sweep the Gate voltage from 0 to 5 V in steps of 0.5 V.

Your simulation plot should be similar to the following set of curves (purple lines). Appendix A and B provide additional information for configuring your PSpice simulation using CircuitLab and OrCAD respectively.



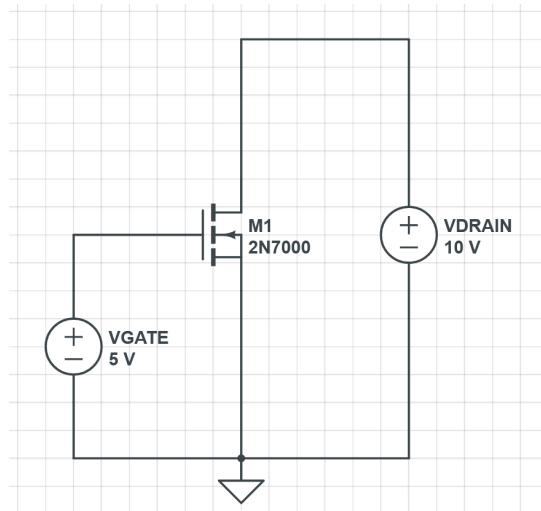
**Submit a copy of your schematic and the associated PSpice I-V plot. When examining the portion of the curves in the saturated region, are the steps between  $I_{DS}$  curves, namely  $\Delta I_1$ ,  $\Delta I_2$ ,**

**$\Delta I_3$ , and  $\Delta I_4$ , equal in value when the gate voltage is increased by uniform steps of 0.5V? What is the reason? If possible, provide an equation showing this effect.**

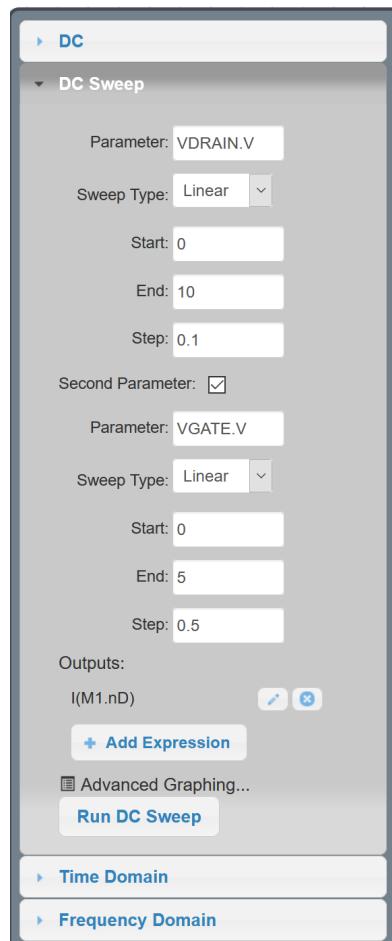
---

#### APPENDIX A: CircuitLab Simulation Help

Find the N-channel MOSFET and two DC voltage sources and connect the circuit below. Note that the MOSFET's Source terminal and the "body" terminal are connected to ground. You will also need to include a "ground" reference in order for the PSPICE simulation to properly run. Double-click the MOSFET to open the menu and select the model 2N7000. Below is a typical schematic for testing the transistor performance.

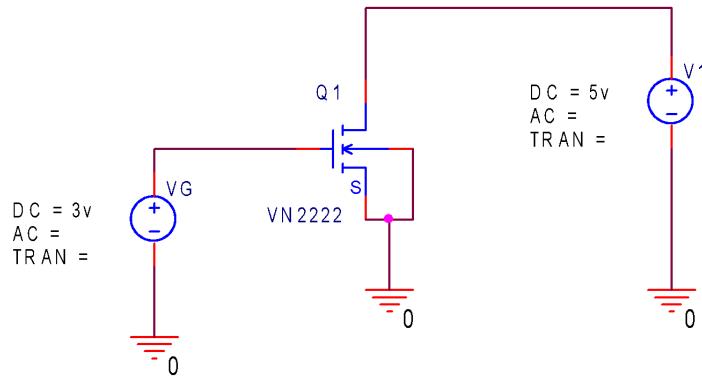


In order to simulate the I-V characteristics as a function of gate voltage, you will need to perform a "DC Sweep" in CircuitLab. Below is the DC Sweep menu with primary and secondary sweep parameters.

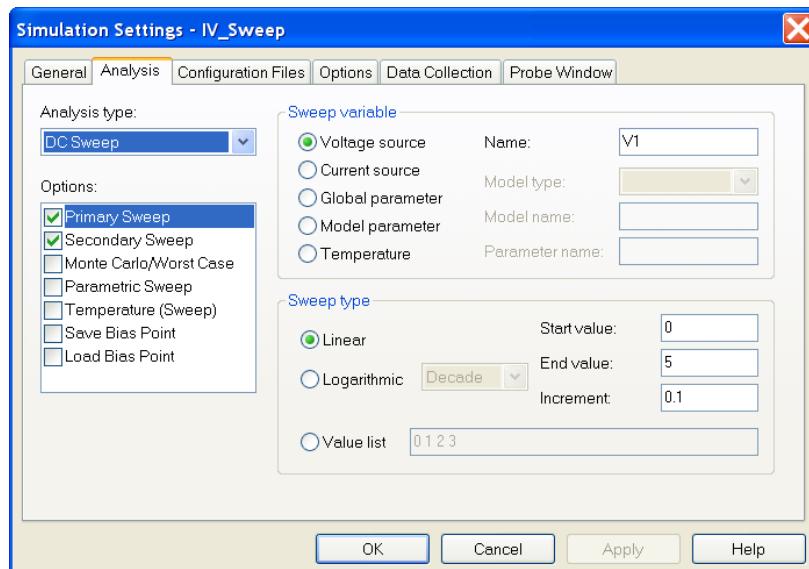


### APPENDIX C: OrCAD Simulation Help

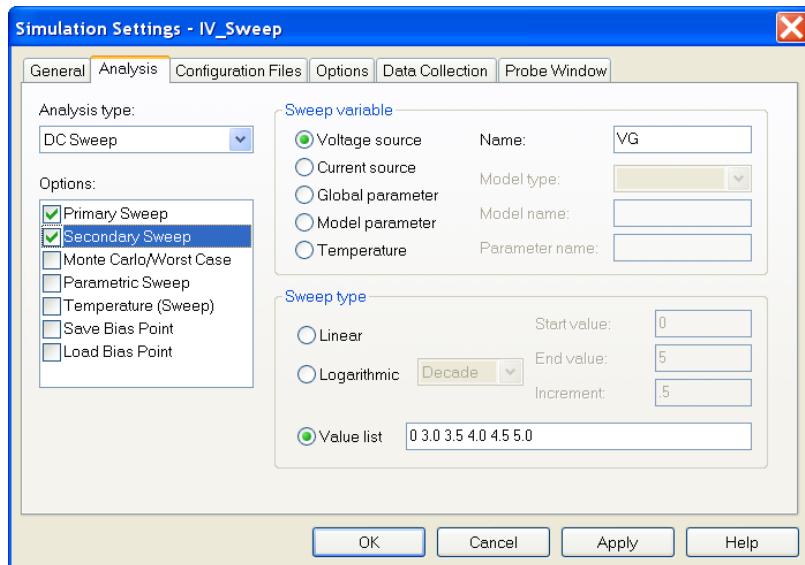
When using OrCAD, select the VN2222 NMOS. The Gate and Drain voltage inputs will be a voltage source such as the “VSRC” found in the SOURCE library of OrCAD. The following schematic shows an example. Note the Source terminal and the “body” terminal are connected to ground.



The I-V characteristic requires that the voltage sources sweep over a range of values. When using the OrCAD PSpice simulator, set the Simulation Profile to the analysis type “DC Sweep”. Set the “Primary Sweep” to a Voltage Source with the name of the drain voltage source,  $V_1$  in the example shown above. The drain voltage will use a linear sweep type over the range of 0 to 10 V in 0.1V increment.



Set a “Secondary Sweep” to a voltage source with the name of the gate source,  $V_G$  in this case. The gate voltage will use the “Value List” sweep type. The listed gate voltages are 0, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0V. You may also use the “Linear” sweep type over the range from 0 to 5 volts in 0.5 V increments.



## Solutions

①

- ⓐ  $V_g = 1V$  Here  $V_{GS} = 1V$  and  $V_{TN} = 2.6V$   
 $V_s = 0V$  As  $V_{GS} < V_{TN}$  the mosfet is in cutoff  
 $V_D = 10V$   $\therefore$  current  $I_D = 0$

⑤

$V_g = 3V$   $V_{GS} = 3V$  and  $V_{GS} > V_{TN}$

$V_s = 0V$   $\therefore$  Mosfet is not in cutoff  
 $V_D = 6V$

$V_{DS} = 6 - 0 = 6V$

$V_{GS} - V_{TN} = 3 - 0 - 2.6V = 0.4V$

Hence  $V_{DS} \geq V_{GS} - V_{TN}$

$\therefore$  Mosfet is in saturation mode

$$I_D = \frac{0.12}{2(0.4)^2} = 0.0096A$$

- ⑥  $V_g = 6V$   $V_{GS} - V_{TN} = 6 - 2.6V = 3.4V$   
 $V_D = 3V$   $\therefore V_{GS} - V_{TN} > V_{DS}$   
 $V_s = 0V$   $\therefore$  Mosfet is in non saturated mode

$$I_D = \frac{0.12}{2(2(3.4) \times 3^{-2})} = 0.684A$$

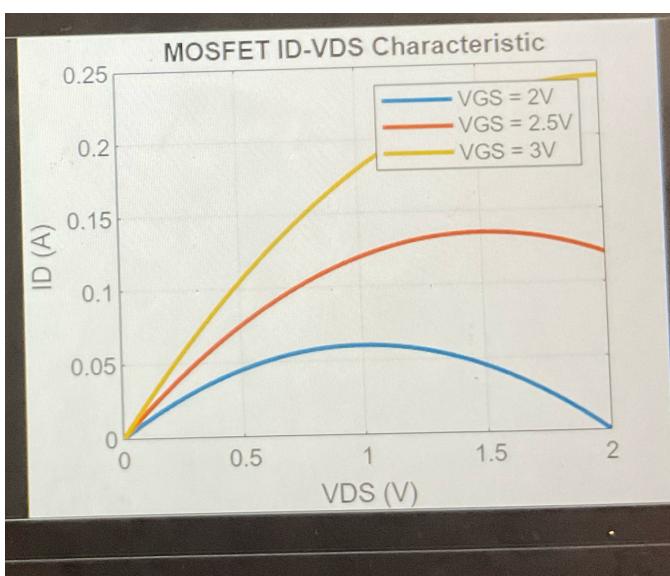
⑦

$V_g = 4V$   $\therefore V_{GS} = 4V$  and is not greater than  $V_{GS} - V_{TN}$

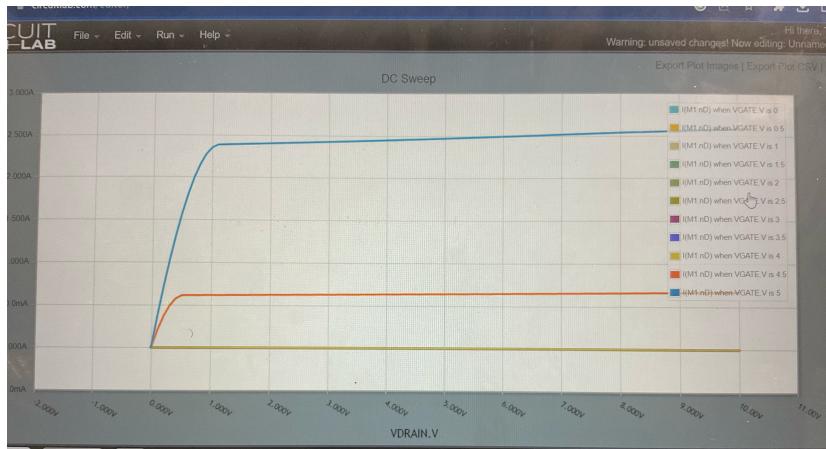
$V_D = 8V$   $\therefore$  Mosfet is in saturated mode

$V_s = 0V$   $I_D = \frac{0.12}{2(4 - 2.6)^2} = 0.1176A$

2



3



Answer to the question in bold:

No, the increase is not in uniform steps of  $\Delta V$ . Because as you increase the gate voltage  $V_{GS}$ , you are also increasing by  $(V_{GS} - V_{Tn})^2$ .

$$\text{The equation is : } I_D = \frac{1}{2} k_n \left( \frac{W}{L} \right) (V_{GS} - V_T)^2$$