

# Extending Compiler Support for the BrainScaleS Plasticity Processor

Bachelor's Thesis Presentation

Arthur Heimbrecht

March 10, 2017

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Welcome everybody to this talk about my Bachelor thesis. As this is a quite technical talk, feel free to ask questions at any time. The topic of my thesis was Extending Compiler Support for the BrainScaleS Plasticity Processor.

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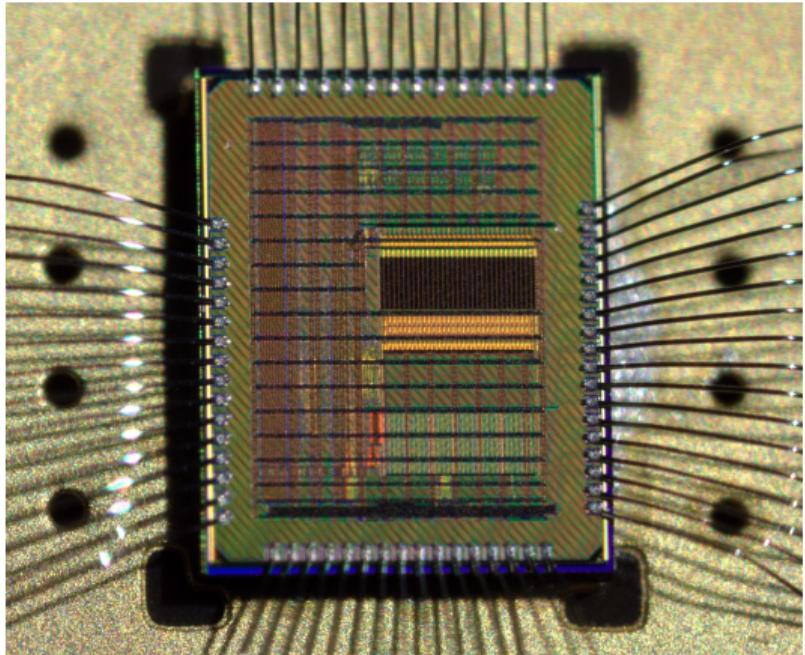
PPU Architecture

GCC Structure

Extending GCC for the PPU

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**Figure 1:** Photograph of HICANN-DLS chip,  
Friedmann et al.

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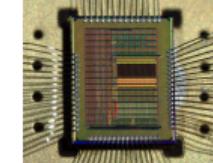
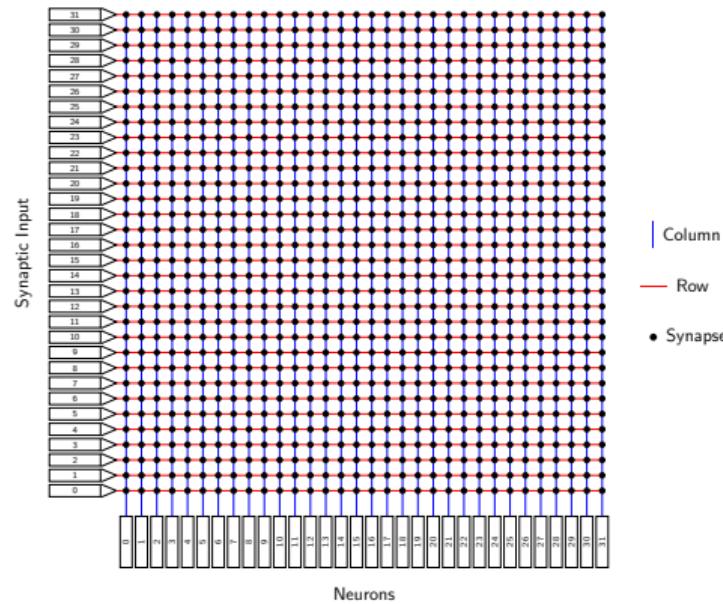


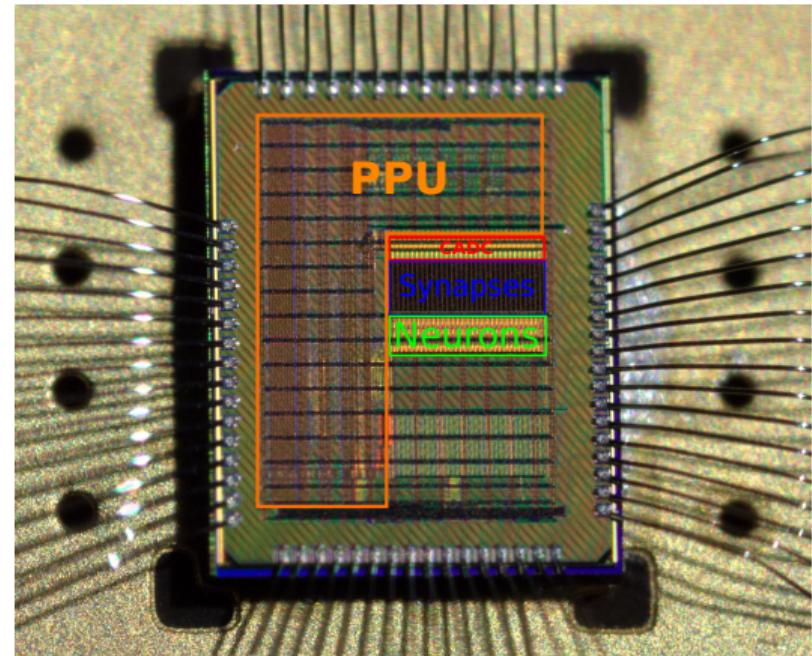
Figure 1: Photograph of HICANN-DLS chip.  
Freudiger et al.

as the title hints there are two main components to this talk, which are the plasticity processing unit (PPU) and Compilers. I will briefly talk about both of these and their applications. Afterwards I will explain, what I did during my thesis, which is of course followed by a short presentation of the results. But first I should explain, what the PPU is.

# HICANN-DLS



**Figure 2:** Photograph of HICANN-DLS chip, modified from Friedmann et al.



**Figure 3:** Photograph of HICANN-DLS chip, modified from Friedmann et al.

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## Processor

### PPU Architecture

#### HICANN-DLS

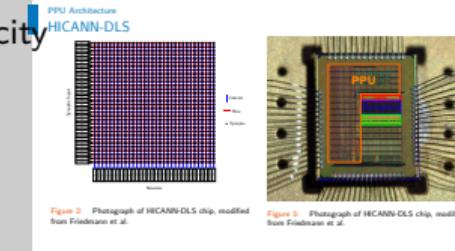


Figure 2: Photograph of HICANN-DLS chip, modified from Friedman et al.

Figure 3: Photograph of HICANN-DLS chip, modified from Friedman et al.

I am assuming that everybody here probably has heard about the HICANN-DLS. In short it is a chip that emulates neural networks through neurons and synapses that are implemented directly on the chip. What is special about the DLS, is the addition of a PPU to the HICANN. It is capable of performing simple computation and allows for on-line plasticity directly on the chip.

As you can see to the right I have added a picture of the HICANN chip and marked the physical compartments. The PPU actually takes up a large space on the chip but before I am going to talk about the PPU, I will talk about the other parts briefly. First we have the neurons. There are 32 neurons on the HICANN-DLS and each neuron is a circuit that receives some input signal which can cause the neurons to spike. These signals come from the so called synapse array. It connects 32 pre-synaptic inputs to all 32 neurons. This gives a total of 1024 synapses on each HICANN.

Each synapse is realized through a circuit that takes the input signal and modifies it with a synaptic weight, that is saved in each synapse. There are also other properties to each synapse, but for this presentation it is enough to

# Plasticity Processing Unit

The design is clean

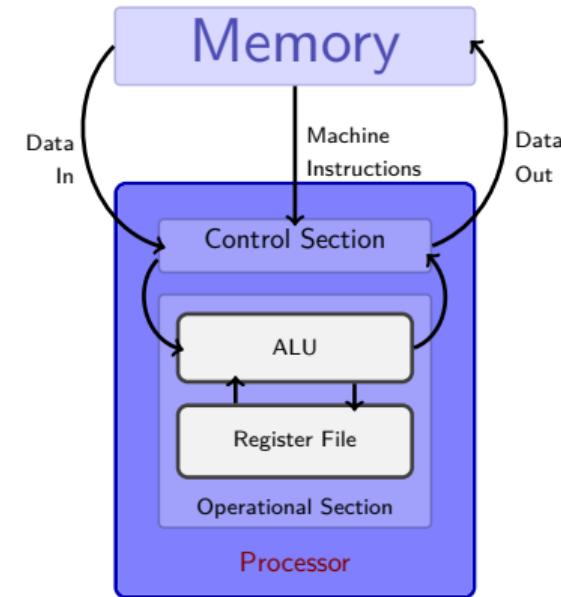


Figure 4: Schematic of Processor in von-Neumann Architecture

# PPU Architecture

The design is clean  
The rules are simple  
The code is extensible

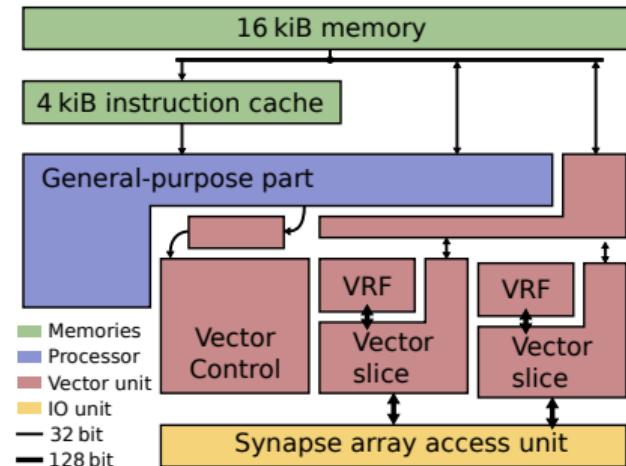


Figure 5: Structure of nux Architecture

# GCC Structure

The design is clean  
The rules are simple  
The code is extensible

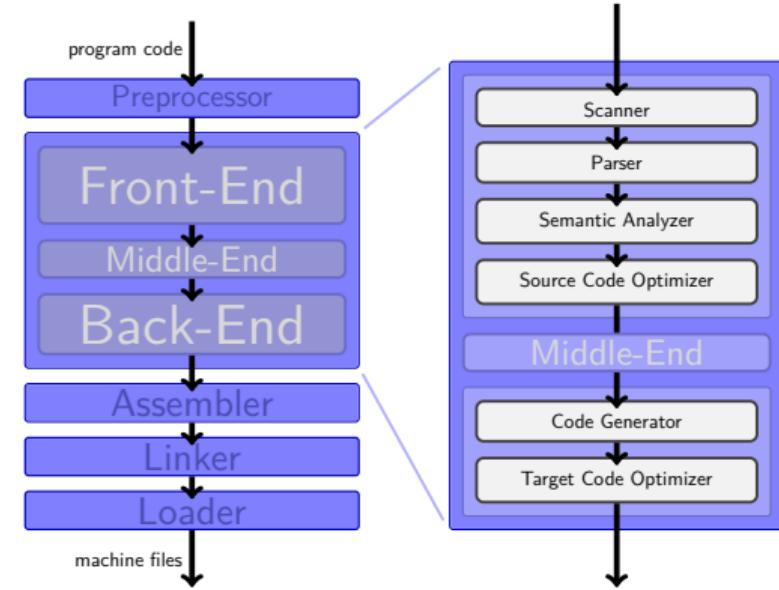


Figure 6: Structure of Compiling Process and Compiler

# Extending GCC for the PPU

# Results

## References

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- Simon Friedmann et al. "Demonstrating Hybrid Learning in a Flexible Neuromorphic Hardware System". In: (2016).