Extending Compiler Support for the BrainScaleS Plasticity Processor

Bachelor's Thesis Presentation

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Contents

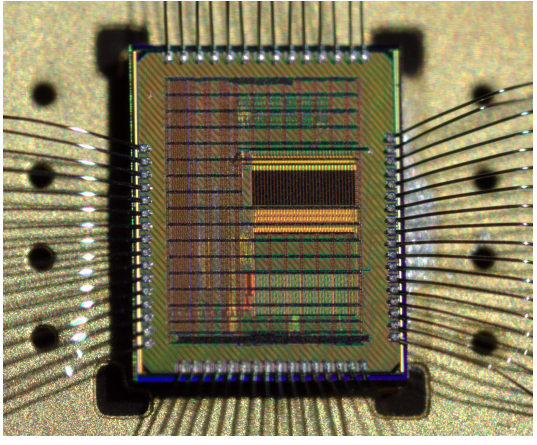

Figure: Photograph of HICANN-DLS v1 chip, Friedmann et al.

HICANN-DLS

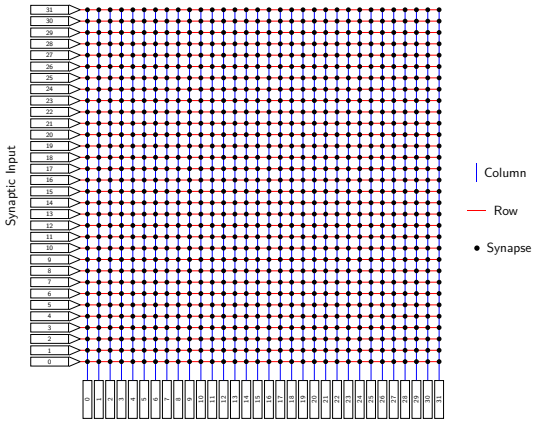

Figure: Schematic representation of the synapse array on HICANN-DLS v2 and newer

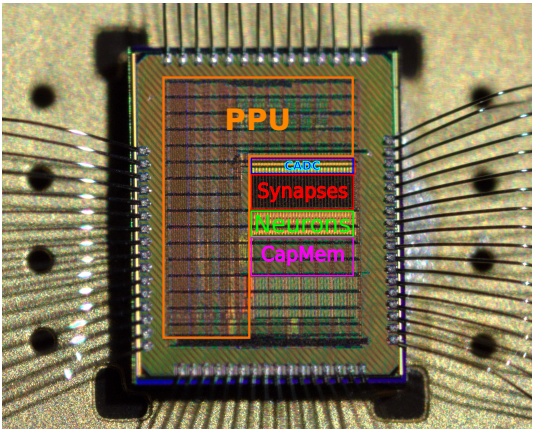

Figure: Photograph of the HICANN-DLS v1 chip, modified from Friedmann et al.

Processors

- “common” von-Neumann architecture
- machine instructions in memory
- data in memory

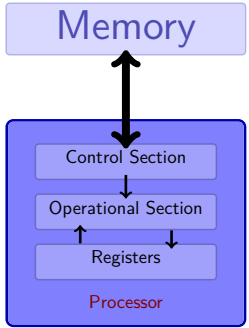

Figure: Schematic of general purpose processor with von-Neumann architecture

Processors

- "common" von-Neumann architecture
- machine instructions in memory
- data in memory
- latency(register) $\approx$ 1 cycle
- latency(memory) $\approx$ 100-1000 cycles

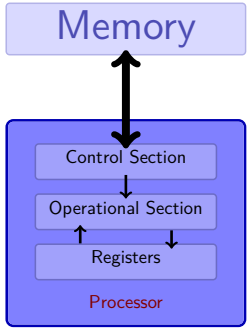

Figure: Schematic of general purpose processor with von-Neumann architecture

Plasticity Processing Unit

- based on PowerISA
- extension with vector registers
  → parallelization of operations
  → better performance
- weight updates
- access to synaptic array

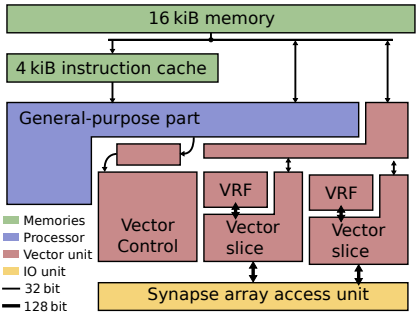

Figure: Structure of the PPU's architecture

Compiling Stages

- code $\xrightarrow{\text{compile}}$ executable
- different compiling stages (e.g. Preprocessor)
- front-end $\leftrightarrow$ programming language
- middle-end $\rightarrow$ optimization
- back-end $\leftrightarrow$ processor architecture

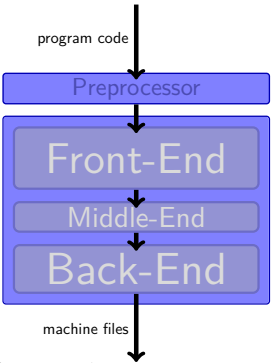

Figure: Structure of compiling process and compiler

GCC and the PPU

- no “official” support for PPU
- currently using macros

Example for macro usage

```
1  #define VR_TMP      0
2  #define VR_A        1
3  ...
4  fxv_addbm(VR_A, VR_A, VR_TMP);
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Preprocessed example

```
1  ...
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- existing AltiVec extension

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Example for AltiVec code

```
1  vector char a, tmp;
2  ...
3  a = vec_add(a, tmp);
```

GCC and the PPU

- no “official” support for PPU
- currently using macros
- existing AltiVec extension
- intrinsics → **use this**

Example for macro usage

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1  #define VR_TMP      0
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Example for AltiVec code

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1  vector char a, tmp;
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Main Work of this Thesis

- add GCC support for PPU

Previous PPU code

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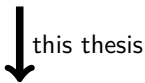

New PPU code

```
1  vector char a, tmp;
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- GCC back-ends not documented

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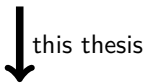

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  - internal functions
  - internal macros

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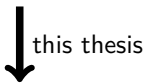

New PPU code

```
1  vector char a, tmp;
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Main Work of this Thesis

- add GCC support for PPU
- GCC back-ends not documented
- AltiVec inspiration for
  - internal functions
  - internal macros
- other components:
  - vector registers
  - vector variables
  - new intrinsics
  - ...

Previous PPU code

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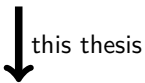

New PPU code

```
1  vector char a, tmp;
2  ...
3  a = fxv_add(a, tmp);
```

New Features

- `-mcpu=nux` target flag & `s2pp.h` header

Compile command

```
1  powerpc-linux-eabi-gcc -mcpu=nux
```

Example file

```
1  #include<s2pp.h>
2
3  start(){
4    return;
5  }
```

New Features

- `-mcpu=nux` target flag & `s2pp.h` header
- `vector` attribute for variables

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- `vector` attribute for variables
- simple vector initialization

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1  #include<s2pp.h>
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3  start(){
4    vector char vec =
5        {1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1};
6    return;
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- `-mcpu=nux` target flag & `s2pp.h` header
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New Features

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- `vector` attribute for variables
- simple vector initialization
- PPU vector intrinsics
- inline assembly support

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6    vec = fxv_add(vec, vec);
7    asm ("fxvaddbm %0, %0, %0"
8        :"+kv" (vec)::);
9    return;
10 }
```

New Features

- `-mcpu=nux` target flag & `s2pp.h` header
- `vector` attribute for variables
- simple vector initialization
- PPU vector intrinsics
- inline assembly support
- optimization

Compile command

```
1  powerpc-linux-eabi-gcc -mcpu=nux -O1
```

Example file

```
1  #include<s2pp.h>
2
3  start(){
4    vector char vec =
5        {1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1};
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7    asm ("fxvaddbm %0, %0, %0"
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```

Advantages

Comparison of unoptimized code (left) and `-O1` optimized code (right)

```
start:
stwu %r1,-64(%r1)
stw %r31,60(%r1)
mr %r31,%r1
li %r9,1
fxvsplatb %f12,%r9
li %r9,16
fxvstax %f12,%r31,%r9
li %r9,16
fxvlax %f12,%r31,%r9
li %r9,16
fxvlax %f11,%r31,%r9
fxvaddbfs %f12,%f12,%f11
li %r9,16
fxvstax %f12,%r31,%r9
#APP
 # 277 "nux/main.c" 1
fxvaddbm %f12, %f12, %f12
 # 0 "" 2
#NO_APP
li %r9,16
fxvstax %f12,%r31,%r9
nop
addi %r11,%r31,64
lwz %r31,-4(%r11)
mr %r1,%r11
blr
```

```
start:
stwu %r1,-48(%r1)
li %r9,1
fxvsplatb %f12,%r9
li %r9,16
fxvstax %f12,%r1,%r9
fxvlax %f12,%r1,%r9
fxvlax %f11,%r1,%r9
fxvaddbfs %f12,%f12,%f11
fxvstax %f12,%r1,%r9
#APP
 # 277 "nux/main.c" 1
fxvaddbm %f12, %f12, %f12
 # 0 "" 2
#NO_APP
fxvstax %f12,%r1,%r9
addi %r1,%r1,48
blr
```

Advantages

- easier PPU programs for users
- efficient programs
- workarounds in compiler

Comparison of unoptimized code (left) and `-O1` optimized code (right)

```
1   start:
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```

Outlook

- further testing for compiler bugs
- already existing applications
- extending PPU test coverage
- C-library support for PPU
  → soft-float
- debugging support?

Compiling Directive

```
powerpc-linux-eabi-gcc -mcpu=nux -O1
```

Example File

```
#include<s2pp.h>

start(){
  vector char vec =
      {1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1};
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- **new tools for PPU experiments!**

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- **more experiments!**

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References

- S. Friedmann, J. Schemmel, A. Grübl, A. Hartel, M. Hock, and K. Meier, "Demonstrating hybrid learning in a flexible neuromorphic hardware system", (2016).
- T. Flik, *Mikroprozessortechnik und rechnerstrukturen*, ger, 7., neu bearb. Aufl. (Springer, Berlin ; Heidelberg [u.a.], 2005), XIV, 649 S.
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- S. Friedmann, *Nux manual*, (2016).
- *Gnu compiler collection internals manual*, `https://gcc.gnu.org/onlinedocs/gccint/index.html`, Free Software Foundation Inc. (2017).

Additional Figures

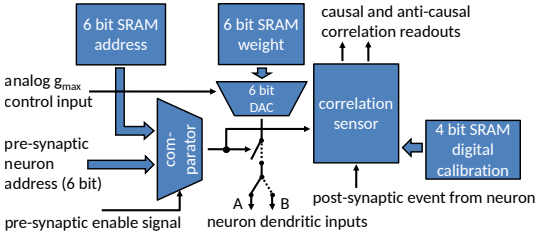

Figure: Block Diagram of the Synapse Circuit (modified from Friedmann et al.).

31	23	15	7	0
mnemonic	operand	operand	operand	
`addi`	`r1` register address	`r2` register address	`5` immediate operand	

Figure: Representation of Assembly Instruction `addi` as a Machine Instruction in Memory. The immediate value `5` is added to register `r2` and the result written in `r1`.

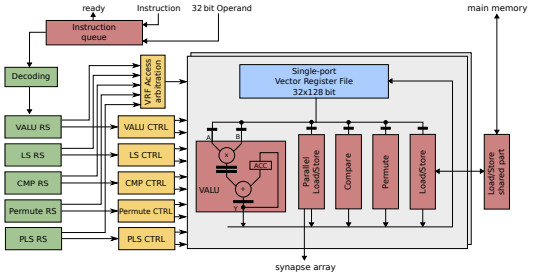

Figure: Detailed Structure of the s2pp Vector Extension (taken from Friedmann et al.)

7	6	5	4	3	2	1	0
		2^5	2^4	2^3	2^2	2^1	2^0

Figure: Comparison of the Representation of Weights in Synapses and the Fractional Representation of Vector Components for Fixed-Point Saturational Arithmetic

Additional Figures

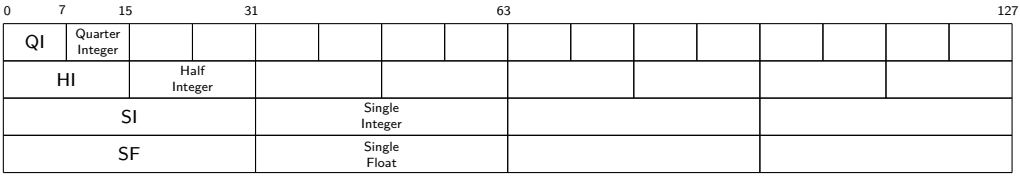

Figure: Vector structures are 128 bits wide and split into common word sizes.

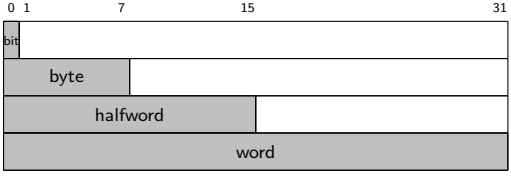

Figure: Illustration of Word Sizes for 32-bit Words