Design and Optimization of Synchronous Counter Using Majority Gate-Based JK Flip-Flop

Chapter · September 2019

DOI: 10.1007/978-981-15-0111-1_9

4 authors, including:

Birinderjit Singh Kalyan
Punjab Technical University
8 PUBLICATIONS **5** CITATIONS
SEE PROFILE

Balwinder singh Lakha
Centre for Development of Advanced Computing
141 PUBLICATIONS **400** CITATIONS
SEE PROFILE

Design and Optimization of Synchronous Counter Using Majority Gate-Based JK Flip-Flop

Mehak Ishrat[1(✉)], Birinderjit Singh Kalyan[2(✉)], Amandeep Sharma[1(✉)], and Balwinder Singh[3(✉)]

[1] Electronics and Communication Engineering, Chandigarh University, Punjab 140413, India
mehak.ishrat37@gmail.com, amandeep.sharma@thapar.edu
[2] Electronics and Electrical Engineering, Chandigarh University, Punjab 140413, India
birinderjit@msn.com
[3] Centre for Development of Advanced Computing, Mohali, India
balwinder@cdac.in

Abstract. Complementary metal oxide semiconductor is an innovation that has changed the domain of hardware. CMOS scaling has achieved maximum limit, indicating adverse impacts not just from physical and mechanical perspective yet additionally from material and practical point of view. This drift move the analysts to search for new encouraging options in contrast to CMOS technology which indicates better execution, thickness and power utilization. To replace the CMOS technology different new technologies are developed in order to solve the different problems faced by CMOS. In this paper, new rising nanotechnology, quantum dot cellular automata is considered. Quantum dot cellular automata contributes in overcoming the difficulties faced by the CMOS technology now a days such as heat dissipation and scaling problems and hence improves the computation in different applications. For that reason, this paper propose the compatible architecture based on majority gate structures. This paper aims to present 2-bit and 3-bit synchronous counter as an application of a well-optimized JK flip-flop which is optimized on account of QCA. The proposed synchronous counter structure can be further extended to 4-bit and more. The advantage of the propound structure in comparison to previous circuits in terms of energy dissipation have been shown derived. QCADesigner E tool is used for the evaluation of the operational exactness of the designed structure.

Keywords: QCA · Quantum dots · Quantum cells · QCA clocking · JK flip flop · Synchronous counter

1 Introduction

Moore's law has been followed by the microelectronics industry from almost last 5 decades because of which the size and speed of electronic devices has shown the remarkable enhancement [1]. According to the Moore's law after every 18 months, on

A. K. Luhach et al. (Eds.): ICAICR 2019, CCIS 1076, pp. 84–95, 2019.
https://doi.org/10.1007/978-981-15-0111-1_9

every square inch of an integrated circuit the total number of transistors will double and it also allows increasing the chip size as well as shrinking the size of the electronic devices while retaining the satisfactory outcomes, hence the overall speed and the power will also double [1]. Current CMOS is scaled very rapidly and continuously and hence is ultimately reaching the fundamental deadline. Further scaling of CMOS technology based devices is also limited by the factors such as high leakage current, high lithography cost, quantum effects, high power dissipation and short channel effects [2]. The shortcomings of the CMOS can be suppress by various emerging technologies [3]. Out of the various nascent technologies, Quantum dot Cellular Automata, Single Electron Transistor and Resonant Tunneling Diodes are few of the alternatives. Quantum dot Cellular Automata (QCA) is the most favourable technology to take the place of CMOS technology [1]. QCA is an arithmetic prototype with no transistors, in which quantum dots are used for the implementation of cellular computation. QCA is based on the concept of the physics of interaction between the electrons. No current flows through the cells of the Quantum dots and the device performance is achieved by the coupling of the cells. The binary information in QCA is represented on cells [4]. Operating speed of tetra hertz and also the device density of 10^{12} devices/cm^2 can be achieved by QCA technology. The method of computation by QCA technology offers impressive properties of QCA such as ultra-low power dissipation, highly low power delay product, the non-complicated interconnects, and also as the dots of the QCA are very small in size hence it is possible to have very high packing densities and fast operating speed of frequency range of tetra hertz [5]. Hence, because of the ultra-low size feature of QCA, it is the strongest alternative to CMOS technology among the rest [4]. The main advantages of QCA over CMOS technology are lesser delay, high density circuits and low power consumption which allows us to carry out quantum computing is not in so distant future [6].

A brief review of QCA along with clocking scheme is stated in the Sect. 2 of this paper. Furthermore, the paper is arranged as: In Sect. 3 some related work for the synchronous counter in QCA is discussed. In Sect. 4, the design and implementation of a 2-bit and 3-bit synchronous counter using J-K flip-flop are presented. Simulation results and waveform are shown in Sect. 5. And in the last section of the paper conclusion is given.

2 QCA Review

2.1 QCA Building Blocks

The primary entity of QCA is a cell. Figure 1(1) shows schematics of QCA cell, a regular QCA cell have four quantum dots in a square nanostructure [7]. Dots are said as the places where a charge can be settled down. Each cell is filled with two electrons, and these electrons tends to penetrate in between the four quantum dots of a cell. Tunneling process only take place inside the cell and no tunneling exists among the two cells [8]. In a cell, the enumeration of the quantum dots (represented by i) is started from the top right quantum dot and then proceeds in clockwise direction [9].

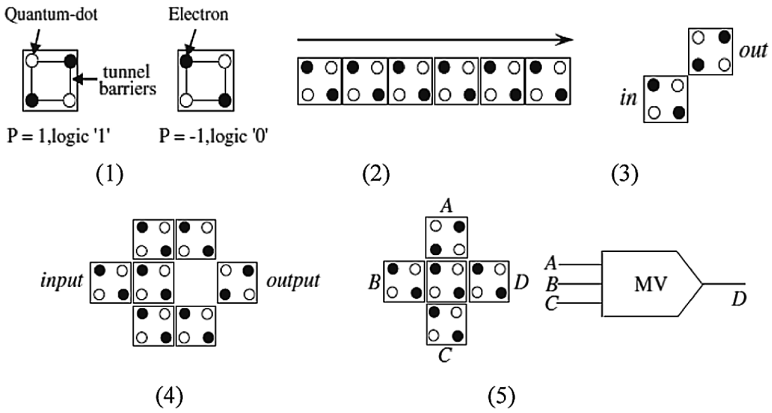

Fig. 1. Representation of a QCA device, (1) cell; (2) wire; (3) and; (4) inverter; (5) majority gate.

In QCA, binary data is represented by the place taken by the mobile electrons in all logic cell. The electrons under the control of the timing plan are set free whenever the barriers between the dots are very low, due to columbic repulsion these two electrons have tendency to hold counter sites within the cell as demonstrated in Fig. 1(1). The two charge presentation with a polarization of −1 and +1 is used to indicate the logic 0 and logic 1 respectively as represented in Fig. 1(1) [7, 10]. A cell will align its polarization with respect to its nearby driver cell whose polarization is fixed. It has been seen that there is extremely non-linear cell to cell interaction, which means a cell with a weak polarization can produces an approximately completely polarized output cell. Thus, along a line of coupled QCA cells, the data can be exchanged by communication among adjacent cells. In QCA a wire is an arrangement of cells placed in series as represented in Fig. 1(2), where the cells are besides to one another. QCA gives a procedure for exchanging data without current flow because there is no transferring of electrons between the cells [9]. The easiest way to build inverter in QCA is by keeping the QCA cells in cater-cornered position as represented in Fig. 1(3), usually seven cells are needed to build the inverter as shown in Fig. 1(4) [11]. The output of the QCA cell has the opposite polarization to that of the input cell. Majority gate is one of the fundamental gate other than the inverter that is used to implement any logical calculations in QCA technology [12]. The majority voter and its logical symbol is shown in Fig. 1(5) [11, 13].

2.2 QCA Clocking

Clock signals are given to the QCA circuits to function properly, that controls and monitors the data transferring and moreover gives the true power gain for that circuit. QCA devices are provided with clocking system in order to provide synchronization in implementing pipelining. The clock is applied to all the four zones, each zone comprises of four phases. The four phases of each zone are the switch phase, hold phase, release phase and relax phase [6]. The barrier between the quantum dots of electron location is raised or lowered by using clock signal [14].

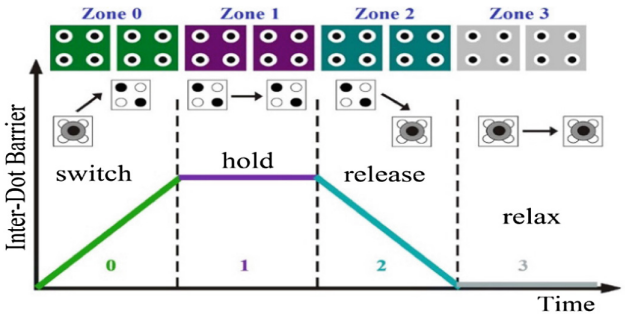

Fig. 2. Clocking phases of clocking zone in QCA.

Figure 2 represents the clocking zone and its different phases. In QCA different colours are used to represent different clock zones, for example, in QCA Designer E simulator, green colour is used to denote zone 0, magenta denotes zone 1, blue colour denotes zone 2 and white colour denotes zone 3 [9].

3 Previous Works

In this section of the paper, review and analysis of counter designs have been discussed. It is much in evidence that most of the earlier research is restricted to implement small logical calculations [15–18]. In QCA up to the present time configurable memory designs are not analysed. To depict a less complex and well organized counter design, some work have been done up till date. Different authors put forward the different approach for designing a sequential circuit [19–22]. A. Vetteth et al. [19] proposed the first three- input majority gate based JK flip-flop. The associated comparison of the reviewed conventional design of counter in QCA is encapsulated in Table 1.

Table 1. Comparison of previous designs of counter using QCA technology.

S. No.	References	Advantages	Disadvantages
1.	Abutaleb et al. [20]	Low power dissipation and low complexity	High delay and susceptible to noise
2.	Sarmadi et al. [21]	Low circuit complexity, high noise, remove hardware overhead	High delay, low practical aspect
3.	Angizi et al. [22]	Low area and cell count, low leakage energy	Susceptible to noise, high delay
4.	Askari et al. [23]	Low area, low cell count	High delay, feedback path
5.	Khan and Chakrabarty [30]	Less consumption of extra area, low expenses of designing, high reliability	Size limitation, less efficient usage of wire connections

Keeping in view the reduction in hardware requirements, a well-organized circuit diagram for JK flip-flop with reduced circuit design [31] is extremely favourable in designing various sequential circuits. The schematic diagram of JK flip-flop demonstrated in Fig. 3, is made up of four majority gates and two inverters [31].

$$Q(out) = JQ^{'} + K'Q \tag{1}$$

The complement of input K is fed to one of input of the majority gate M1 and the output Q is feedback to the circuit to another input of the majority gate M1. The output JQ′ + KQ′ is produced from the majority gate M2 which acts as OR gate. The clock input combined with the output of M1 and M3 are fed to the inputs of the majority gate M2. Equation (1) produces the desired characteristics of JK flip flop.

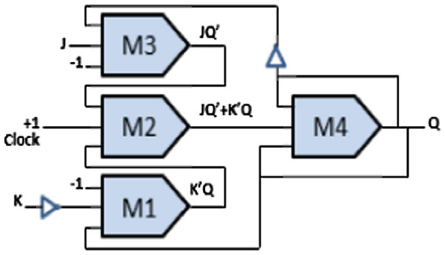

Fig. 3. Majority gate based JK flip flop.

4 Proposed Work

4.1 Implementation of JK Flip-Flop

Flip-flops are the basic structural constituents for designing sequential circuits. Output of the flip-flops depends on both the present input and the previous output [15]. It is a primary one bit element in a sequential circuit that acts as binary storage [12]. In order to implement the proposed synchronous counter, the schematic of JK flip-flop in Fig. 3 is accomplished by using the three input majority gate structure. The schematic layout of JK flip-flop in QCA is shown in Fig. 4.

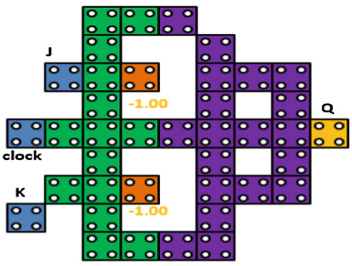

Fig. 4. Layout of JK flip flop in QCA.

4.2 Proposed Design of Synchronous Counter

Synchronous counters are widely employed in digital circuits using four types of flip-flops. The application of synchronous counters are to divide frequency, count time and pulse [11]. This section of the paper presents a highly optimized configuration of a n-bit synchronous counter. In synchronous counter each flip-flop is triggered via a single clock pulse. The counter output continuously changes depending on the either edge of the clock. The proposed mod-4 (2-bit) synchronous counter can further be modified to mod-8 (3 bit), mod-16 (4-bit) and more. The purposed design is composed of JK flip-flop and other combinational logic circuits.

As illustrated in Figs. 5 and 6, the purposed synchronous counter is comprised of two JK flip-flops which are connected together and edge triggering mechanism is provided by connecting each JK flip-flop to a single clock. This paper presents only 2-bit and 3-bit synchronous counter. In the proposed architecture of synchronous counter, two JK flip-flops are employed and are clocked by a single clock simultaneously. The presented design of synchronous counter can be expanded in an n-bit synchronous counter.

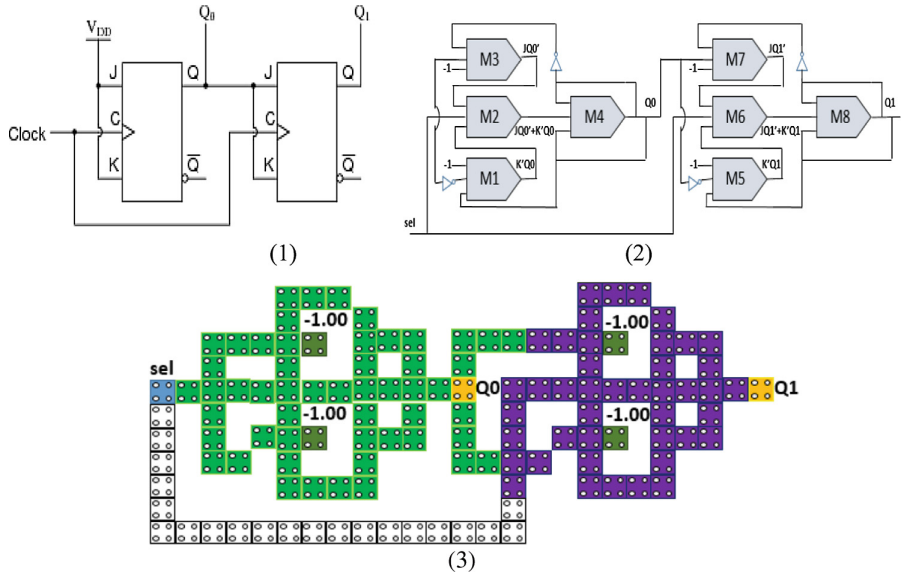

Fig. 5. Proposed QCA-based 2-bit synchronous counter. (1) block diagram, (2) schematic diagram and (3) QCA layout.

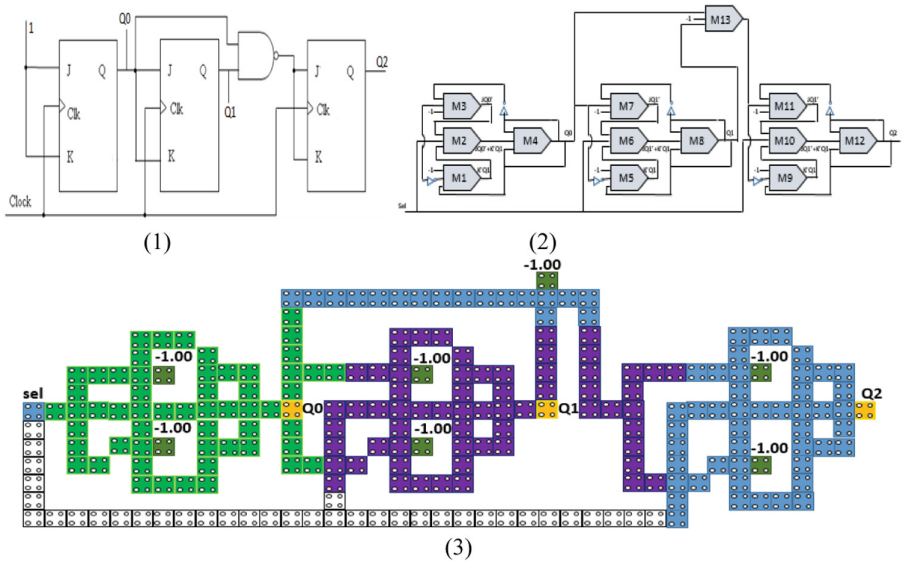

Fig. 6. Proposed QCA-based 3-bit synchronous counter. (1) block diagram, (2) schematic diagram and (3) QCA layout.

5 Results and Discussion

QCADesigner E bistable engine is used to validate the functionality of the purposed designs. In this section of the paper, the proposed synchronous counter is simulated using QCADesigner E tool. The remaining part of this section presents the simulation process.

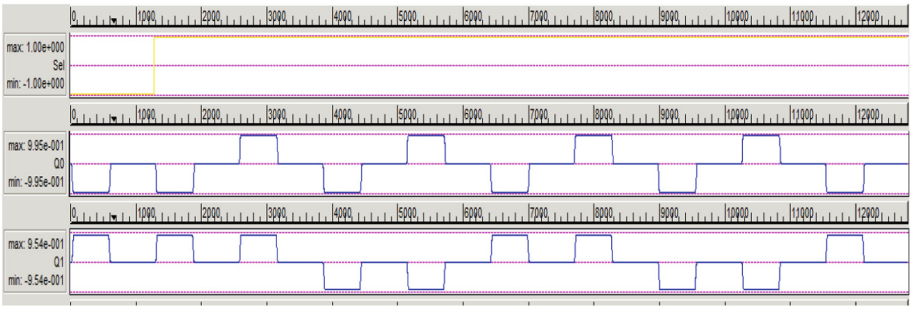

Fig. 7. Simulation waveform of 2-bit synchronous counter.

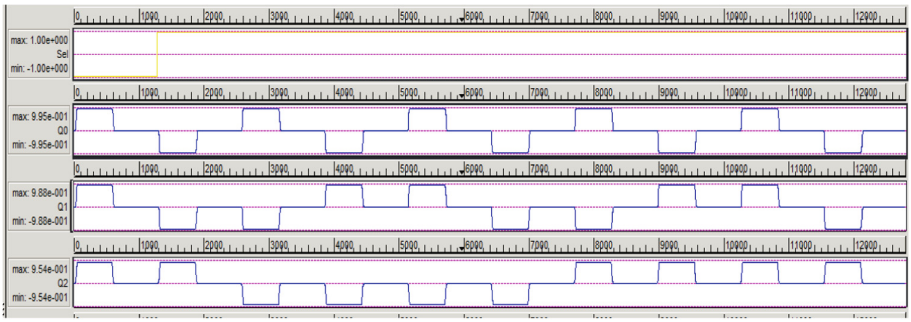

Fig. 8. Simulation waveform of 3-bit synchronous counter.

QCADesigner E tool is used for the simulation purpose of the purposed designs, it also contributes in optimization of power consumption to the best possible extent. As illustrated in Fig. 5(3), the output (Q1) of the first flip-flop is linked to the inputs (J & K) of the next flip-flop. The working of the proposed synchronous counter can be explained such that a 2-bit synchronous counter have two outputs and one input called sel (select). Therefore, for a 3-bit synchronous counter, there are three outputs and one input. For a 2-bit synchronous counter, 2^2 i.e. 4 combinations of output are formed. A selection line which acts as the enable signal is provided to the proposed synchronous model to produce output of the proposed model, which means sel (select) line controls the on and off series of the circuit. The mentioned operation is based on the low or high input at the sel (selection) line. The simulation waveform of the purposed 2-bit and 3-bit counter is presented in Figs. 7 and 8 respectively. To check the design functionality of the proposed counter QCADesigner E tool has been used. The accurate function of the purposed 2-bit synchronous counter is verified by the Fig. 7. From the simulation results, the counting operation is correctly realized for outputs-Q0 and Q1.

5.1 Comparison

The proposed synchronous counters are compared with the previous designs of synchronous counters and is summarized in Table 2. Clearly it is noticeable that the purposed design results in significant advancement in respect of complexity, area occupied and latency in contrast to the prior designs.

The proposed 2-bit and 3-bit synchronous counter uses 123 and 226 cells respectively. The latency for the proposed counters is 1 clock cycle, which is a very low latency. By minimizing the cells count and occupied area of the design, power dissipation of the design can be reduce.

The total energy dissipation (Sum_Ebath) of 2-bit synchronous counter using the QCADesigner E tool obtained is 3.56e-002 eV (Error: +/− −2.88e-003 eV) and the average energy dissipation per cycle (Avg_Ebath) of 2-bit synchronous counter obtained is 3.23e-003 eV (Error: +/− −2.62e-004 eV). The total energy dissipation (Sum_Ebath) and the average energy dissipation per cycle (Avg Ebath) of 3-bit synchronous counter using QCADesigner E tool obtained are 6.05e-002 eV (Error: +/−

−4.71e-003 eV) and 5.50e-003 eV (Error: +/− −4.28e-004 eV) respectively. Keeping in view the values of energy dissipation attained through QCADesigner E tool, Figs. 9 and 10 illustrate the noticeable optimization in power dissipation of proposed 2-bit and 3-bit synchronous counter respectively.

Table 2. Comparison of existing QCA-based synchronous counter designs.

Design	Area (μm^2)	Complexity (cell counts)	Latency (clock cycle)
2-bit synchronous counter			
C.-B. Wu et al. [24]	0.74	430	4
S. Sheikhfaal et al. [25]	0.26	240	2
S. Angizi et al. [26]	0.22	141	2.25
A. M. Chabi et al. [27]	0.67	464	5.75
M. Goswami et al. [28]	0.62	328	3
Proposed 2-bit counter design	0.11	123	1
3-bit synchronous counter			
C.-B. Wu et al. [24]	1.02	677	6
S. Sheikhfaal et al. [25]	0.48	428	2
S. Angizi et al. [26]	0.36	328	2.25
M. Abutaleb et al. [20]	0.22	196	5.75
M. Goswami et al. [28]	1.18	786	7.75
Proposed 3-bit counter design	0.24	226	1

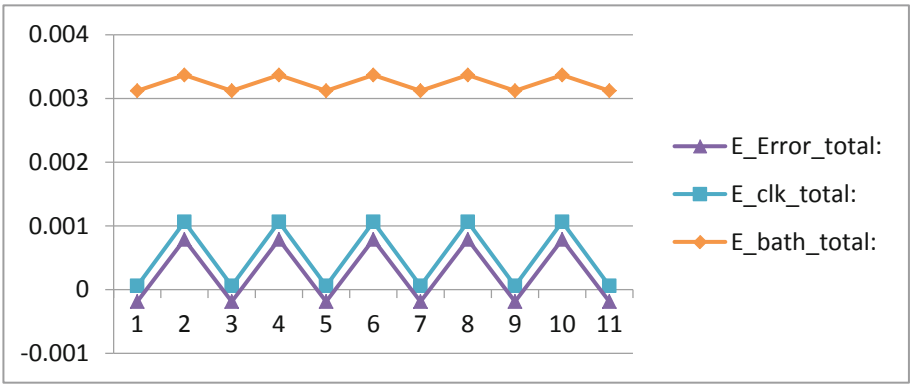

Fig. 9. The illustration of energy dissipation of 2-bit synchronous counter.

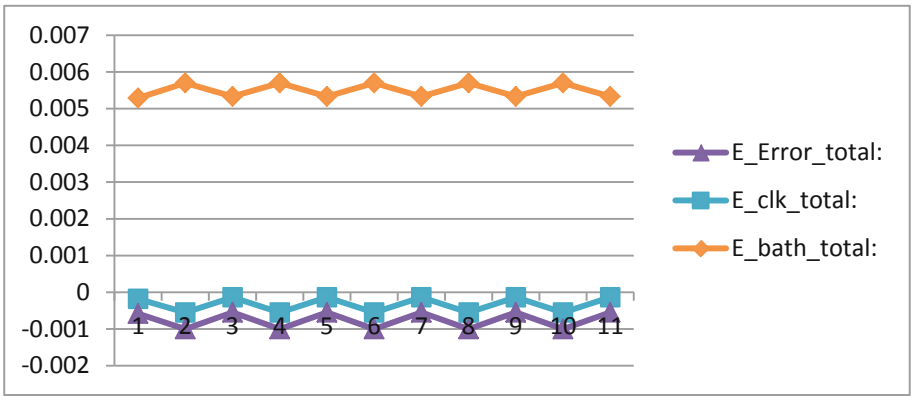

Fig. 10. The illustration of energy dissipation of 3-bit synchronous counter.

6 Conclusion

With the unique specifications Quantum dot cellular automata decreases the physical limit of CMOS devices realization. Hence it inspires researchers to bring into play the QCA technology for designing various integrated circuits. This paper brings a well efficient realization of synchronous counter design using well-optimized JK flip-flops. Less cell count, low area consumption and delay are considered as the advantages of the proposed design in contrast to the available designs. QCADesigner tool is used for the QCA layout and validation of purposed designs. A well considerable improvement in respect of area, complexity and delay of proposed synchronous counter is visible from the simulation results and a comprehensive contrast among the proffered and the previous counter designs have been derived in regards of power dissipation, area and hardware complexity. The comparisons verify that the presented design of this paper is more advantageous in all the mentioned parameters. Moreover, efficient 4 bit and n-bit QCA based synchronous counters from the proposed design can be constructed. It is feasible to employ the purposed design as a basic sequential component for a larger QCA designs such as memory units, nano processor and ALU. It can be concluded that the clock delay of QCA-based circuits is very low and can be even neglected.

References

1. Mehta, U., Dhare, V.: Quantum-dot Cellular Automata (QCA): A Survey. arXiv preprint arXiv:1711.08153 (2017)
2. Abdullah-Al-Shafi, M., et al.: Designing single layer counter in quantum-dot cellular automata with energy dissipation analysis. Ain Shams Eng. J. **9**, 2641–2648 (2018)
3. Peercy, P.S.: The drive to miniaturization. Nature **406**(6799), 1023 (2000)
4. Bilal, B., Ahmed, S., Kakkar, V.: Quantum dot cellular automata: a new paradigm for digital design. Int. J. Nanoelectronics Mater. **11**(1) (2018)

5. Sheikhfaal, S., Angizi, S., Sarmadi, S., Moaiyeri, M.H., Sayedsalehi, S.: Designing efficient QCA logical circuits with power dissipation analysis. Microelectronics J. **46**(6), 462–471 (2015)
6. Goswami, M., Mondal, A., Mahalat, M.H., Sen, B., Sikdar, B.K.: An efficient clocking scheme for quantum-dot cellular automata. Int. J. Electron. Lett. 1–14 (2019)
7. Amirzadeh, Z., Gholami, M.: Counters designs with minimum number of cells and area in the quantum-dot cellular automata Technology. Int. J. Theor. Phys. 1–18 (2019)
8. Ramachandran, S.S., Kumar, K.J.: Design of a 1-bit half and full subtractor using a quantum-dot cellular automata (QCA). In: IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), IEEE, pp. 2324–2327 (2017)
9. Liu, W., Swartzlander Jr., E.E., O'Neill, M.: Design of Semiconductor QCA Systems. Artech House (2013)
10. Liu, W., Lu, L., O'Neill, M., Swartzlander, E.E.: A first step toward cost functions for quantum-dot cellular automata designs. IEEE Trans. Nanotechnol. **13**(3), 476–487 (2014)
11. Yang, X., Cai, L., Zhao, X., Zhang, N.: Design and simulation of sequential circuits in quantum-dot cellular automata: falling edge-triggered flip-flop and counter study. Microelectronics J. **41**(1), 56–63 (2010)
12. Sangsefidi, M., Abedi, D., Yoosefi, E., Karimpour, M.: High speed and low cost synchronous counter design in quantum-dot cellular automata. Microelectronics J. **73**, 1–11 (2018)
13. Bahar, A.N., Laajimi, R., Abdullah-Al-Shafi, M., Ahmed, K.: Toward efficient design of flip-flops in quantum-dot cellular automata with power dissipation analysis. Int. J. Theor. Phys. **57**(11), 3419–3428 (2018)
14. Sasamal, T.N., Singh, A.K., Ghanekar, U.: Toward efficient design of reversible logic gates in quantum-dot cellular automata with power dissipation analysis. Int. J. Theor. Phys. **57**(4), 1167–1185 (2018)
15. Chakrabarty, R., Mahato, D.K., Banerjee, A., Choudhuri, S., Dey, M., Mandal, N.K.: A novel design of flip-flop circuits using quantum dot cellular automata (QCA). In: IEEE 8th Annual Computing and Communication Workshop and Conference (CCWC), IEEE, pp. 408–414 (2018)
16. Roshan, M.G., Gholami, M.: Novel D latches and D flip-flops with set and reset ability in QCA nanotechnology using minimum cells and area. Int. J. Theor. Phys. **57**(10), 3223–3241 (2018)
17. Biswas, P., Gupta, N., Patidar, N.: Basic reversible logic gates and it's QCA implementation. Int. J. Eng. Res. Appl. **4**(6), 12–16 (2014)
18. Kavitha, S.S., Kaulgud, N.: Quantum dot cellular automata (QCA) design for the realization of basic logic gates. In: 2017 International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), IEEE, pp. 314–317 (2017)
19. Sarmadi, S., Azimi, S., Sheikhfaal, S., Angizi, S.: Designing counter using inherent capability of quantum-dot cellular automata loops. Int. J. Mod. Educ. Comput. Sci. **7**(9), 2 (2015)
20. Sheikhfaal, S., Navi, K., Angizi, S., Navin, A.H.: Designing high speed sequential circuits by quantum-dot cellular automata: memory cell and counter study. Quantum Matter **4**(2), 190–197 (2015)
21. Angizi, S., Moaiyeri, M.H., Farrokhi, S., Navi, K., Bagherzadeh, N.: Designing quantum-dot cellular automata counters with energy consumption analysis. Microprocess. Microsyst. **39**(7), 512–520 (2015)
22. Moharrami, E., Navimipour, N.J.: Designing nanoscale counter using reversible gate based on quantum-dot cellular automata. Int. J. Theor. Phys. **57**(4), 1060–1081 (2018)

23. Vetteth, A., Walus, K., Dimitrov, V.S., Jullien, G.A.: Quantum-dot cellular automata of flip-flops. ATIPS Lab. **2500**, 1–5 (2003)
24. Abutaleb, M.M.: Robust and efficient quantum-dot cellular automata synchronous counters. Microelectron. J. **61**, 6–14 (2017)
25. Angizi, S., Sarmadi, S., Sayedsalehi, S., Navi, K.: Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata. Microelectronics J. **46**(1), 43–51 (2015)
26. Askari, M., Taghizadeh, M., Fardad, K.: Design and analysis of a sequential ring counter for QCA implementation. In: 2008 International Conference on Computer and Communication Engineering, IEEE, pp. 933–936 (2008)
27. Wu, C.B., Xie, G.J., Xiang, Y.L., Lv, H.J.: Design and simulation of dual-edge triggered sequential circuits in quantum-dot cellular automata. J. Comput. Theor. Nanosci. **11**(7), 1620–1626 (2014)
28. Chabi, A.M., Roohi, A., DeMara, R.F., Angizi, S., Navi, K., Khademolhosseini, H.: Cost-efficient QCA reversible combinational circuits based on a new reversible gate. In: 2015 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS), IEEE, pp. 1–6 (2015)
29. Goswami, M., Chowdhury, M.R, Sen, B.: Design of Configurable Sequential Circuits in Quantum-dot Cellular Automata. arXiv preprint arXiv:1708.07616 (2017)
30. Khan, A., Chakrabarty, R.: Design of ring and Johnson counter in a single reconfigurable logic circuit in quantum dot cellular automata. Int. J. Comput. Sci. Technol. **4**, 363–367 (2012)
31. Kalyan, B.S., Singh, B.: Quantum dot cellular automata (QCA) based 4-bit shift register using efficient JK flip flop. Int. J. Pure Appl. Math. **118**, 143–157 (2018)