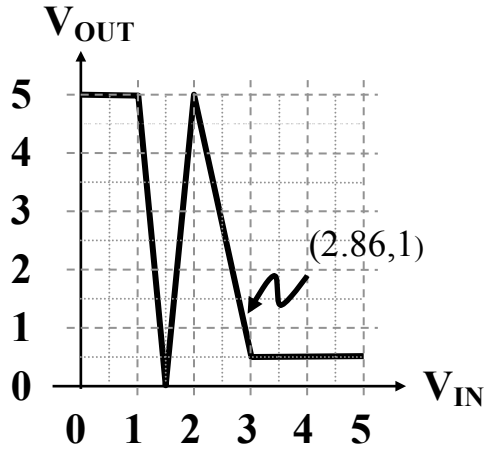
6.004 Tutorial Problems
L05 – The Digital Abstraction

Note: A small subset of essential problems are marked with a red star (★). We especially encourage you to try these out before recitation.

Problem 1. ★

Ms. Anna Logge, founder at a local MIT startup, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The figure on the right shows the voltage transfer curve of a proposed inverter for a new logic family (you can find spare copies below).

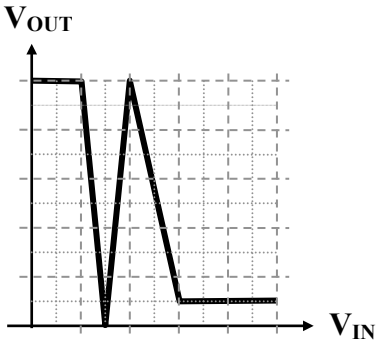


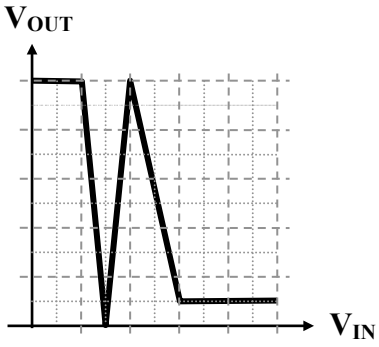
Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. ***Noise Immunity*** **(the last row) is defined as the smaller of the two noise margins**.

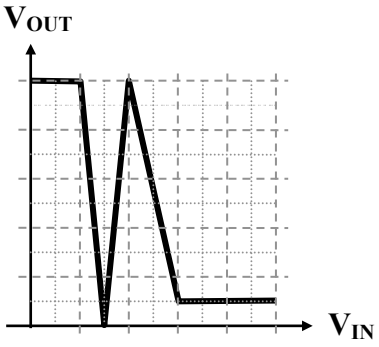
Complete the table by filling in missing entries. Choose each value to maximize the noise margins of the corresponding scheme. **If the numbers in a scheme can't be completed such that the device functions as an inverter with positive noise margins, fill the entries for that column with *X*s.**

LNI's Possible Logic Mappings:

	Scheme A	**Scheme B**	**Scheme C**
V_{OL}	X	0.5	1
V_{IL}	2	1	0.5
V_{IH}	X	3	X
V_{OH}	X	5	X
Noise Immunity	X	0.5	X







Scheme A: illegitimate, V_{IL} = 2 places the "trough" part of the VTC within the "valid input" range; however, since the trough touches the horizontal axis (V_{OUT} = 0), any choice for V_{OL} will cause the VTC to overlap with a forbidden region.

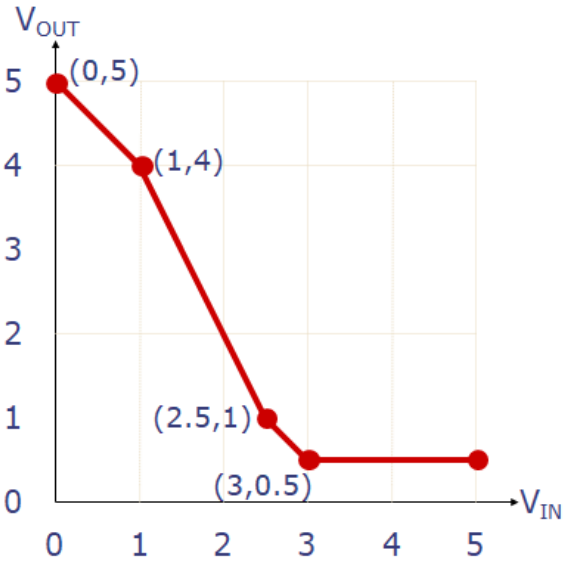
Scheme B: V_{OL} = 0.5, V_{OH} = 5, Noise Immunity = 0.5. The values of V_{IL} = 1 and V_{IH} = 3 exclude the jagged part of the VTC from consideration. Thus, we simply set V_{OL} = 0.5 (the value of V_{OUT} for V_{IN} > 3) and set V_{OH} = 5 (the value of V_{OUT} for V_{IN} < 1) to maximize our noise margins. We calculate our noise immunity as:

Noise Immunity = min(5-3, 1-0.5) = 0.5

Scheme C: illegitimate, since $V_{OL} < V_{IL} < V_{IH} < V_{OH}$ must hold for a legitimate specification.

Problem 2.

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification (V_{IL}, V_{IH}, V_{OL}, V_{OH}) that would allow this device to be a digital inverter? If so, give the specification that maximizes noise margin.



Note: Noise Margin = min(Low Noise Margin, Max Noise Margin)

In general, we can solve these optimization problems for simple, step-wise VTC curves by choosing the most extreme values for V_{OH} and V_{OL} (i.e. maximizing V_{OH} -V_{OL}) and moving those lines more centrally until we have legitimate specifications. Often, we will discover constraints that define a strict relationship between the aforementioned output voltages and the input voltages V_{IH} and V_{IL}; thus, selecting optimal V_{OH} and V_{OL} imply an optimal V_{IH} and V_{IL} in these cases. Here is an example of how you might optimize:

Iteration 1: $V_{OL} = 0.5$, $V_{OH} = 5$ => $V_{IL} = 0$, $V_{IH} = 3$
(illegitimate because $V_{IL} = 0$ is impossible)

Iteration 2: $V_{OL} = 0.5$, $V_{OH} = 4$ => $V_{IL} = 1$, $V_{IH} = 3$
(legitimate; yields a Low Noise Margin of 1 – 0.5 = 0.5 and a High Noise Margin of 4 – 3 = 1)

At this point, we notice that the limiting factor in maximizing the Noise Margin is the Low Noise Margin. Thus, since we cannot decrease V_{OL} any further, we must increase V_{IL} to optimize. However, notice that increasing further implies a decrease in order to keep the VTC outside of the forbidden regions. Thus, we will eventually reach an equilibrium at which the noise margins are equal:

$$V_{OH} - V_{IH} = V_{IL} - V_{OL}$$

Noting that the optimal point (V_{IL}, V_{OH}) lies in the middle segment of the graph and that this segment has slope (1-4)/(2.5-1) = -2, we have:

$$V_{OH} = 4 - 2(V_{IL} - 1)$$

$$[4 - 2(V_{IL} - 1)] - 3 = V_{IL} - 0.5 \Rightarrow V_{IL} = 7/6 \Rightarrow V_{OH} = 4 - 2(7/6 - 1) = 11/3$$

Problem 3. ★

Suppose we define all signaling thresholds in our digital system to be relative to the supply voltage, V_{DD}:

- $V_{OL} = 0.1V_{DD}$
- $V_{IL} = 0.4V_{DD}$
- $V_{IH} = 0.6V_{DD}$
- $V_{OH} = 0.9V_{DD}$

$V_{DD,A} = 1V$

$V_{OL,A} = 0.1V$

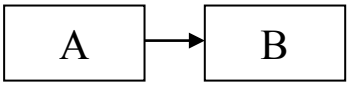
$V_{IL,A} = 0.4V$

$V_{IH,A} = 0.6V$

$V_{OH,A} = 0.9V$

We want to connect two types of digital devices, A and B, that use different supply voltages, $V_{DD,A}$ and $V_{DD,B}$. **Assume that $V_{DD,A} = 1V$.**

(1) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



Outputs of A must be valid inputs to B

$V_{OL,A} \le V_{IL,B}$

$0.1 \le 0.4 V_{DD,B}$

$0.25 \le V_{DD,B}$

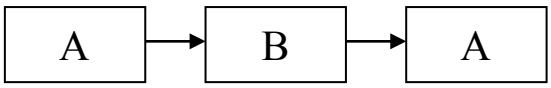
$V_{OH,A} \ge V_{IH,B}$

$0.9 \ge 0.6 V_{DD,B}$

$1.5 \ge V_{DD,B}$

$\boxed{0.25 \le V_{DD,B} \le 1.5}$

(2) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



Additional constraints: outputs of B are valid inputs to A

$V_{OL,B} \le V_{IL,A}$

$0.1 V_{DD,B} \le 0.4$

$V_{DD,B} \le 4$ (already satisfied)

$V_{OH,B} \ge V_{IH,A}$

$0.9 V_{DD,B} \ge 0.6$

$V_{DD,B} \ge 2/3$

$\boxed{\frac{2}{3} \le V_{DD,B} \le 1.5}$

(3) For the same circuit as in part 2, under what range of supply voltages $V_{DD,B}$ will the system have noise margins of at least 0.1V?

$V_{OL,A} + 0.1 \le V_{IL,B}$

$V_{OH,A} - 0.1 \ge V_{IH,B}$

$0.5 \le V_{DD,B} \le 4/3$

$V_{OL,B} + 0.1 \le V_{IL,A}$

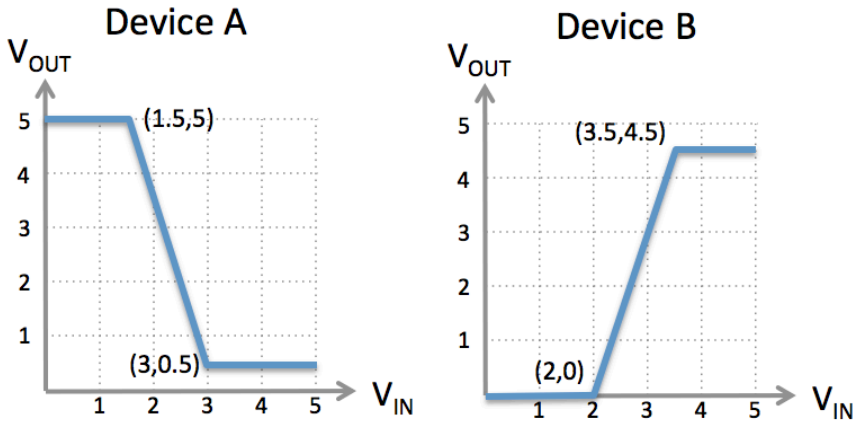
$V_{OH,B} - 0.1 \ge V_{IH,A}$

$7/9 \le V_{DD,B} \le 3$

$\boxed{\frac{7}{9} \le V_{DD,B} \le \frac{4}{3}}$

Problem 4. ★

The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:



Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize the noise immunity (i.e., the smaller of the two noise margins).

V_{OL} = _0.5__ V_{IL} = _1.67_ V_{IH} = _3.5__ V_{OH} = _4.5__

Low Noise Margin = _1.17_ High Noise Margin = __1__

Note: Noise Margin = min(Low Noise Margin, Max Noise Margin)

As in Problem 1, we begin our optimization by choosing the most extreme values for V_{OH} and V_{OL} (i.e. maximizing $V_{OH} - V_{OL}$) and moving those lines more centrally until we have legitimate specifications. In this case, we must pay attention to the VTCs of two devices simultaneously. Here is an example of how you might optimize:

Iteration 1: $V_{OL} = 0$, $V_{OH} = 5$ => $V_{IL} = 1.5$, $V_{IH} = 3$
(illegitimate because $V_{OL} = 0$ is impossible; also, both VTCs overlaps forbidden regions)

Iteration 2: $V_{OL} = 0.5$, $V_{OH} = 4.5$ => $V_{IL} = 1.5$, $V_{IH} = 3$
(better, but still illegitimate because V_{IH} is too low)

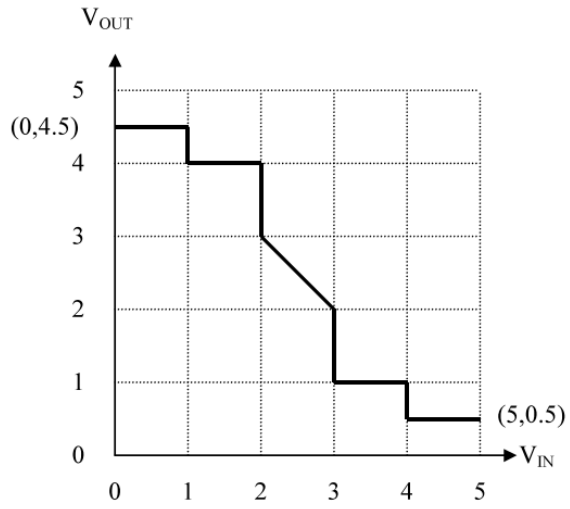
Iteration 3: $V_{OL} = 0.5$, $V_{OH} = 4.5$ => $V_{IL} = 1.5$, $V_{IH} = 3.5$
(legitimate)

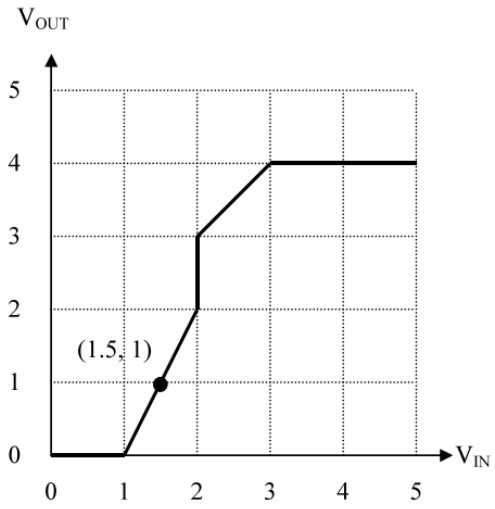
Graphically, we see that we cannot improve the High Noise Margin any further. However, for the sake of completeness, we can continue optimizing the Low Noise Margin.

Iteration 4: $V_{OL} = 0.5$, $V_{OH} = 4.5$ => $V_{IL} = 1.67$, $V_{IH} = 3.5$
(legitimate; we simply traced a horizontal line at $V_{OH} = 4.5$ to find where it intercepts Device A's VTC. This point is the largest threshold for V_{IL} can achieve)

Problem 5.

The following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:



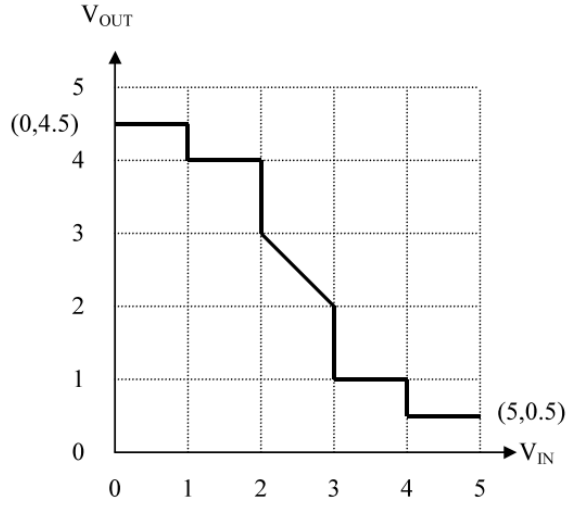


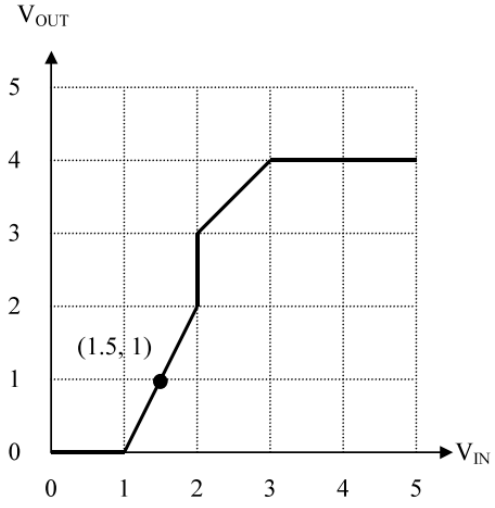
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

V_{OL} = __1__ V_{IL} = _1.5__ V_{IH} = __3__ V_{OH} = __4__

Low Noise Margin = _0.5_ High Noise Margin = __1__

Scratch copy of the VTC diagrams:





Note: Noise Margin = min(Low Noise Margin, Max Noise Margin)

As in Problem 4, we begin our optimization by choosing the most extreme values for V_{OH} and V_{OL} (i.e. maximizing $V_{OH} - V_{OL}$) and moving those lines more centrally until we have legitimate specifications. Here is an example of how you might optimize:

Iteration 1: $V_{OL} = 0$, $V_{OH} = 4.5$ => $V_{IL} = 0$, $V_{IH} = 5$
(illegitimate because V_{OL}, $V_{IL} = 0$ is impossible; also, VTC overlaps forbidden regions)

Iteration 2: $V_{OL} = 0.5$, $V_{OH} = 4$ => $V_{IL} = 1.25$, $V_{IH} = 4$
(legitimate; we get $V_{IL} = 1.25$ and $V_{IH} = 4$ by drawing a horizontal line at $V_{OL} = 0.5$ and seeing where it intercepts the second and first VTCs, respectively)

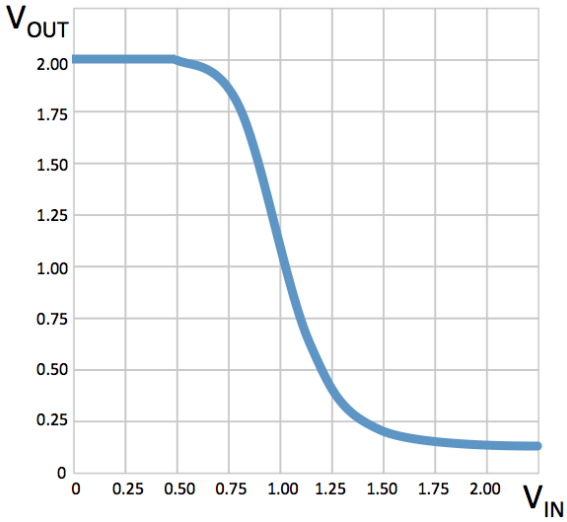
At this point, we can calculate that the Low Noise Margin = 0.75 and the High Noise Margin = 0. Clearly, we need to increase the High Noise Margin to improve our overall result. Since we cannot increase our V_{OH}, we must instead decrease our V_{IH}, and we can afford to sacrifice the size of our Low Noise Margin to achieve this.

We increase V_{OL} by the smallest possible increment (0.5) in order to decrease our V_{IH} while keeping a legitimate specification.

Iteration 3: $V_{OL} = 1$, $V_{OH} = 4$ => $V_{IL} = 1.5$, $V_{IH} = 3$
(legitimate and optimal; Low Noise Margin = 0.5 and High Noise Margin = 1)

Problem 6. ★

The voltage transfer curve for an inverter is shown to the right. The manufacturer decided to crowdsource the digital signaling specifications for their inverter and has received some suggestions for V_{OL}, V_{IL}, V_{IH}, and V_{OH}, presented in tabular form below.



For each suggested specification, determine if the inverter would be a legitimate combinational device with non-zero positive noise margins. If it is a legitimate combinational device, give the noise immunity of the inverter (the smaller of the low and high noise margins) when operating under that specification. If the inverter wouldn't be a legitimate combinational device, please write NOT LEGIT in the rightmost column.

Fill in rightmost column for each suggested specification.

Suggestion	V_{OL}	V_{IL}	V_{IH}	V_{OH}	*Noise immunity, or NOT LEGIT*
#1	0.00	0.50	1.50	2.00	Not legit
#2	0.25	0.75	1.25	1.75	Not legit
#3	0.50	0.75	1.25	1.50	0.25
#4	0.75	0.50	1.75	1.50	Not legit

#1: Can't produce $V_{OL} = 0$ output

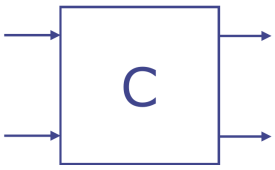
#2: Test: For $V_{in} \geq V_{IH} = 1.25$, is $V_{out} \leq V_{OL} = 0.25$? Not satisfied

#3: Valid

#4: Test: Is $V_{OL} < V_{IL} < V_{IH} < V_{OH}$? Not satisfied

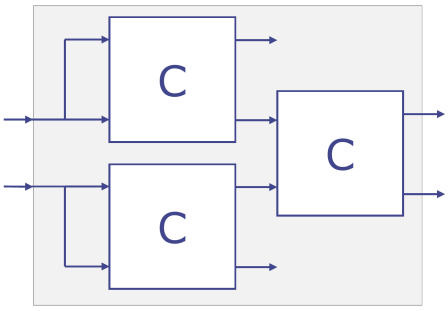
Problem 7. ★

The circuit C shown below is a 2-input, 2-output combinational device.

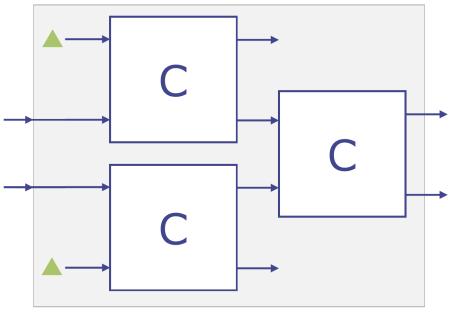


Each of the three circuits below contains multiple copies of circuit C. **Note**: the ▲ symbol indicates a "floating" input.

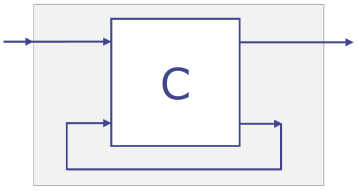
Circuit 1



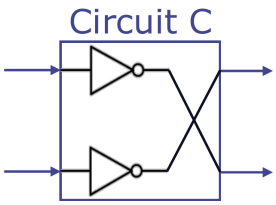
Circuit 2



Circuit 3



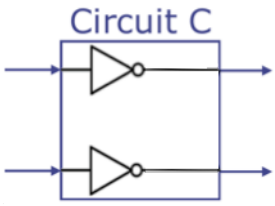
(A) Below is one possible implementation of C:



Given this implementation, determine which of the above circuits are combinational.

Circuit 1 _Yes_ **Circuit 2** _No_ **Circuit 3** _Yes_

(B) Below is an alternative implementation of C:



Given this alternative implementation, determine which of the above circuits are combinational.

Circuit 1 _Yes_ **Circuit 2** _Yes_ **Circuit 3** _Yes_

A) Circuit 1: This is combinational, which we can determine by tracing paths from the inputs to the outputs.

Circuit 2: This is not combinational, because the floating inputs may be invalid even when the original inputs to the circuit are valid, and since this floating inputs affect the outputs of the circuits, we may obtain invalid outputs even with valid inputs.

Circuit 3: This is combinational, which we can determine by tracing paths from the input to the output. In fact, this circuit simply copies its input to the output.

B) Circuit 1: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply copies its inputs to the outputs.

Circuit 2: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply copies its inputs to the outputs. Note that the floating inputs do not affect the outputs, which is why this circuit is still combinational despite their presence.

Circuit 3: This is combinational, which we can determine by tracing paths from the inputs to the outputs. In fact, this circuit simply inverts its input. Note that the directed cycle in this circuit stands alone and does not affect the output, which is why it is still combinational