The Digital Abstraction and Sequential Timing Constraints

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Quiz 3: Tonight 7:30-9:30PM in
34-101 (A-S) and 32-155 (T-Z)

All labs must be checked off by
next Thursday (May 16).

Design project due on Thursday.

What have we learned in 6.004?

- Programming in Assembly
- Binary Representation
- Combinational Circuits
- Logic Optimization using Boolean Algebra
- Sequential Circuits
- Concurrency
- Processor Implementation
- Caches
- OS & Virtual Memory
- Pipelining
- Pipelined Processors
- Synchronization

What assumptions did we make?

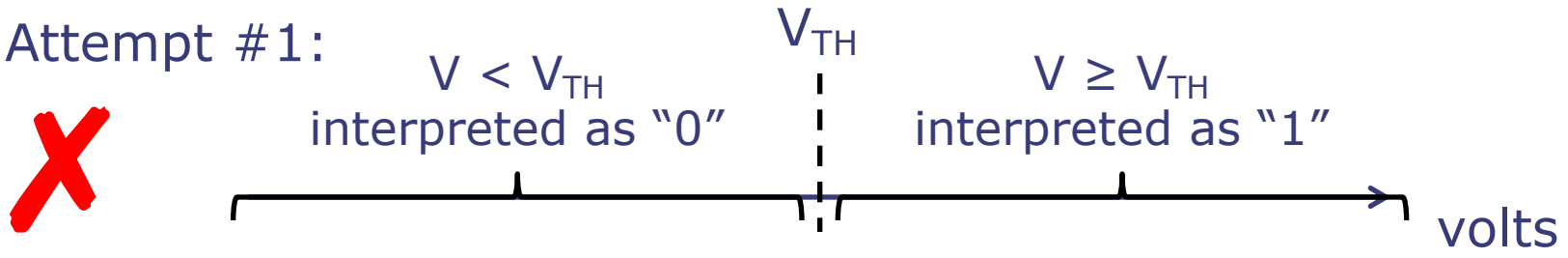
- Combinational logic gates satisfy the *digital abstraction*.
  - Digital abstraction ensures that logic gates can tolerate noise and are restorative in that errors don't accumulate
- Sequential circuits satisfy the required *timing constraints*
  - Data must be stable around the rising edge of the clock to ensure proper behavior of sequential circuits

The Digital Abstraction

Using Voltages "Digitally"

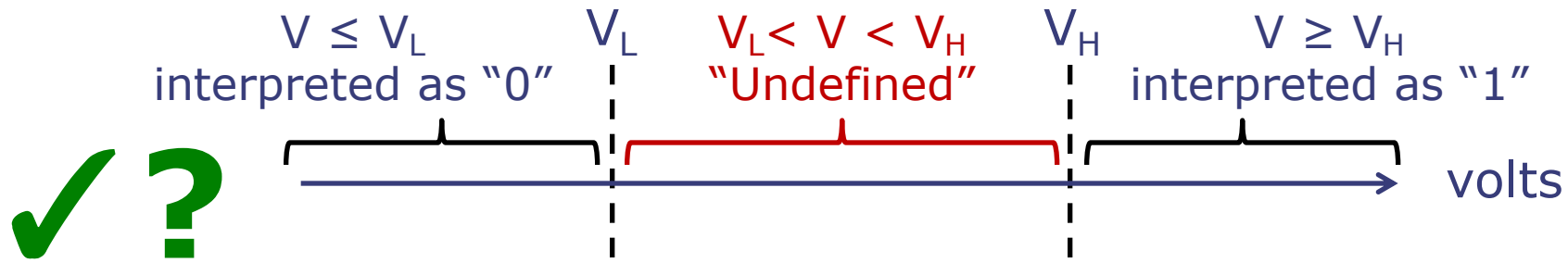
- Key idea: Encode two symbols, "0" and "1" (1 bit) using voltages (an analog, continuous value)
- Use the same convention for *every* component and wire in our digital system

Attempt #1:

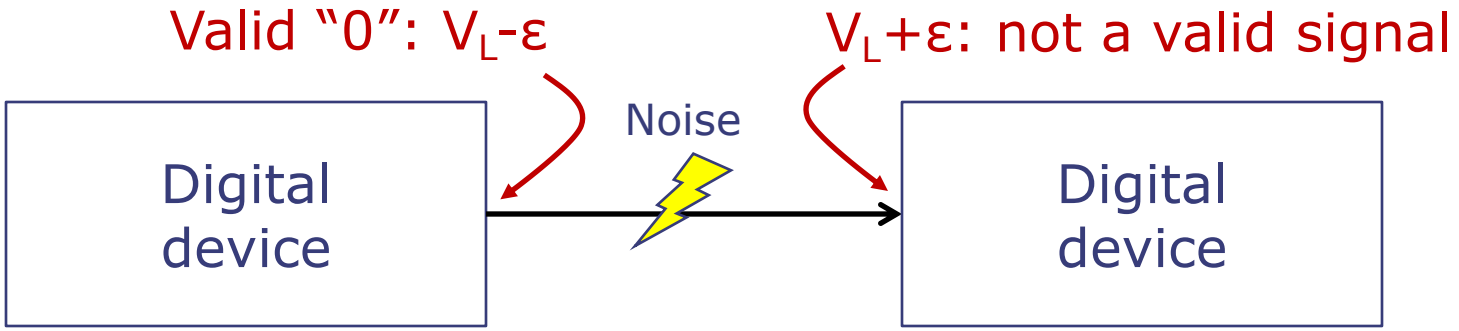


Not quite correct. Why? *Hard to distinguish V_{TH}-ε from V_{TH}+ε*

Attempt #2:



Will This System Work?



Upstream device transmits a signal at V_L-ε, a valid "0". Noise on the wire causes the downstream device to receive V_L+ε, which is undefined.

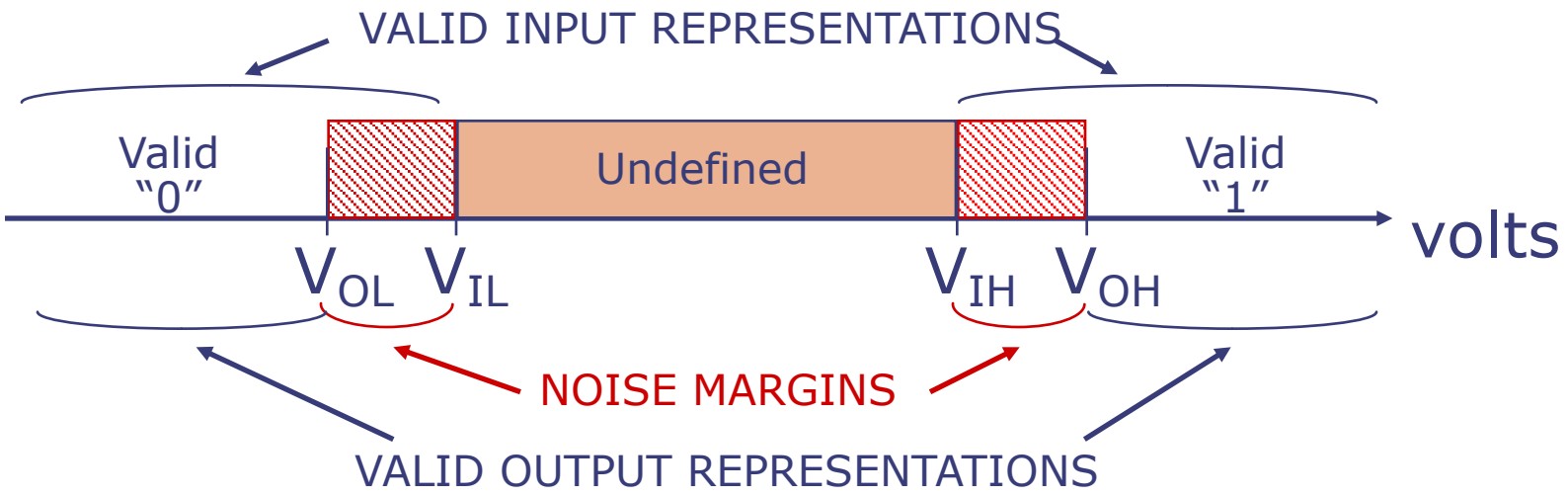
How can we address this?

Output voltages should use narrower ranges, so that signal will still be valid when it reaches an input even if there is noise.

Noise Margins

Proposed fix: Different specifications for inputs and outputs

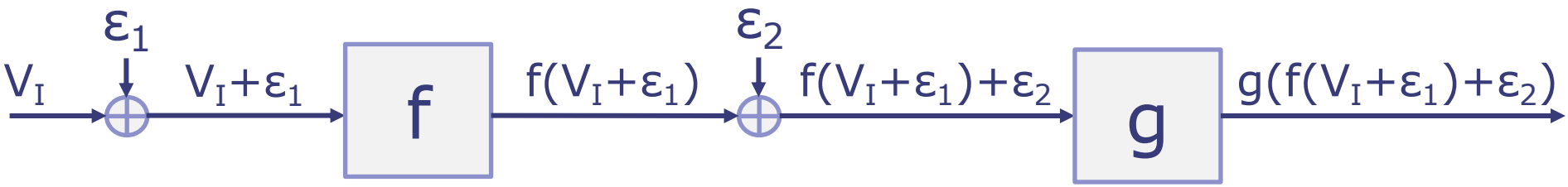
- Digital output: "0" ≤ V_{OL}, "1" ≥ V_{OH}
- Digital input: "0" ≤ V_{IL}, "1" ≥ V_{IH}
- **$V_{OL} < V_{IL} < V_{IH} < V_{OH}$**



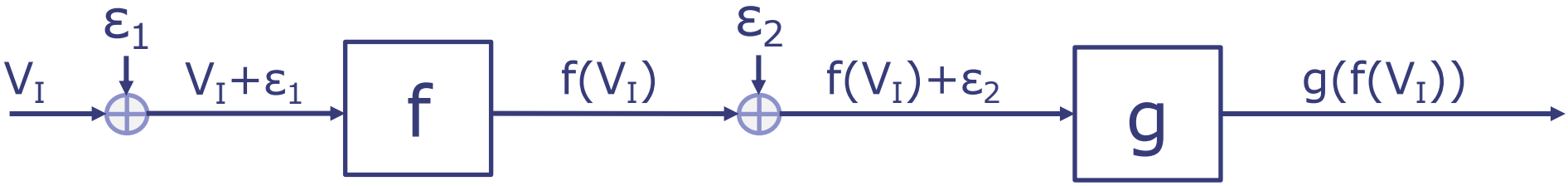
A digital device accepts marginal inputs and provides unquestionable outputs (to leave room for noise).

Digital Systems are Restorative

Analog systems: Noise accumulates



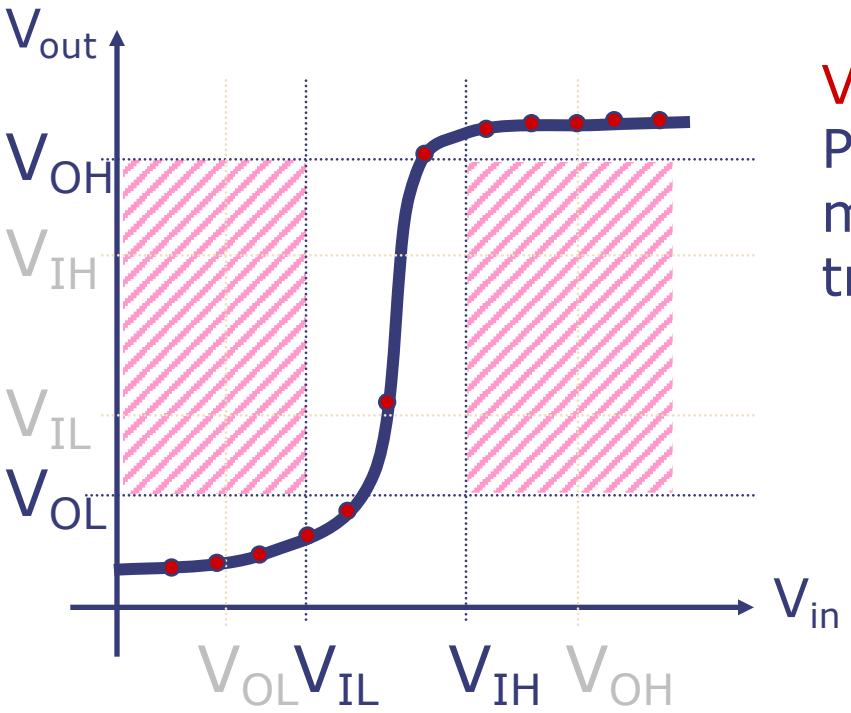
Digital systems: Noise is canceled at each stage



Intuitively, canceling noise requires active components, i.e., components that inject energy into the system

Voltage Transfer Characteristic

Buffer: A simple digital device that copies its input value to its output

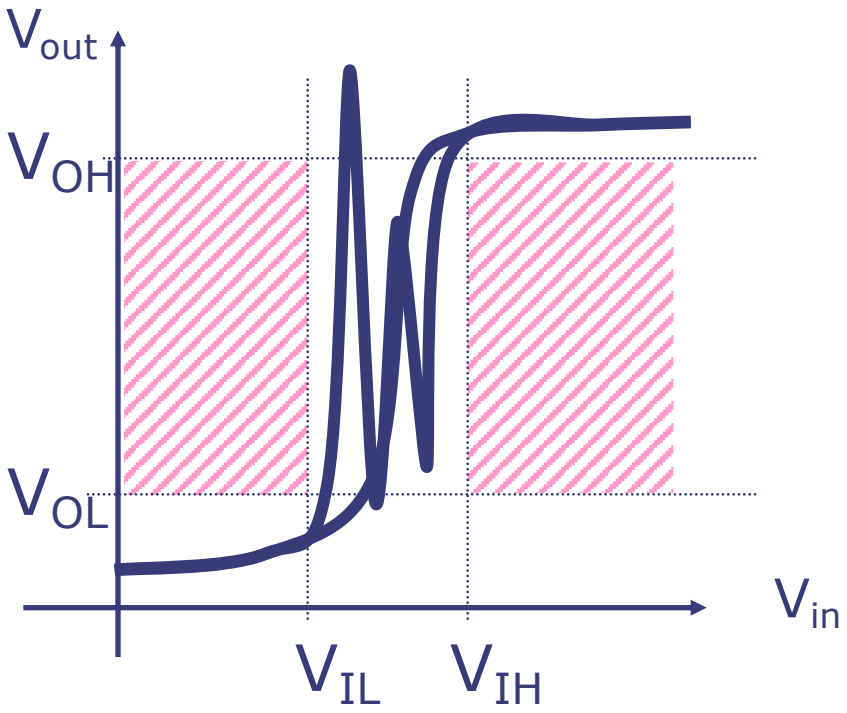


Voltage Transfer Characteristic (VTC): Plot of V_{out} vs. V_{in} where each measurement is taken after any transients have died out.

Note: VTC does not tell you anything about how fast a device is — it measures static behavior, not dynamic behavior.

VTC must avoid the shaded regions (aka "*forbidden zones*"), which correspond to *valid* inputs but *invalid* outputs.

Voltage Transfer Characteristic



1) Note the center white region is taller than it is wide (V_{OH}-V_{OL} > V_{IH}-V_{IL}). Net result: device must have GAIN > 1 and thus be ACTIVE

2) Note the VTC can do anything when $V_{IL} < V_{IN} < V_{IH}$

Digital Abstraction Problem

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification (V_{IL}, V_{IH}, V_{OL}, V_{OH}) that would allow this device to be a digital inverter?

$$V_{OL} < V_{IL} < V_{IH} < V_{OH}$$

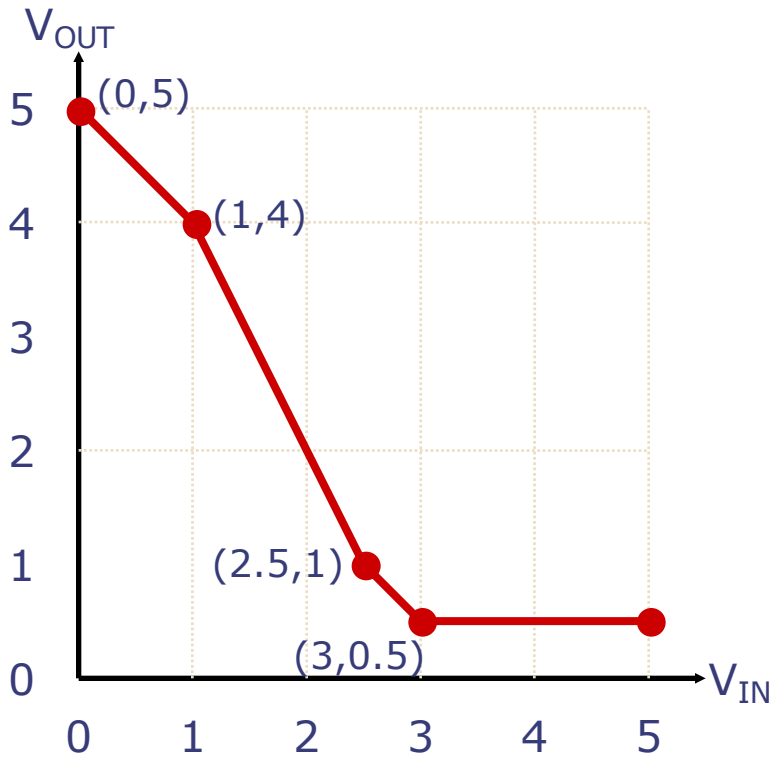
$V_{in} < V_{IL}$ ⇒ $V_{out} > V_{OH}$

$V_{IL} = 1$ $V_{OH} = 4$

$V_{in} > V_{IH}$ ⇒ $V_{out} < V_{OL}$

$V_{IH} = 3$ $V_{OL} = 0.5$

Low NM = 0.5 High NM = 1



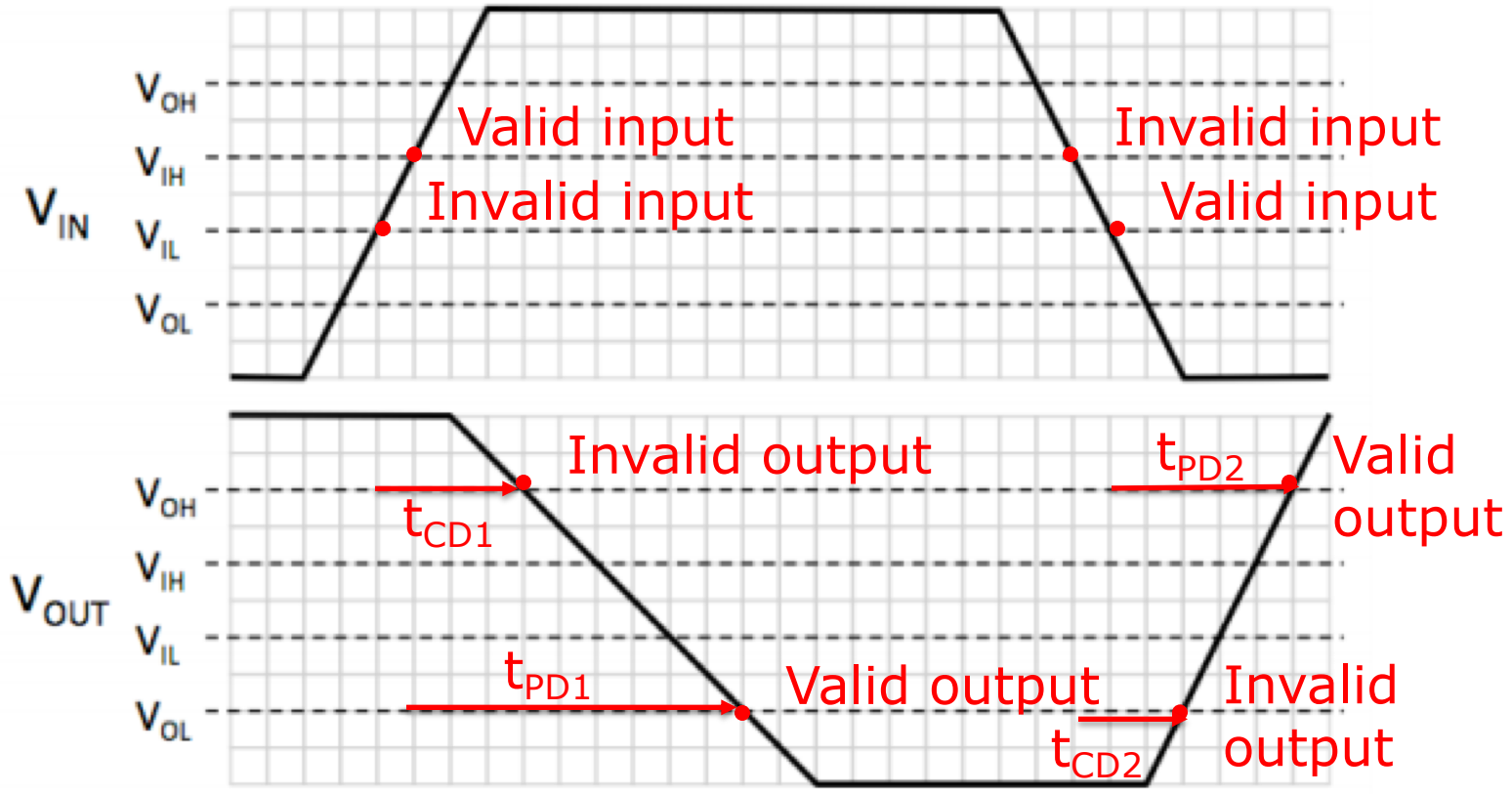
Sequential Timing

Combinational Propagation and Contamination Delays

- t_{PD}: Propagation delay measures the maximum time it takes for a gate to switch from one valid value to another.

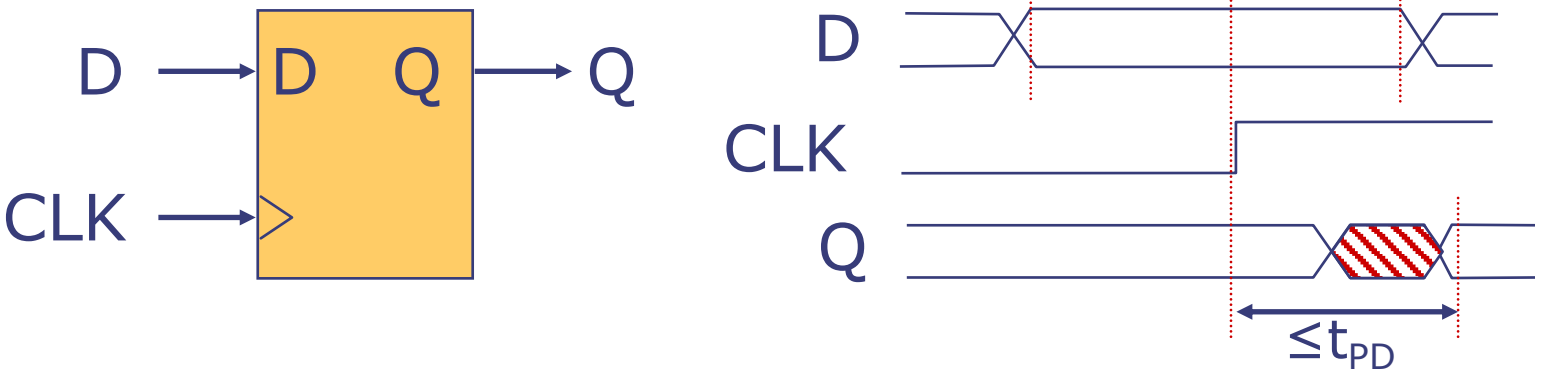
- t_{CD}: Contamination delay measures the minimum time that a gate will retain its previous valid value before becoming invalid

Inverter Timing Diagram



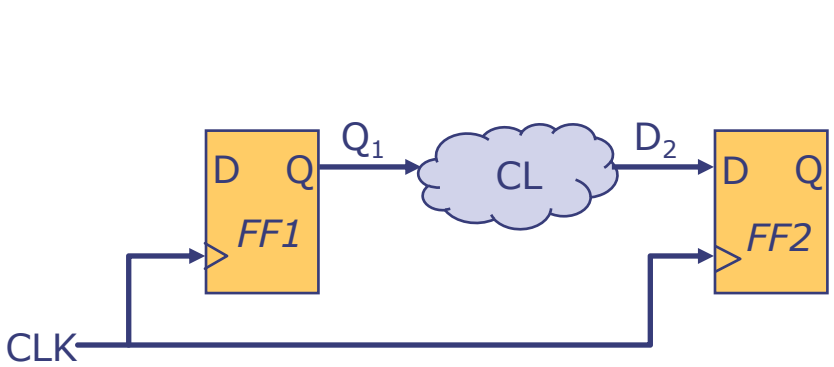
$t_{PD} = \max(t_{PD1}, t_{PD2})$ $t_{CD} = \min(t_{CD1}, t_{CD2})$

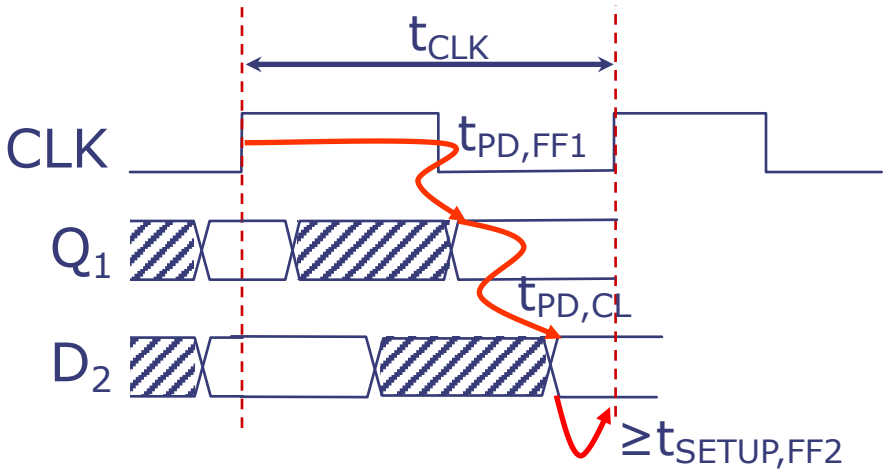
D Flip-Flop Timing



- Flip-flop input D should not change around the rising edge of the clock to avoid *metastability*
- Formally, D should be a stable and valid digital value:
  - For at least t_{SETUP} before the rising edge of the clock
  - For at least t_{HOLD} after the rising edge of the clock
- Flip-flop propagation delay t_{PD} is measured from rising edge of the clock to valid output (CLK→Q)

Meeting the Setup-Time Constraint



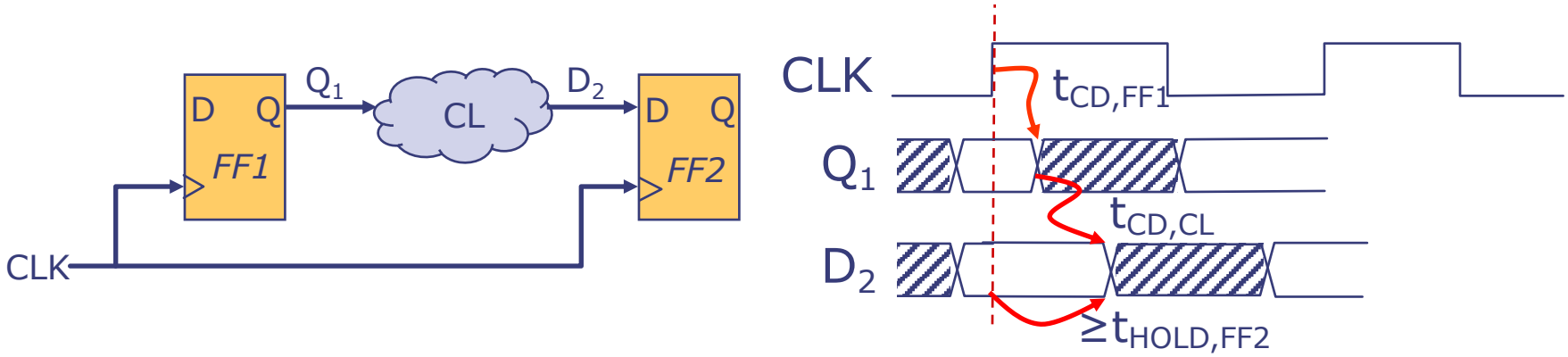


- To meet FF2's setup time,

$$t_{CLK} \geq t_{PD,FF1} + t_{PD,CL} + t_{SETUP,FF2}$$

- The slowest register-to-register path in the system determines the clock; Equivalently, a given register technology and clock limit the amount of combinational logic between registers

Meeting the Hold-Time Constraint



- Hold time (t_{HOLD}) constraint of FF2 may be violated if D_2 changes too quickly
- Propagation delay (t_{PD}), the upper bound on time from valid inputs to valid outputs, does not help us analyze hold time!
- *Contamination delay* (t_{CD}) is the lower bound on time from input transition to output transition
- To meet FF2's hold-time constraint

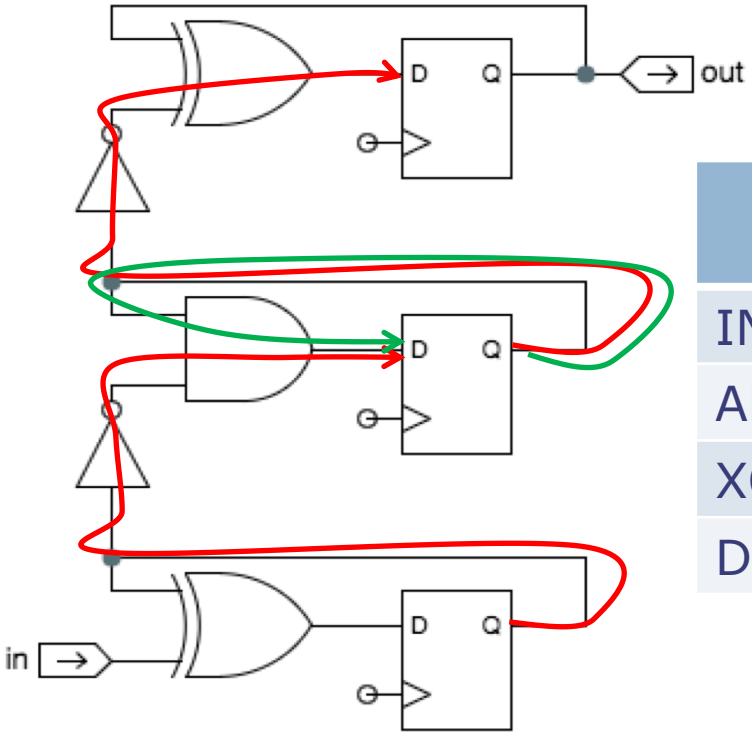
$$t_{CD,FF1} + t_{CD,CL} \geq t_{HOLD,FF2}$$

Tools may need to add logic to fast paths to meet t_{HOLD}

Clock speed

- How fast can a sequential circuit be clocked?
- Depends on two orthogonal factors:
  - Propagation Delay
    - The design of the flip-flop determines how fast it can change its state
    - The longest propagation delay of the combinational logic between any two registers limits how fast we can clock the circuit
  - Hold time
    - We can control the clock period in our designs, but we cannot control the hold time of our registers.

Sequential Timing Problem



	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
INV	20ps	100ps	--	--
AND	30ps	200ps	--	--
XOR	40ps	400ps	--	--
DREG	100ps	300ps	80ps	?ps

$$t_{CLK} \geq t_{PD,DREG} + t_{PD,INV} + t_{PD,XOR} + t_{SETUP,DREG} = 880 \text{ ps}$$

$$t_{HOLD,Reg} \leq t_{CD,DREG} + t_{CD,AND} = 130 \text{ ps}$$

Thank you!

Next lecture:
Cache Coherence