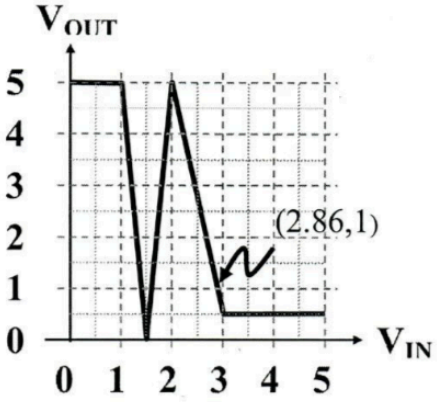
6.004 Spring 2019 Tutorial Problems
L24 – The Digital Abstraction and Sequential Timing Constraints

Problem 1.

Ms. Anna Logge, founder at a local MIT startup, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The figure on the right shows the voltage transfer curve of a proposed inverter for a new logic family (you can find spare copies below).

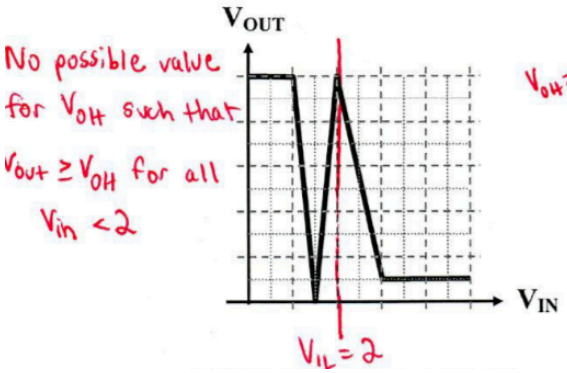


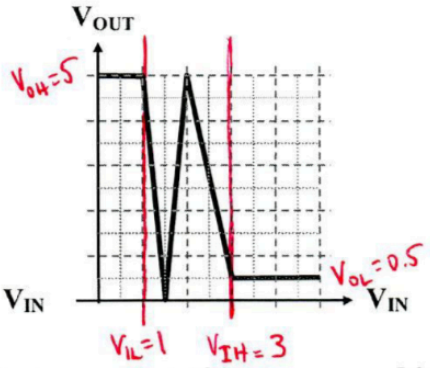
Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. **Noise Immunity (last row) is defined as the smaller of the two noise margins.**

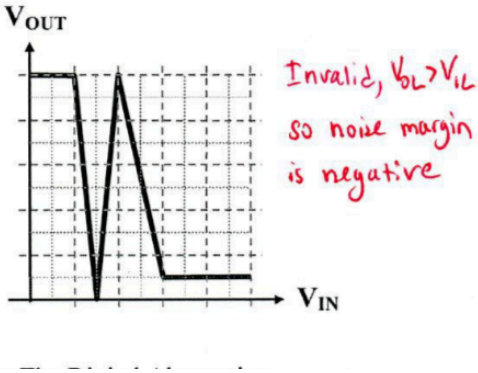
Complete the table by filling in missing entries. Choose each value to maximize the noise margins of the corresponding scheme. **If the numbers in a scheme can't be completed such that the device functions as an inverter with positive noise margins, fill the entries for that column with Xs.**

LNI's Possible Logic Mappings:

	Scheme A	Scheme B	Scheme C
V_{OL}	X	0.5	1
V_{IL}	2	1	0.5
V_{IH}	X	3	X
V_{OH}	X	5	X
Noise Immunity	X	0.5	X







Problem 2.

Suppose we define all signaling thresholds in our digital system to be relative to the supply voltage, V_{DD}:

- $V_{OL} = 0.1V_{DD}$
- $V_{IL} = 0.4V_{DD}$
- $V_{IH} = 0.6V_{DD}$
- $V_{OH} = 0.9V_{DD}$

$V_{DD,A} = 1V$

$V_{OL,A} = 0.1V$

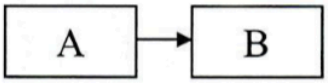
$V_{IL,A} = 0.4V$

$V_{IH,A} = 0.6V$

$V_{OH,A} = 0.9V$

We want to connect two types of digital devices, A and B, that use different supply voltages, $V_{DD,A}$ and $V_{DD,B}$. **Assume that $V_{DD,A} = 1V$.**

(1) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



Outputs of A must be valid inputs to B

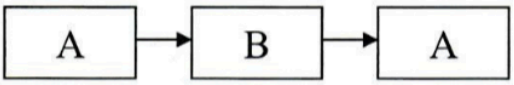
$V_{OL,A} \le V_{IL,B}$ $\quad$ $V_{OH,A} \ge V_{IH,B}$

$0.1 \le 0.4\,V_{DD,B}$ $\quad$ $0.9 \ge 0.6\,V_{DD,B}$

$0.25 \le V_{DD,B}$ $\quad$ $1.5 \ge V_{DD,B}$

$\boxed{0.25 \le V_{DD,B} \le 1.5}$

(2) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



Additional constraints: outputs of B are valid inputs to A

$V_{OL,B} \le V_{IL,A}$ $\quad$ $V_{OH,B} \ge V_{IH,A}$

$0.1V_{DD,B} \le 0.4$ $\quad$ $0.9\,V_{DD,B} \ge 0.6$

$V_{DD,B} \le 4$ (already satisfied) $\quad$ $V_{DD,B} \ge 2/3$

$\boxed{\frac{2}{3} \le V_{DD,B} \le 1.5}$

(3) For the same circuit as in part 2, under what range of supply voltages $V_{DD,B}$ will the system have noise margins of at least 0.1V?

$V_{OL,A} + 0.1 \le V_{IL,B}$ $\quad$ $V_{OH,A} - 0.1 \ge V_{IH,B}$

$0.5 \le V_{DD,B} \le 4/3$

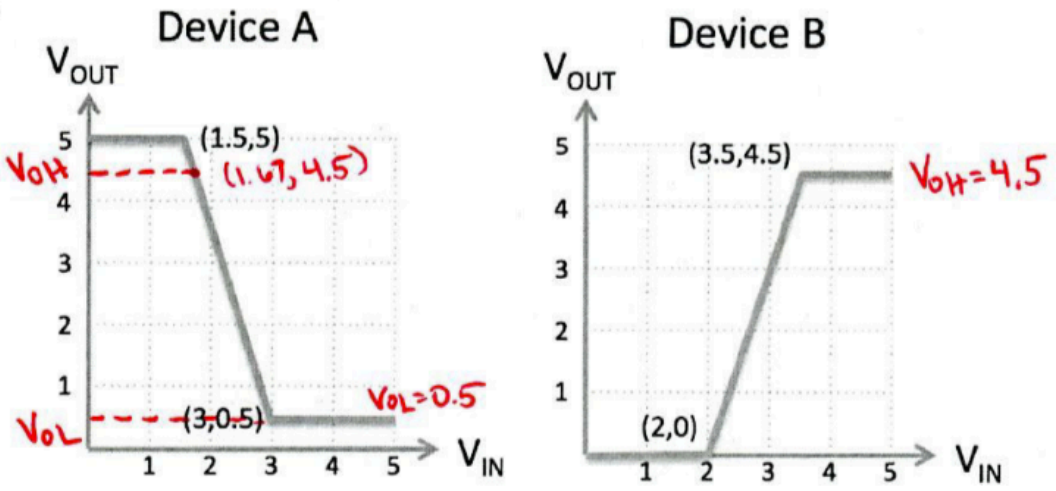
$V_{OL,B} + 0.1 \le V_{IL,A}$ $\quad$ $V_{OH,B} - 0.1 \ge V_{IH,A}$

$7/9 \le V_{DD,B} \le 3$

$\boxed{\frac{7}{9} \le V_{DD,B} \le \frac{4}{3}}$

Problem 3.

The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:



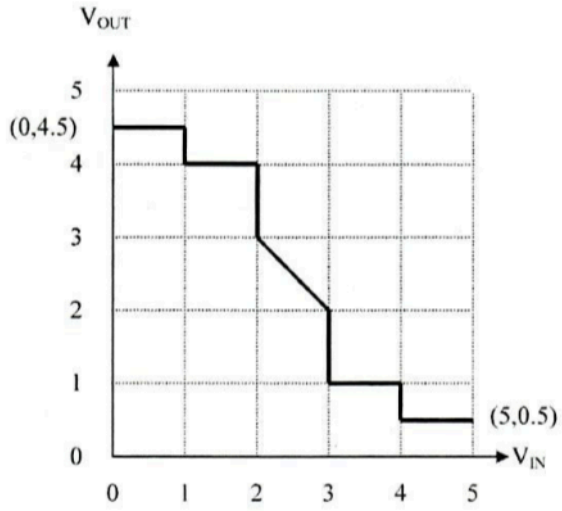
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize the noise immunity (i.e., the smaller of the two noise margins).

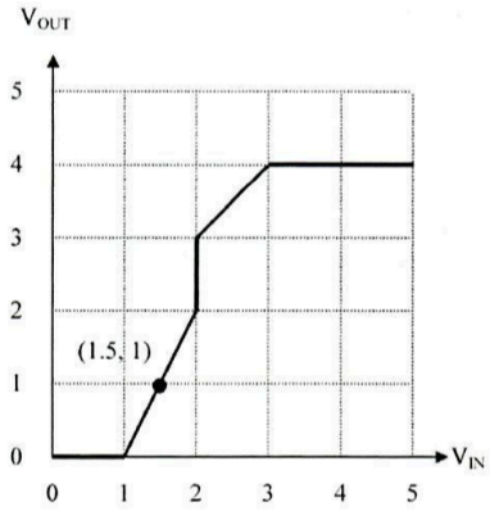
V_{OL} = 0.5 V_{IL} = 1.5 or 1.67 V_{IH} = 3.5 V_{OH} = 4.5

Low Noise Margin = 1 or 1.17 **High Noise Margin** = 1

Problem 4.

The following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:



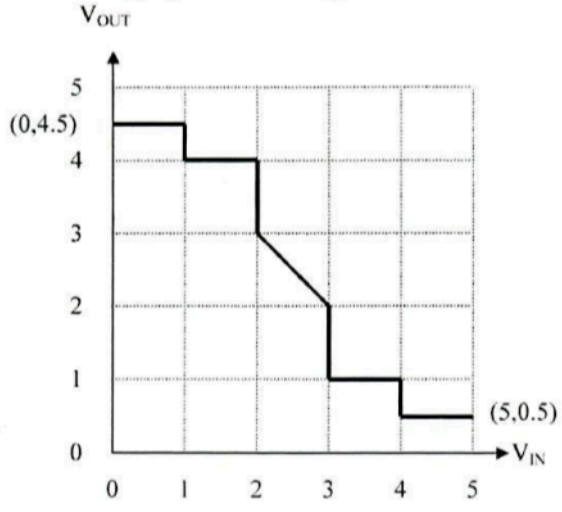


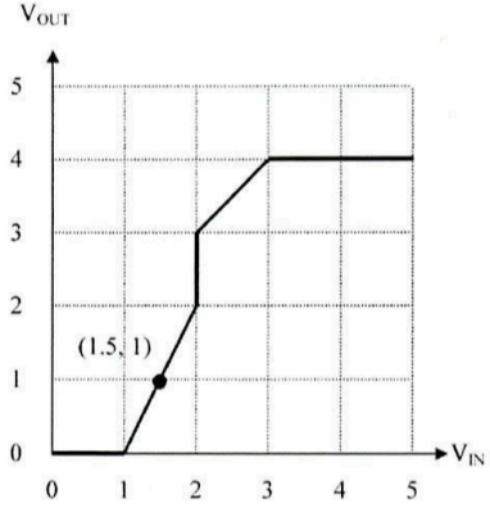
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

V_{OL} = 1 **V_{IL} =** 1.5 **V_{IH} =** 3 **V_{OH} =** 4

Low Noise Margin = 0.5 **High Noise Margin =** 1

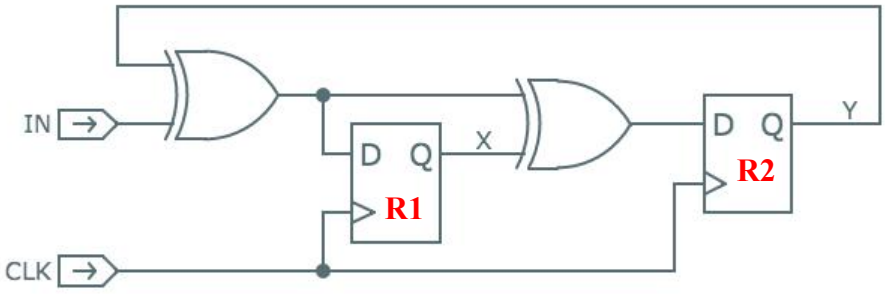
Scratch copy of the VTC diagrams:





Problem 5.

Consider the following sequential logic circuit. It consists of one input IN, a 2-bit register that stores the current state, and some combinational logic that determines the state (next value to load into the register) based on the current state and the input IN.



(A) Using the timing specifications shown below for the XOR and DREG components, determine the shortest clock period, t_{CLK}, that will allow the circuit to operate correctly or write NONE if no choice for t_{CLK} will allow the circuit to operate correctly and briefly explain why.

Component	t_{CD}	t_{PD}	t_{SETUP}	t_{HOLD}
XOR2	0.15ns	2.1ns	–	–
DREG	0.1ns	1.6ns	0.4ns	0.2ns

Minimum value for t_{CLK} (ns): 6.2
or explain why none exists

Longest path is from R2 -> R2 through two XOR gates.

$t_{CLK} >= t_{PD,REG} + 2 * t_{PD,XOR2} + t_{SETUP,REG} = 1.6 + 2 * 2.1 + 0.4 = 6.2$

(B) One of the engineers on the team suggests using a new, faster XOR2 gate with t_{CD} = 0.05ns and t_{PD} = 0.7ns. Determine a new minimum value for t_{CLK} or write NONE and explain why no such value exists.

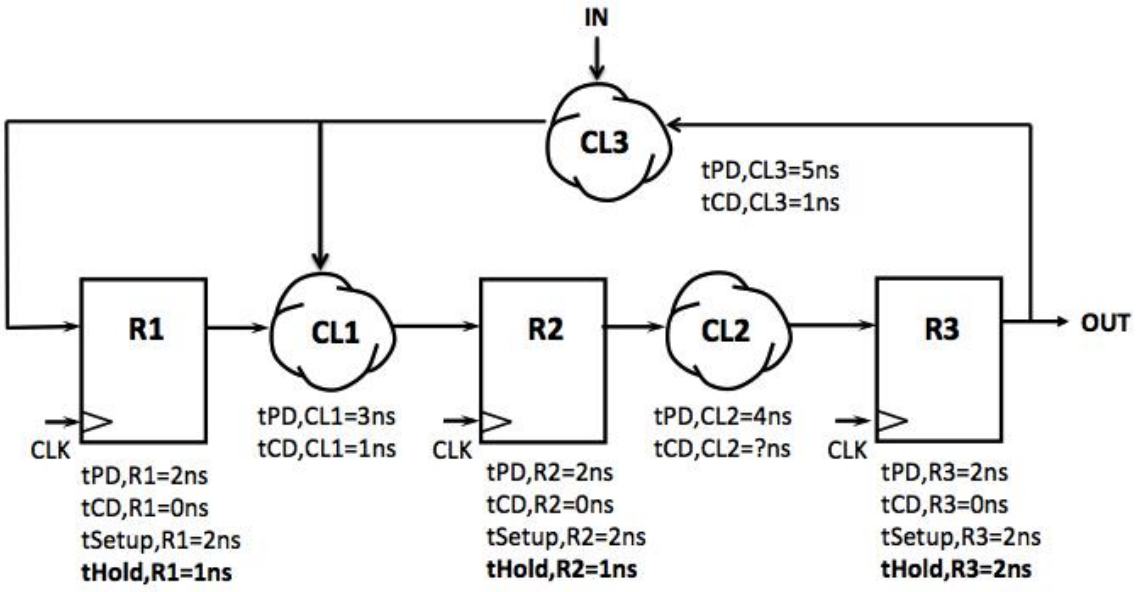
Minimum value for t_{CLK} (ns): NONE
or explain why none exists

Hold time constraint with old delays.
$t_{CD,REG} + t_{CD,XOR2} = 0.1 + 0.15 = 0.25 >= t_{HOLD,REG} = 0.2$

Hold time constraint does not hold with new delays.
$t_{CD,REG} + t_{CD,XOR2} = 0.1 + 0.05 = 0.15$ not $>= t_{HOLD,REG} = 0.2$

Problem 6.

Consider the following sequential logic circuit. It consists of three D registers, three different pieces of combinational logic (CL1, CL2, and CL3), one input IN, and one output OUT. The propagation delay, contamination delay, and setup time of the registers are all the same and are specified below each register. **The hold time for the registers is NOT the same** and is specified in bold below each register. The timing specification for each combinational logic block is shown below that logic.



(A) What is the smallest value for the t_{CD} of CL2 that will allow all the registers in the circuit to operate correctly?

Smallest value for t_{CD} of CL2 (ns): **2**

Check hold time constraint between R2 and R3

$t_{CD,R2} + t_{CD,CL2} >= t_{HOLD,R3}$ => $t_{CD,CL2} >= t_{HOLD,R3} - t_{CD,R2} = 2 - 0 = 2$

(B) What is the smallest value for the period of CLK (i.e., t_{CLK}) that will allow all the registers in the circuit to operate correctly?

$t_{PD} + t_{SETUP}$ on longest path R3 -> R2 **Smallest value for t_{CLK} (ns):** **12**

$t_{PD,R3} + t_{PD,CL3} + t_{PD,CL1} + t_{SETUP,R2} = 2 + 5 + 3 + 2 = 12$

(C) What are the propagation delay and contamination delay of the output, OUT, of this circuit relative to the rising edge of the clock?

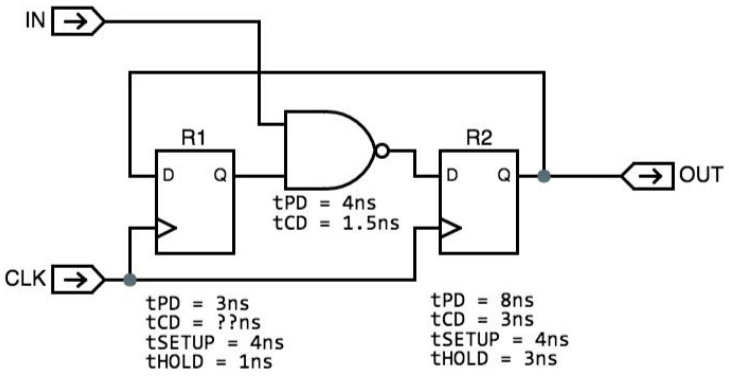
The delay measured from rising edge of the clock to OUT goes through R3

t_{PD} for OUT (ns): **$t_{PD,R3} = 2$**

t_{CD} for OUT (ns): **$t_{PD,R3} = 0$**

Problem 7.

Consider the following sequential logic circuit. The timing specifications are shown below each component. Note that the two registers do NOT have the same specifications.



(A) What is the smallest value for the period of CLK (i.e., tCLK) that will allow both registers in the circuit to operate correctly?

Smallest value for tCLK (ns): **12**

For R1->R2 $t_{CLK} >= t_{PD,R1} + t_{PD,NAND2} + t_{SETUP,R2} = 3 + 4 + 4 = 11$

For R2->R1 $t_{CLK} >= t_{PD,R2} + t_{SETUP,R1} = 8 + 4 = 12$

(B) What is the smallest value for the tCD of R1 that will allow both registers in the circuit to operate correctly?

Smallest value for tCD of R1 (ns): **1.5**

For R1->R2 $t_{CD,R1} + t_{CD,NAND2} >= t_{HOLD,R2} \Rightarrow t_{CD,R1} >= 3 - 1.5 = 1.5$

(C) Suppose two of these sequential circuits were connected in series, with the OUT signal of the first circuit connected to the IN signal of the second circuit. The same CLK signal is used for both circuits. Now what is the smallest value for the period of CLK (i.e., tCLK) that will allow both registers in the circuit to operate correctly?

Smallest value for tCLK (ns): **16**

For R2 -> R2_COPY $t_{CLK} >= t_{PD,R2} + t_{PD,NAND2} + t_{PD,R2\_COPY} = 8 + 4 + 4 = 16$