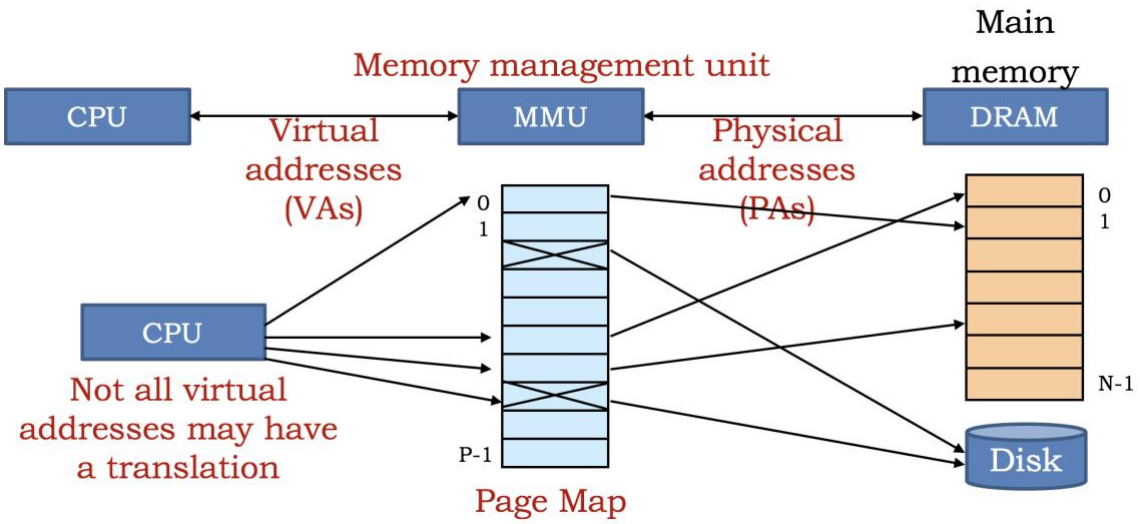
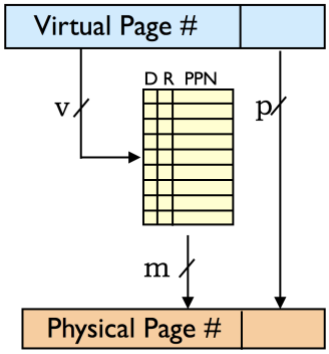
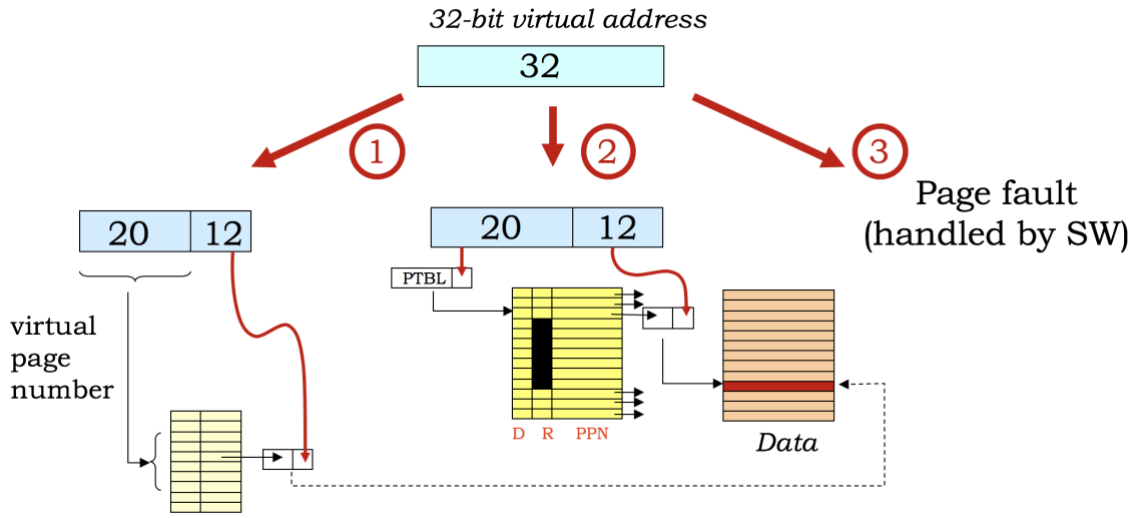
6.004 Tutorial Problems
L17 – Virtual Memory





(v + p)	bits in virtual address
(m + p)	bits in physical address
2_v	number of *virtual* pages
2_m	number of *physical* pages
2_p	bytes per physical page
2_{v+p}	bytes in virtual memory
2_{m+p}	bytes in physical memory
$(m+2)2_v$	bits in the page table



Look in TLB: VPN→PPN cache

Note: A subset of problems are marked with a red star (★). We especially encourage you to try these out before recitation.

Problem 1. ★

The micro-RISC has a 12-bit virtual address, an 11-bit physical address and uses a page size of 256 (= 2_8) bytes. The micro-RISC has been running for a while and at the current time the page table has the contents shown on the right. Assume all physical pages are currently in use.

VPN	*D*	*R*	*PPN*
0	0	1	2
1	—	0	—
2	0	1	4
3	—	0	—
4	1	1	0
5	1	1	1
6	—	0	—
7	—	0	—
8	—	0	—
9	—	0	—
A	—	0	—
B	—	0	—
C	1	1	7
D	1	1	6
LRU→E	1	1	5
F	0	1	3

(A) Assuming each page table entry contains the usual dirty (D) and resident (R) bits, what it is the total size of the page table in bits?

Size of page table (bits): _____

(B) The following load instruction, located at virtual address 0x0BC, is about to be executed.

```
lw x1, 0x2C8(x0)
```

When the instruction is executed, what main memory locations are accessed by the instruction fetch and then the memory access initiated by the LW? Use the page table shown to the right. Assume the LRU page is virtual page 0xE.

Physical address for instruction fetch: 0x_____

Physical addr for data read by LW instruction: 0x _____

(C) A few instructions later, the following instruction, located at virtual address 0x0CC, is executed:

```
sw x1, 0(x2)    // current value of X2 = SP = 0x600
```

Please mark up the page table to show its contents after the SW has been executed. Use the page table shown to the right. Assume the LRU page is virtual page 0xE.

Remember to show any changes to the dirty and resident control bits as well as updates to the physical page numbers. If an entry in the page table no longer matters, please indicate that by replacing it with "— 0 — " for the D, R and PPN entries.

Show updated contents of page table

Problem 2.

Consider a RISC-V processor that includes a 40-bit virtual address, an MMU that supports 4096 (2_{12}) bytes per page, 2_{32} bytes of physical memory, and a large Flash memory that serves as a disk. The MMU and the page fault handler implement an LRU replacement strategy.

Note that in the RISC-V processor we have been building in class, the word size is 32 bits. In order to support a 40-bit virtual address space, this problem is referring to a RISC-V processor that uses a larger (>= 40 bit) word size.

(A) What is the size of the page table for this processor? Assuming the page table includes the standard dirty and resident bits, specify the width of each page table entry in bits, and number of entries in the page table.

Size of page table entry in bits:_____

Number of entries in the page table:_____

(B) The following test program is running on this RISC-V processor. The first 8 locations of the page table, just before executing this test program, are shown below; the least-recently-used page ("LRU") and next least-recently-used page ("next LRU") are as indicated. This RISC-V processor also has a 4 element, fully associative, Translation Lookaside Buffer (TLB) that caches page table translations from VPN to PPN.

```
. = 0x0
lui x3, 2
lw x5, 0x600(x3)
lui x3, 4
sw x5, 0x100(x3)
```

TLB

	Tag (VPN)	*D*	*R*	*PPN*
LRU→	0x3	1	1	0x1
	0x2	0	1	0x3
	0x6	0	1	0x2
Next LRU→	0x1	0	1	0x5

Page Table

VPN	*D*	*R*	*PPN*
0	1	1	0x7
1	0	1	0x5
2	0	1	0x3
LRU→ 3	1	1	0x1
4	--	0	--
5	0	1	0x0
6	0	1	0x2
Next LRU→ 7	0	1	0x6

For each virtual page that is accessed by this program, specify the **VPN**, whether or not it results in a **TLB hit** on the first access to that page, whether or not it results in a **page fault**, and the **PPN** that the page ultimately maps to. *You may not need to use all rows of the table.*

VPN	**TLB Hit (Yes/No)**	**Page Fault (Yes/No)**	**PPN**

(C) Which physical pages, if any, need to be written to disk during the execution of the test program in part B?

Physical page numbers written to disk or NONE: _____

(D) What is the physical address of the LW instruction?

Physical address of LW instruction: 0x_____

Problem 3.

Consider a RISC-V processor that includes a 32-bit virtual address, an MMU that supports 4096 (2_{12}) bytes per page, 2_{24} bytes of physical memory, and a large Flash memory that serves as a disk. The MMU and the page fault handler implement an LRU replacement strategy.

(A) The designers are thinking about implementing the page table using a separate SRAM memory with L entries, where each entry has B bits. If the page table includes the standard dirty and resident bits, what are the appropriate values for the parameters L and B?

Appropriate value for the parameter L: _____

Appropriate value for the parameter B: _____

(B) If the designers decide to decrease the page size to 2048 (2_{11}) bytes but keep the same size virtual and physical addresses, what affect will the change have on the following architectural parameters? Use a letter "a" through "e" to indicate how the *new* value of the parameter compares to the *old* value of the parameter:

(a) doubled (b) increased by 1 (c) stays the same (d) decreased by 1 (e) halved

Size of page table entry in bits: _____

Number of entries in the page table: _____

Maximum percentage of virtual memory that can be resident at any given time: _____

(D) A test program has been running on the RISC-V with a page size of 2_{12} bytes and has been halted *just before* execution of the following instruction at location 0x1234. Assume the current contents of x2 are 0x3000.

```
sw x1, 0x4C8(x2)    | PC = 0x1234
```

The first 8 locations of the page table at the time execution was halted are shown to the right; the least-recently-used page ("LRU") and next least-recently-used page ("next LRU") are as indicated. Assume that all the pages in physical memory are in use. Execution resumes and the SW instruction is executed.

VPN	*D*	*R*	*PPN*
0	1	1	0x1
1	0	1	0x0
2	1	1	0x6
3	--	0	--
Next LRU→ 4	0	1	0x4
5	0	1	0x2
LRU→ 6	1	1	0x7
7	0	1	0x3

Please **show the contents of the page table** after the SW instruction has completed execution by crossing out any values that changed and writing in their new values. Note that the D and PPN fields for a non-resident page do not need to be specified.

(E) Which physical pages, if any, need to be written to disk during the execution of the SW instruction in part (D)?

Physical page numbers written to disk or NONE: _____

Problem 4. ★

Consider a virtual memory system that uses a single-level page table to translate virtual addresses into physical addresses. Each of the questions below asks you to consider what happens when **just ONE of the design parameters** (page size, virtual memory size, physical memory size) of the original system is changed. **Circle the correct answer.**

(A) If the physical memory size (in bytes) is **doubled**, the number of entries in the page table
(a) stays the same
(b) doubles
(c) is reduced by half
(d) increases by one
(e) decreases by one

(B) If the page size (in bytes) is **halved**, the number of entries in the page table
(a) stays the same
(b) doubles
(c) is reduced by half
(d) increases by one
(e) decreases by one

(C) If the virtual memory size (in bytes) is **doubled**, the number of bits in each entry of the page table
(a) stays the same
(b) doubles
(c) is reduced by half
(d) increases by one
(e) decreases by one

(D) If the page size (in bytes) is **doubled**, the number of bits in each entry of the page table
(a) stays the same
(b) doubles
(c) is reduced by half
(d) increases by one
(e) decreases by one

Consider a virtual memory system for a new processor with 4096 (2_{12}) virtual pages and 16384 (2_{14}) physical pages where each page contains 1024 (2_{10}) bytes. The first 8 entries of the current page table are shown below:

index	**D**	**R**	**PPN**
0	1	1	0x22
1	0	1	0x01
2	--	0	--
3	0	1	0x02
4	1	1	0x03
5	--	0	--
6	1	1	0x15
7	0	1	
…			

(E) What is the total number of bits in the page table?

Total number of bits in the page table: _____

(F) Which address bits from the CPU are used to choose an entry from the page table?

Address bits used to choose page table entry: A[_____ : _____]

(G) What is the physical address for the word at virtual location 0x1234? Write "not resident" if the location is not currently present in physical memory.

Physical address for byte at virtual address 0x1234 or "not resident": _____

(H) Briefly explain what action caused the D bit for page 6 to be 1.

Briefly explain.

Problem 5.

(A) A particular RISC-V implementation has 32-bit virtual addresses, 32-bit physical addresses and a page size of 2_{12} bytes. A test program has been running on this RISC-V and has been halted *just before* execution of the following instruction at location 0x1FFC. Assume x2 = 0x3000 and x3 = 0x6000 just prior to executing these instructions.

```
lw x1, 0x4C8(x2)    | PC = 0x1FFC
sw x1, 0x4(x3)      | PC = 0x2000
```

The first 8 locations of the page table at the time execution was halted are shown below; the least recently used page ("LRU") and next least recently used page ("next LRU") are as indicated. Assume that all the pages in physical memory are in use. Execution resumes and **both** the LW and SW instructions are executed.

Please **show the contents of the page table** after the SW instruction has completed execution by crossing out any values that changed and writing in their new values.

VPN	*D*	*R*	*PPN*
0	1	1	0x1
1	0	1	0x0
LRU→ 2	1	1	0x6
3	--	0	--
Next LRU→ 4	0	1	0x4
5	0	1	0x2
6	0	1	0x7
7	0	1	0x3

(B) Which physical pages, if any, needed to be written to disk during the execution of the LW and SW instructions?

Physical page numbers written to disk or NONE: _____

(C) Please give the 32-bit physical memory addresses used for the four memory accesses associated with the execution of the LW and SW instruction.

32-bit physical memory address of LW instruction: 0x_____

32-bit physical memory address of data read by LW: 0x_____

32-bit physical memory address of SW instruction: 0x_____

32-bit physical memory address of data written by SW: 0x_____

Problem 6. ★

Consider a system with 40-bit virtual addresses, 36-bit physical addresses, and 64 KB (2_{16} bytes) pages. The system uses a page table to translate virtual addresses to physical addresses; each page table entry include dirty (D) and resident (R) bits.

Note that in the RISC-V processor we have been building in class, the word size is 32 bits. In order to support a 40-bit virtual address space, this problem is referring to a processor that uses a larger (>= 40 bit) word size.

(A) (2 points) Assuming a flat page table, what is the size of each page table entry, and how many entries does the page table have?

Size of page table entry in bits: _____

Number of entries in the page table: _____

(B) (1 point) If you changed the system to use 16 KB (2_{14} bytes) pages instead of 64 KB pages, how would the number of entries in the page table change? Please give the ratio of the new size to the old size.

(# entries with 16 KB pages) / (# entries with 64 KB pages): _____

Assume 64 KB pages for the rest of this exercise.

(C) (6 points) The contents of the page table and TLB are shown to the right. The page table uses an LRU replacement policy, and the LRU page (shown below) will be chosen for replacement. For each of these four accesses, compute its corresponding physical address and indicate whether the access causes a TLB miss and/or a page fault. **Assume each access starts with the TLB and Page Table state shown to the right.**

TLB

VPN (tag)	V	D	PPN
0x0	1	0	0xBE7A
0x3	0	0	0x7
0x5	1	1	0xFF
0x2	1	0	0x900

Fill in table below

	Virt Addr	PPN (in hex)	Phys Addr (in hex)	TLB Miss?	Page Fault?
1.	**0x06004**	_____	_____	**Y / N**	**Y / N**
2.	**0x30286**	_____	_____	**Y / N**	**Y / N**
3.	**0x68030**	_____	_____	**Y / N**	**Y / N**
4.	**0x4BEEF**	_____	_____	**Y / N**	**Y / N**

Page Table

VPN	R	D	PPN	
0	1	0	0xBE7A	
1	0	0	---	
2	1	0	0x900	
3	1	0	0x8	← **LRU PAGE**
4	0	0	---	
5	1	1	0xFF	
6	1	0	0x70	

...