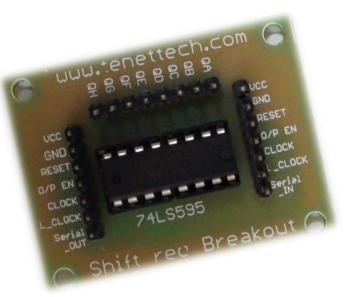


# Tenet's 74HC595 Shift registerbreakout



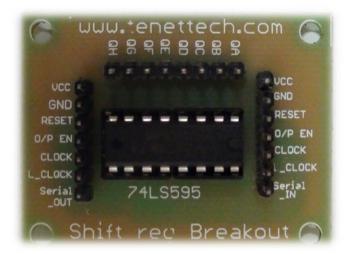


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### Introduction

The 'HC595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.



### **Features**

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max ICC
- Typical tpd = 13 ns

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- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Shift Register Has Direct Clear

## **Applications**

- Network Switches
- Power Infrastructure
- LED Displays
- Servers

## **Specifications**

### **Absolute Maximum Ratings**

Parameters	Specs.		
Supply voltage range, VCC	-0.5 V to 7 V		
Input clamp current, IIK (VI < 0 or VI > VCC)	±20 mA		
Output clamp current, IOK (VO < 0 or VO > VCC)	±20 mA		
Continuous output current, IO (VO = 0 to VCC)	±35 mA		
Continuous current through VCC or GND	±70 mA		
Storage temperature range, Tstg	-65°C to 150°C		

# **Recommended operating conditions**

Symbol	Parameters		Min.	Typ.	Max.	Unit
VCC	Supply voltage		2	5	6	V
VIH	High-level input	VCC = 2 V	1.5			V
	voltage	VCC = 4.5 V	3.15			
		VCC = 6 V	4.2			
VIL	Low-level input	VCC = 2 V			0.5	V
	voltage	VCC = 4.5 V			1.35	

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		VCC = 6 V		1.8	
VI	Input voltage		0	VCC	V
VO	Output voltage		0	VCC	V
Δt/Δv‡	Input transition	VCC = 2 V		1000	ns
	rise/fall time	VCC = 4.5 V		500	
		VCC = 6 V		400	
TA	Operating free-air		-40	85	°C
	temperature				