EIE2810 Digital Systems Design Laboratory

Laboratory Report #5

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Introduction

This laboratory consists of 3 experiments, they are:

- Experiment A: Construct a word generator with 4 D-type flip-flops.
- Experiment B: Construct a counter with a 7-segment display based on the word generator in experiment A.
- Experiment C: Construct a responder with 4 D-type flip-flops.

1. Experiment A

1.1 Design

According to the truth table of 74HC74, to construct a 4-channel word generator, the set pin and reset pin are connected to two SIMs respectively, while the rest of the set pins and reset pins are connected to V_{CC}, the clock pin of the first D-type flip-flop is connected to the signal generator, the $\overline{Q}$ pin is connected to the D pin, and the Q pin is connected to the clock pin of next D-type flip-flop. The designed circuit is shown in Figure 1. We need to note that in Figure 1, all of the ~PR pins are $\overline{SD}$ pins and all of the ~CLR pins are $\overline{RD}$ pins in the real experiments.

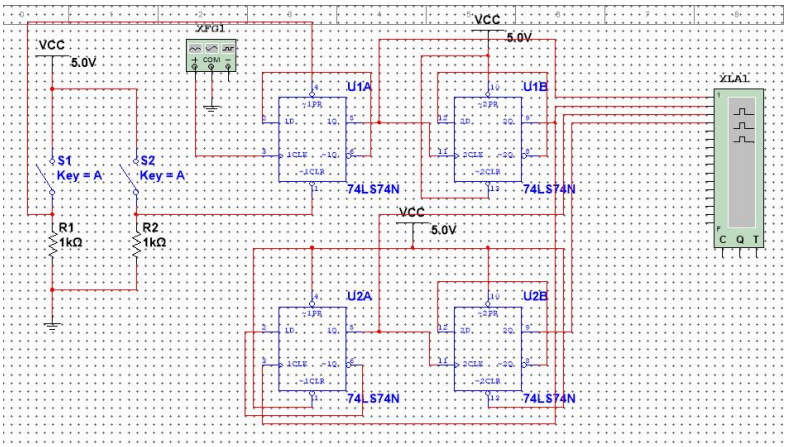

Figure 1 The Designed Circuit of the 4-Channel Word Generator

1.2 Results

The signal received by the logic analyzer is shown in Figure 2, Figure 3, Figure 4, and Figure 5. We need to note that the SIM activation situations of these four figures are different. The clock signal is a square wave with a 2 HZ frequency, the low-level voltage being 0V and the high-level voltage being 5V.

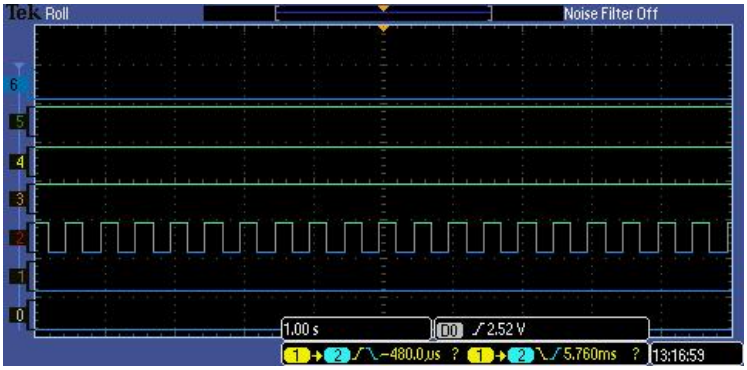

Figure 2 The Signal Received by the Logic Analyzer When Both 2 SIMs are Open

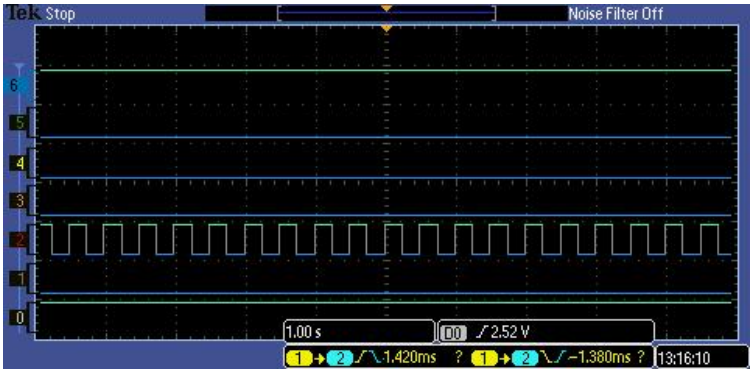

Figure 3 The Signal Received by the Logic Analyzer When Only One of the SIMs is Open

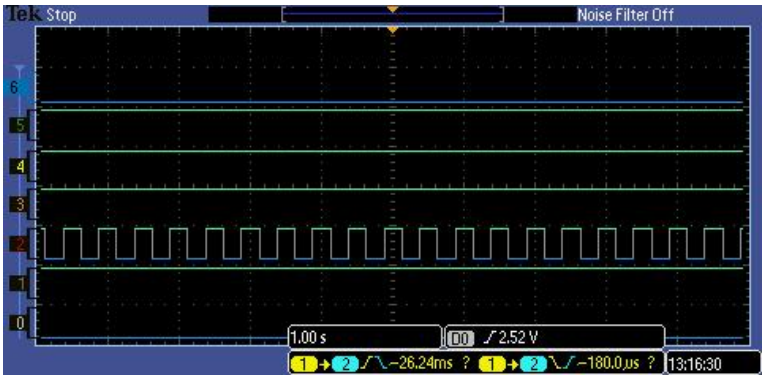

Figure 4 The Signal Received by the Logic Analyzer When Another SIM is Open

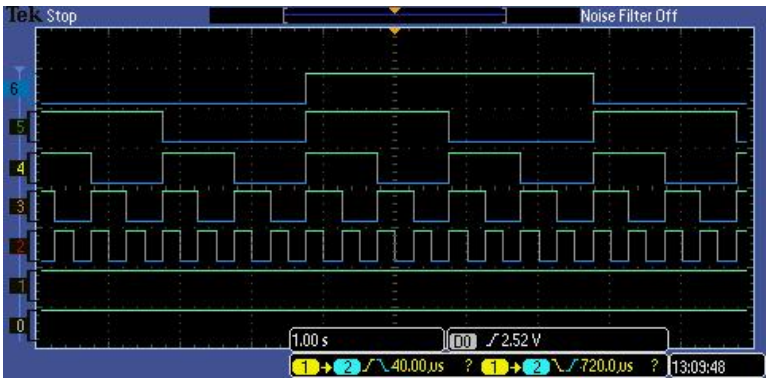

Figure 5 The Signal Received by the Logic Analyzer When Both 2 SIMs are Close

As shown in Figure 2 to Figure 5, line 0 is the reset signal while line 1 is the set signal, line 2 is the clock signal, and lines 3 to line 5 are the Q signal provided by 4 flip-flops respectively. As shown in Figure 5, when both 2 of the SIMs are close, the four Q signals construct a 4-channel word generator signal. This means we successfully constructed a 4-channel word generator with 4 D-type flip-flops.

2. Experiment B

2.1 Design

2.1.1 The Design of the Down Counter

To construct a down counter, we directly connect four Q outputs of the word generator constructed in experiment A to the 4 inputs of 74HC47 IC. The designed circuit for the down counter is shown in Figure 6. We need to note that in Figure 6, all of the ~PR pins are $\overline{SD}$ pins and all of the ~CLR pins are $\overline{RD}$ pins in the real experiments.

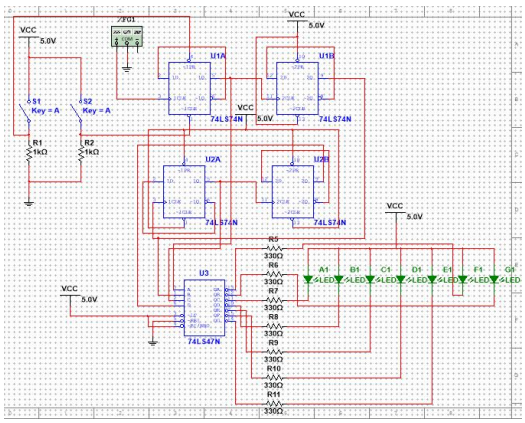

Figure 6 The Designed Circuit of the Down Counter

2.1.2 The Design of the Up Counter

To realize the up counter, we only need to connect four $\overline{Q}$ outputs of the word generator constructed in experiment A to the 4 inputs of 74HC47 IC. To realize the function of returning to 0 from 9, a NAND Gate is added to the circuit. Treat the $\overline{Q}$ output of the second and fourth flip-flop as the input of the NAND Gate, connect the output of the NAND Gate to four $\overline{SD}$ pins, and connect four $\overline{RD}$ pins to V_{CC}, the designed circuit for the up counter is shown in Figure 7. We need to note that in Figure 7, all of the ~PR pins are $\overline{SD}$ pins and all of the ~CLR pins are $\overline{RD}$ pins in the real experiments.

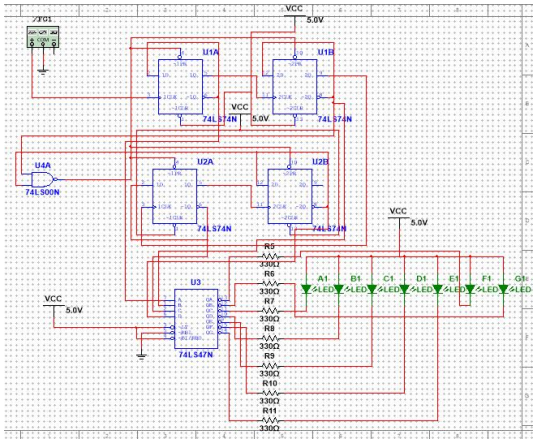

Figure 7 The Designed Circuit for the Up Counter

The mechanism for the returning is that when the BCD code provided by the word generator hasn't reached 1010_2, the NAND Gate will always provide a "1" logic to support the flip-flop process, when the BCD code reaches 1010_2, the NAND Gate will provide a 0, with all reset pins are connected to V_{CC}, all of the flip-flops are at set state. This makes the BCD code goes back to 0000_2 and starts up-counting again.

2.2 Results

2.2.1 The Results of the Down Counter

The results of the down counter are shown in Figure 8.

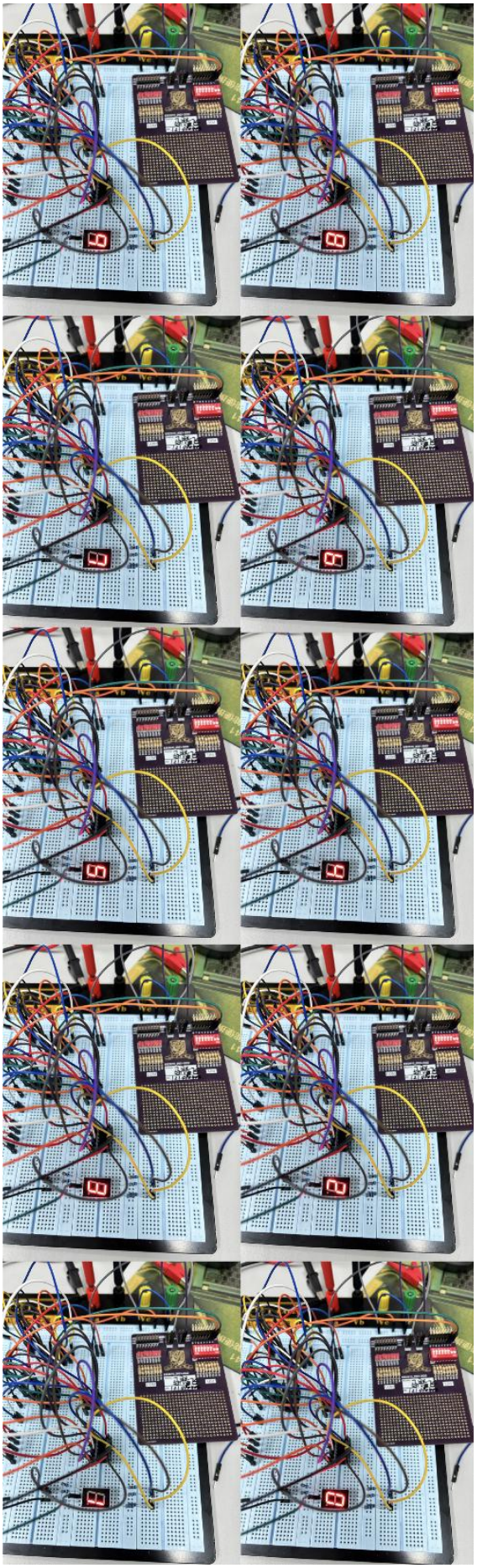

Figure 8 The Results of the Down Counter

As shown in Figure 8, the 7-segment display decrease from 9 to 0. There exists an error code after it displays 0 but the figure is not included. The error code occurs because the word generator will not go back to 0000_2 directly until it reaches 1111_2. When the 7-segment display cannot show a number bigger than 1001_2, then the error codes appear. All of the empirical results go well with the analyses, which means we successfully constructed a down counter.

2.2.2 The Results of the Up Counter

The results of the up counter are shown in Figure 9.

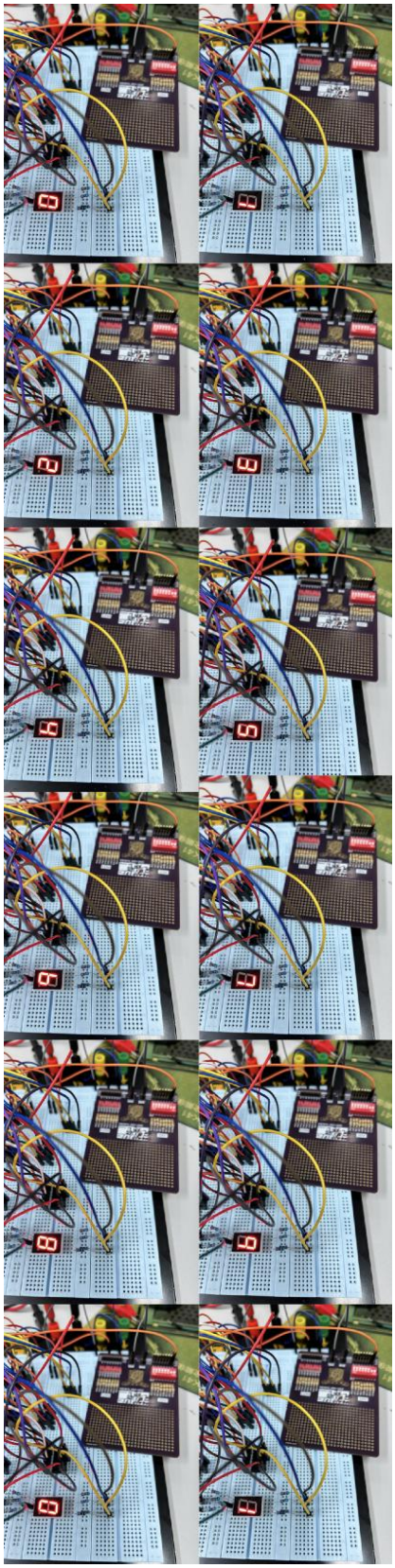

Figure 9 The Results of the up Counter

As shown in Figure 9, the 7-segment display increase from 0 to 9 and back to 0. The error codes in the down counter are eliminated in this up counter successfully. All of

the empirical results go well with the theoretical analyses, which means we successfully constructed an up counter and eliminated the error codes.

2.3 Questions

2.3.1 The 0 to 8 up Counter

To construct a 0 to 8 up counter and make it able to go back to 0 from 8, first connect the input of the decoder to the $\overline{Q}$ pins of the four flip-flops in order. Then connect all reset pins to V_{CC} and the $\overline{Q}$ pins of the MSB pin and LSB to the input of a NAND Gate. Connect the output of the NAND Gate to all of the set pins so that as long as the word generator reaches 1001_2, it will be set and start from 0000_2.

2.3.2 The Least Number of Basic Gates

Just as we have done in the experiment, the least number of basic gates is 1.

3. Experiment C

3.1 Design

To construct the responder system with an encoder, we connected the 4 outputs of the given circuit diagram to the 1 to 4 input pins of the encoder, connect the rest of the input pins of the encoder to V_{CC}, the 3 outputs of the encoder to the LSB, second LSB, second MSB input pins of the decoder, respectively. Lastly, connect the outputs of the decoder to the 7-segment display. The designed circuit for the responder is shown in Figure 10. We need to note that in Figure 10, all of the ~PR pins are $\overline{SD}$ pins and all of the ~CLR pins are $\overline{RD}$ pins in the real experiments.

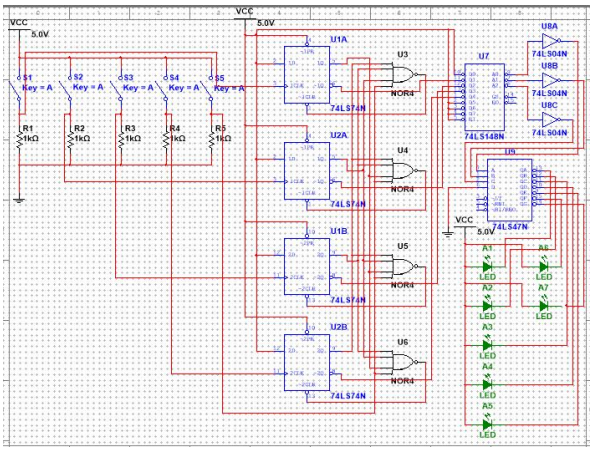

Figure 10 The Designed Circuit for the Responder

3.2 Results

The finished circuit for the responder system is shown in Figure 11.

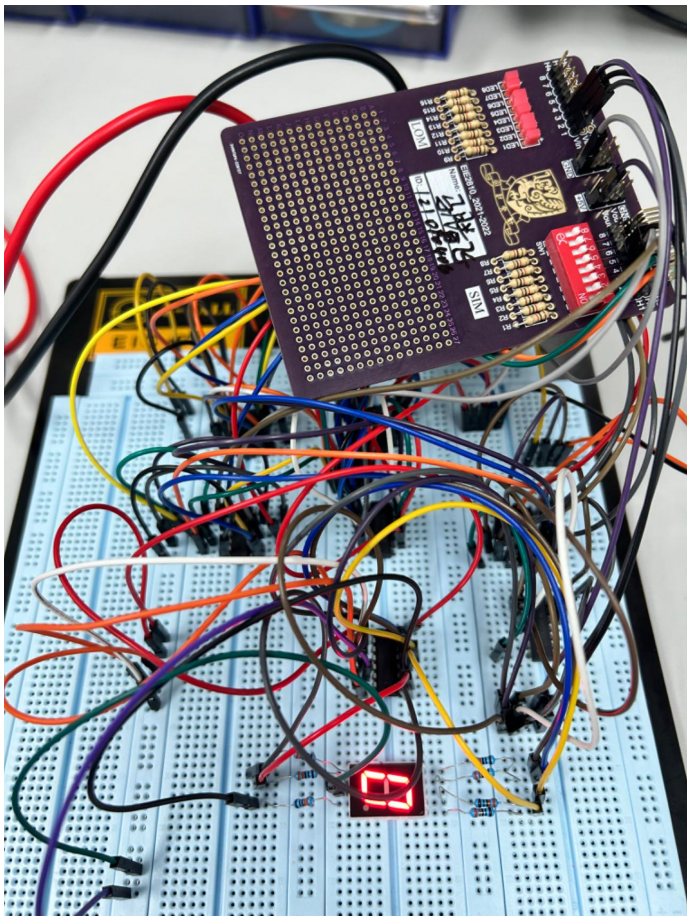

Figure 11 The Finished Circuit for the Responder System

The testing results for the responder system are shown in Figure 12, Figure 13, Figure 14, and Figure 15.

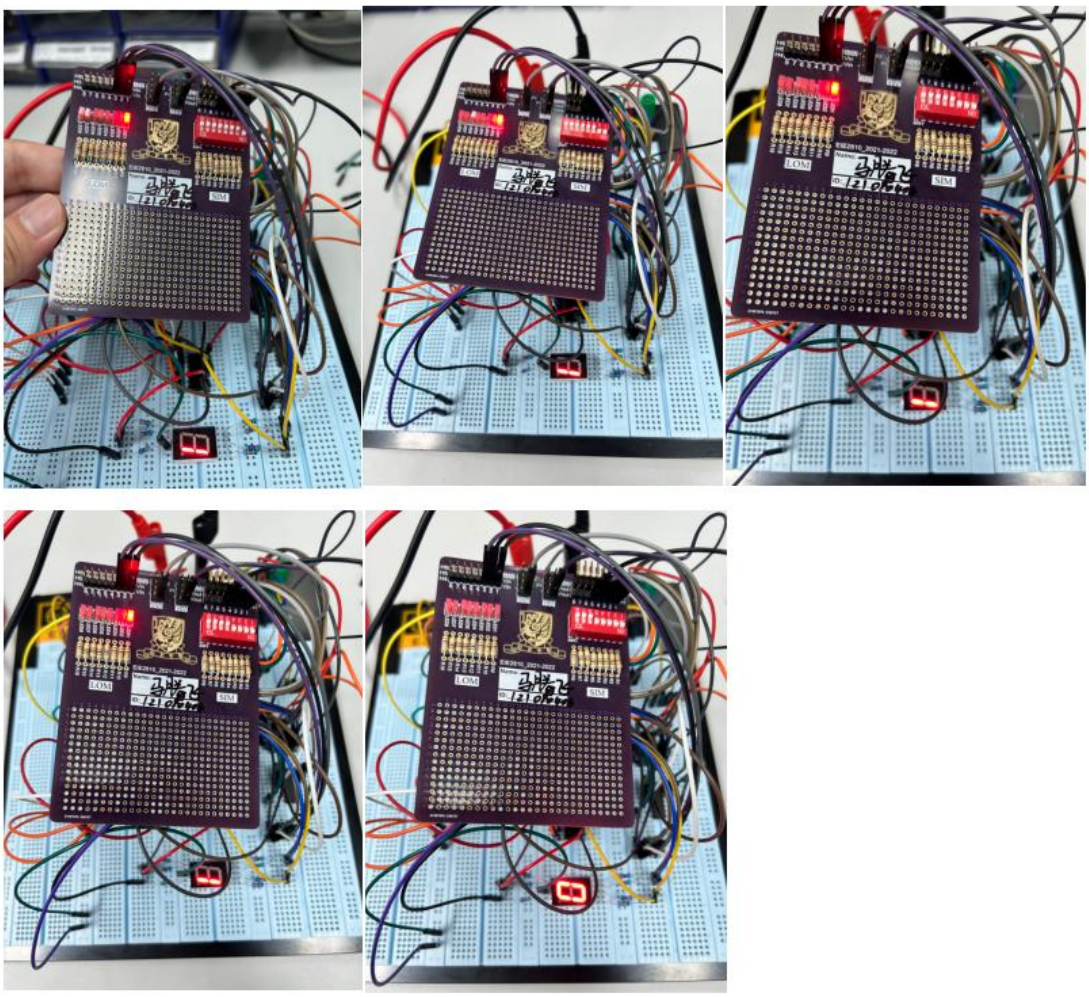

Figure 12 The Behavior of the Responder System When Player 1 First Press the Button

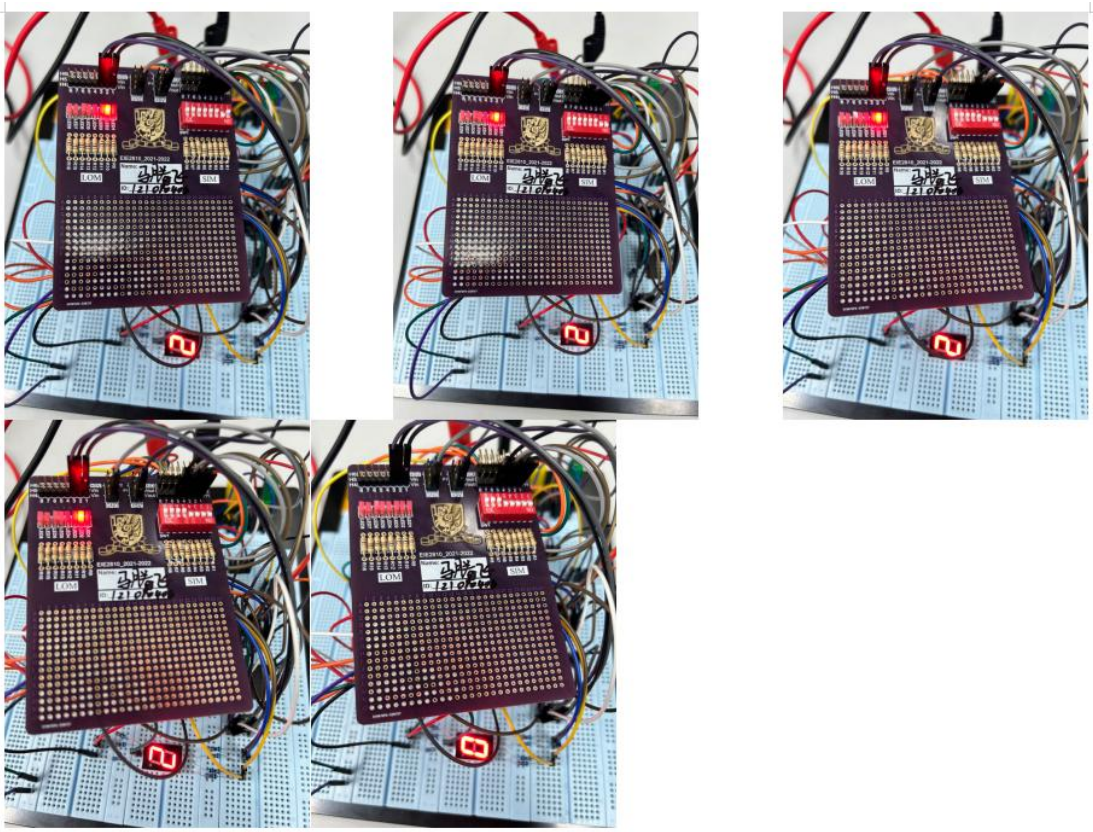

Figure 13 The Behavior of the Responder System When Player 2 First Press the Button

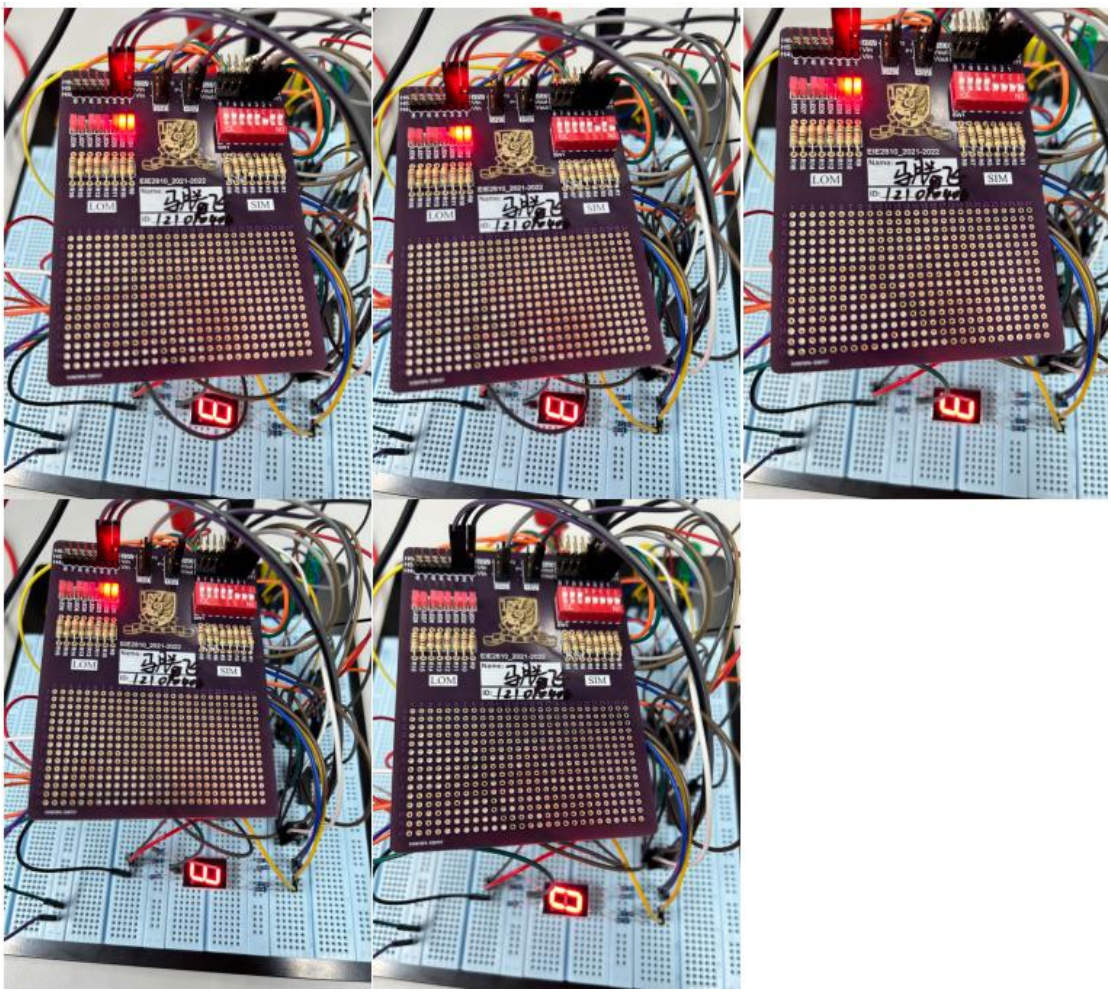

Figure 14 The Behavior of the Responder System When Player 3 First Press the Button

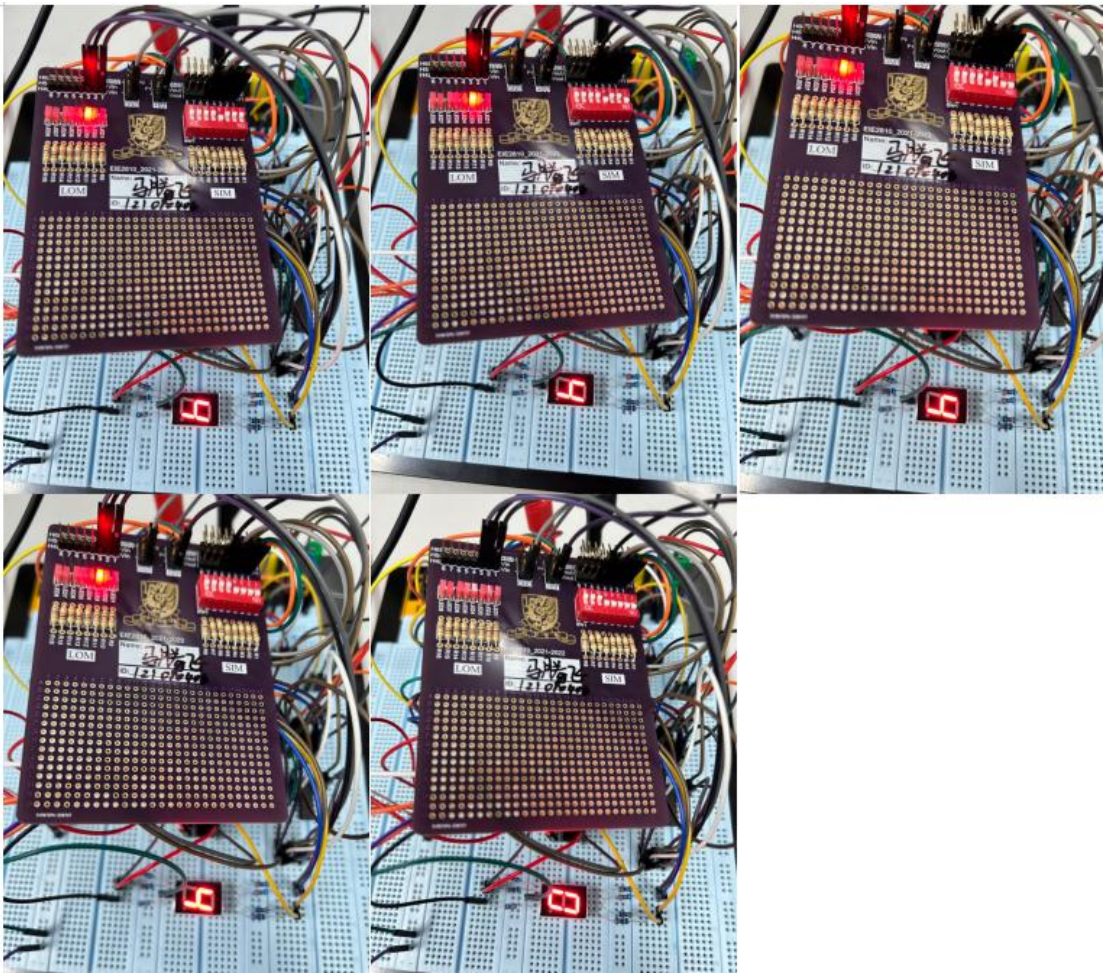

Figure 15 The Behavior of the Responder System When Player 4 First Press the Button

As shown in Figure 12, Figure 13, Figure 14, and Figure 15, no matter which player first presses the button, those who press the button later cannot change the display of the 7-segment display and the LOM until the judge resets the whole system. All of the empirical results go well with the requirements, which means we successfully constructed the responder system with an encoder.

3.3 Questions

According to the truth table of the IC 74HC47, when $\overline{RBI}$ is low and A_3, A_2, A_1, and A_0 are all low, it will output all high-level voltage so that there will have no display on the 7-segment display, and when A_3, A_2, A_1, and A_0 are not all low, no matter what state $\overline{RBI}$ is, the output will operate normally so that there will exist display. So, when the judge reset the system, A_3, A_2, A_1, and A_0 are all low, so, we only need to connect $\overline{RBI}$ to the ground to satisfy this requirement.

4. Conclusions

In this lab, we constructed a word generator with 4 flip-flops, constructed the down counter and up counter with a 7-segment display, and constructed a responder system with an encoder. From the lab, we know:

1) The inner logic of the word generator and the way to construct a word generator.

2) The inner logic of the counter and the way to use a word generator to construct a counter

3) The way to reset the system when the system goes to a certain condition

4) The inner logic and principle