EIE2810 Digital Systems Design Laboratory

# Laboratory 5

# Flip-flop, Counter, Encoder

School of Science and Engineering
The Chinese University of Hong Kong, Shenzhen

2024, Spring term

## 1. Objectives

In the Laboratory 5, we will spend the 2-week session on the following:

- Learn to use D flip-flop to upgrade a function generator to a word generator.
- Learn to design a looped counter by D flip-flop.
- Learn to design a responder module based on D flip-flop.
- Learn to use an 8-3 line encoder, and integrate it with the responder module and 7-segment module into a responder system.

## 2. Introduction

2.1 D Flip-flop

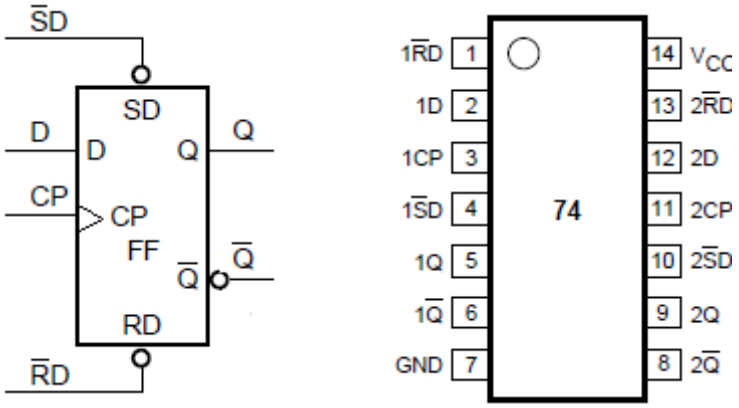
74HC74 is a dual D-type flip-flop with set and reset. Its function tables are shown as below. "X" means "Don't care". Vcc can be set as 5 V.

Table 1. Function tables of D flip-flop

| INPUT | | | | OUTPUT | |
|---|---|---|---|---|---|
| $\overline{SD}$ | $\overline{RD}$ | CP | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |

| INPUT | | | | OUTPUT | |
|---|---|---|---|---|---|
| $\overline{SD}$ | $\overline{RD}$ | CP | D | Qn+1 | $\overline{Q}$n+1 |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

The logic symbol and pin arrangement are shown as below.




(a) Logic symbol (b) pin arrangement

Fig. 1 74HC74 logic symbol and pin arrangement

- When $\overline{SD}$ and $\overline{RD}$ are set as high, at the rising edge of CP, the state of D will be transferred to become the next state of Q, and $\overline{Q}$ will also be updated to the opposite of Q.
- When $\overline{SD}$ is low and $\overline{RD}$ is high, Q become high and $\overline{Q}$ is low. This is state-set.
- When $\overline{SD}$ is high and $\overline{RD}$ is low, Q become low and $\overline{Q}$ is high. This is state-reset.
- When $\overline{SD}$ and $\overline{RD}$ are both low, Q and $\overline{Q}$ are both high.

With this D-type flip-flop and some basic gates, we will design a number of interesting and useful systems in this lab.

## 2.2 8-3 Line Priority Encoder

74HC148 is an 8-3 line priority encoder, which will encode the input from 8 lines into a 3-bit signal. The pin arrangement and truth table are illustrated as below. Vcc can be set as 5 V.

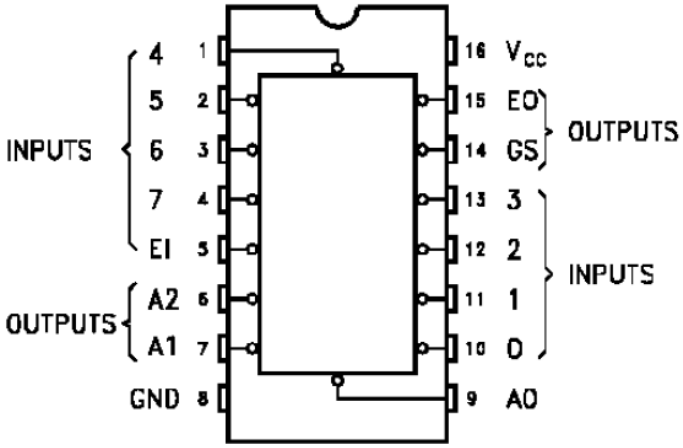



Fig. 2 Pin arrangement of 74HC148

Table 2. Truth table of 74HC148

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E1 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A2 | A1 | A0 | GS | E0 |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | L | H | L | H |
| L | X | X | X | X | X | L | H | H | L | H | L | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | H | L | L | L | H |
| L | X | X | L | H | H | H | H | H | H | L | H | L | H |
| L | X | L | H | H | H | H | H | H | H | H | L | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | L | H |

A7 have highest priority. When it is low, the encoder output will be 0x000.
Try to understand the truth table. It will be used in the experiment on responder.

Pay attention to the case when E1 is low, A0-A7 are all high, indicating that no input line has a valid signal, the E0 is low. Otherwise, E0 is high.

2.3 Other ICs needed in the lab

Here are some other ICs to be used in the lab.

(1) 4002. This is a chip with two 4-input NOR gates. The pin arrangement is as below. Vss is ground. $V_{DD}$ can be set as 5V.

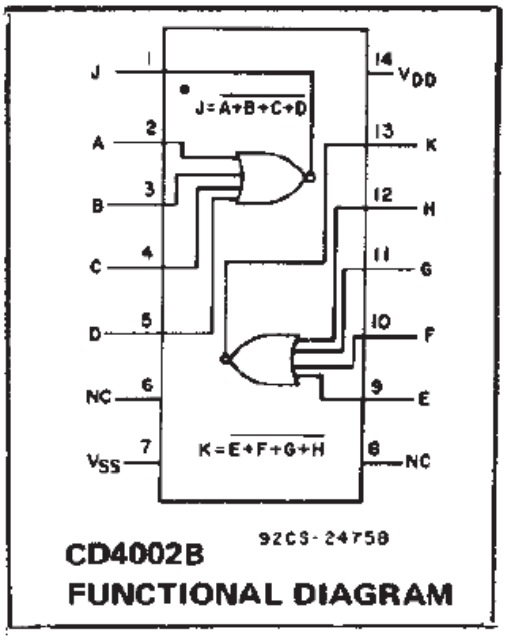



Fig. 3 Pin arrangement of 4002

(2) 74HC47 and 7-Segment Display
We will use this BCD-7segment decoder and a 7 segment display again in this experiment to show the result to the 7-segment display. The pin arrangements and truth table are shown below for your convenience in the design.

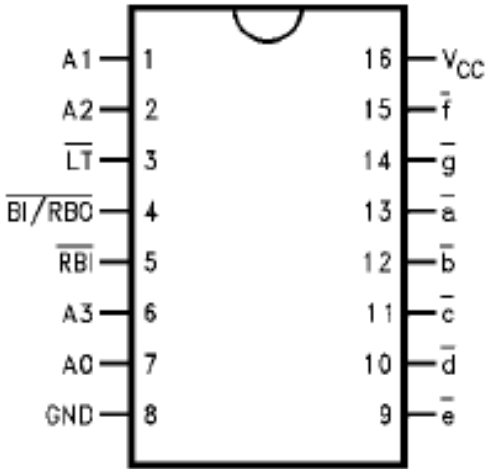



Fig. 4 Pin arrangement of 74HC47

Table 3. Truth table of 74HC47

**Truth Table**

| Decimal or Function | Inputs | | | | | | | Outputs | | | | | | | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{LT}$ | $\overline{RBI}$ | A3 | A2 | A1 | A0 | $\overline{BI/RBO}$ | $\overline{a}$ | $\overline{b}$ | $\overline{c}$ | $\overline{d}$ | $\overline{e}$ | $\overline{f}$ | $\overline{g}$ | |
| 0 | H | H | L | L | L | L | H | L | L | L | L | L | L | H | |
| 1 | H | X | L | L | L | H | H | H | L | L | H | H | H | H | |
| 2 | H | X | L | L | H | L | H | L | L | H | L | L | H | L | |
| 3 | H | X | L | L | H | H | H | L | L | L | L | H | H | L | |
| 4 | H | X | L | H | L | L | H | H | L | L | H | H | L | L | |
| 5 | H | X | L | H | L | H | H | L | H | L | L | H | L | L | |
| 6 | H | X | L | H | H | L | H | H | H | L | L | L | L | L | |
| 7 | H | X | L | H | H | H | H | L | L | L | H | H | H | H | |
| 8 | H | X | H | L | L | L | H | L | L | L | L | L | L | L | |
| 9 | H | X | H | L | L | H | H | L | L | L | H | H | L | L | |
| 10 | H | X | H | L | H | L | H | H | H | H | L | L | H | L | |
| 11 | H | X | H | L | H | H | H | H | H | L | L | H | H | L | |
| 12 | H | X | H | H | L | L | H | H | L | H | H | H | L | L | |
| 13 | H | X | H | H | L | H | H | L | H | H | L | H | L | L | |
| 14 | H | X | H | H | H | L | H | H | H | H | L | L | L | L | |
| 15 | H | X | H | H | H | H | H | H | H | H | H | H | H | H | |
| $\overline{BI}$ | X | X | X | X | X | X | L | H | H | H | H | H | H | H | |
| $\overline{RBI}$ | H | L | L | L | L | L | L | H | H | H | H | H | H | H | |
| $\overline{LT}$ | L | X | X | X | X | X | H | L | L | L | L | L | L | L | |

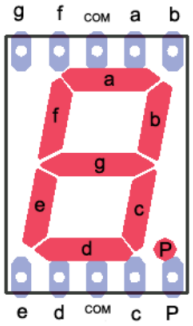



Fig. 5 Pin arrangement of a 7-segment display

## 3. Experiments

3.1 4-channel word generator

Word generator in Multisim is very helpful as input to logic circuit so that you can observe the waveform to check the logic function. However, the function generator in the lab can not work as the word generator to output a number of parallel signals. Based on flip-flop, you can help to further upgrade the function generator into a word generator.

1) Design a 4-channel word generator based on two 74HC74 ICs. You can take reference on how to design based on Figure 7-37 in page 411 of your textbook *Digital Fundamentals*. Though the figure does not include Set and Reset, you are able to include them in the design.
2) Use 2 channels of SIM to provide Set and Reset signals.
3) Output a square wave of 2Hz (0V as low, 5 V as high, and 50% as duty cycle) from the function generator, and connect it to the Clock input of the first D flip-flop.
4) Use 7 channels of Logic Analyzer to capture the signals of Set, Reset, 2Hz square wave, and the 4 states of the 4 D flip-flops. Validate that your circuit works well.
5) Keep this circuit for 3.2.

**[DEMONSTRATION]** Show instructor or TA when you have completed this.

**[IN REPORT]** Include all your design, and test results.

3.2 Counter shown in 7-Segment Display

1) The 4-channel outputs can be regarded as BCD codes (from 1111 to 0000 and back to 1111 again) input to the 7-segment display. Try to wire 74HC47 and the 7-segment display again. Connect the 4-channel outputs into 74HC47, and observe that your display flashes from 9 down to 0. You can also see that when the BCD code is from 1010 to 1111, other symbol are shown in the 7-segment display.
2) We do not want to have the count-down functionality. You are required to change the circuit very little to make it count-up from 0 to 9. When it is over 9, the display still shows oddly. It does not matter at this step.
3) Now, it is time to make the counter into a loop from 0 to 9 and back to 0 again. Try to design the circuit, and realize it. (Hint: when the state reach 1010, set the 4 D flip-flops. You will need to use some basic chips. You can try to choose from 74HC08, 74HC00, 74HC32)
4) When you complete this experiment, unwire the two 74HC74 chips, but keep 74HC47 and the 7-segment display, which you still need in the future.

**[DEMONSTRATION]** Show instructor or TA when you have completed each step in 1) and 3).

**[IN REPORT]** Include all your design, and test results.

**[QUESTION]**

(1) How to design a circuit generating a circuit of BCD codes from 0000=>0001=>0010=>0011=>0100=>0111=>1000=>0000=>0001=>…?
(2) In step 3) we have provided chips which are not necessary. Can you find the least number of basic gates?

3.3 Responder (抢答器)

In a competition, four players will press each responder to get the chance to answer questions. The quickest will get his/her ID shown in the screen, while disabling the

others' responders. A judge will clear the signal and reset for the next round. Based on flip-flop, you can design this.

1) Observe the circuit diagram as below. Understand why it can work as the responder.

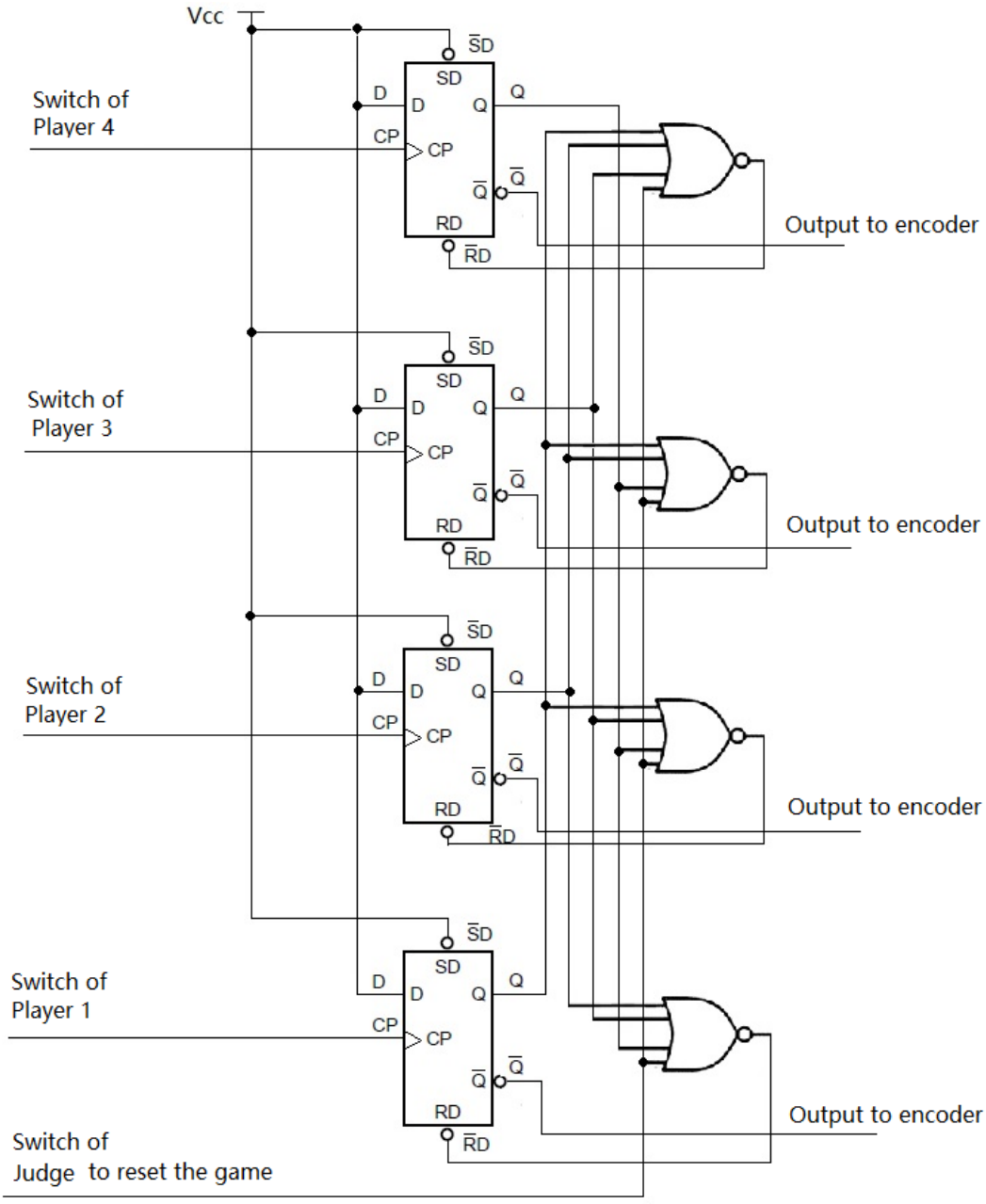



Fig. 6 Circuit of responder module

Build the circuit with 74HC74x2, 4002x2, SIM and LOM. Verify that it works.

2) Design a circuit to connect the 4 outputs to 8-3 line priority encoder. In this experiment, only one output can be low at one time, the priority encoder 74HC148 has the same functionality as an ordinary encoder. You should note that the 3-line output are opposite of the lower 3 bits of a traditional BCD code, i.e. 7 is indicated by 000 rather than 111. You need to use a 74HC04 to invert it back, and then add

a 0 in the MSB to form a full BCD code. Connect the output now with the LOM to verify that your circuit works well. When the fastest player turns on the switch, his switch ID will be shown as BCD code in your LOM.

3) Show the BCD code onto the 7-segment display.

**[DEMONSTRATION]** Show instructor or TA when you have completed 1), 2) and 3).

**[IN REPORT]** Include all your design, and test results.

**[QUESTION]** Currently, when the judge resets the circuit, the display shows "0". But there is no player with ID "0". It is better that no segment in the display is lightened. There is a way that you change your circuit by changing only 1 wire. Can you find out how? (Hint: observe the truth tables of 74HC148 and 74HC47.)

## 4. Lab Report

Submit the report of Lab 5 in ***PDF*** to the folder ***Digital Systems Design Lab/Report Submission/Lab 5*** on Blackboard by the deadline below:

- **23:59, April 28, 2024**

**Each day of late submission will result in 10% deduction in the report raw marks.**

## Appendix:

IC needed for this lab:

1. 74HC74 x2
2. 4002 x2
3. 74HC00 x1
4. 74HC04 x1
5. 74HC08 x1
6. 74HC47 x1
7. 74HC148 x1
8. 7-segment display x1
9. 20 channel Dupont cable x1
10. 330 Ohm resistor x7