

EIE2810 Digital Systems Design Laboratory

Laboratory Report #4

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This laboratory consists of 4 experiments, they are:

- Experiment A: The full adder simulation.
- Experiment B: Verify the 7-segment display with BCD codes.
- Experiment C: Verify the 2-bits * 2-bits multiplier with a 4-line-to-16-line decoder.
- Experiment D: Use the 7-segment display to show the outcomes of the 2-bits * 2-bits multiplier.

1. Experiment A

1.1 Design

To verify the full adder, with the truth table, we designed a circuit diagram for the full adder, and the designed circuit diagram is shown in Figure 1.

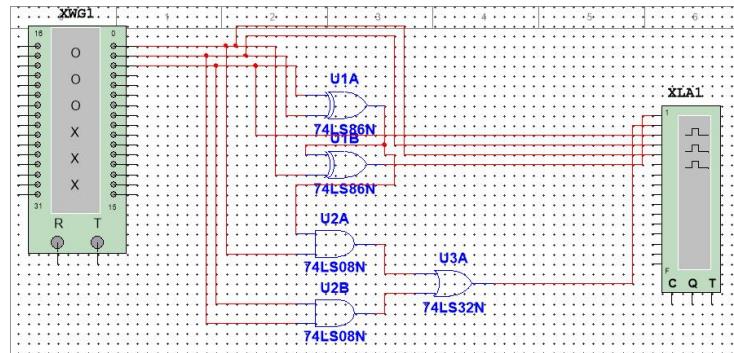


Figure 1 The Designed Circuit for the Full Adder

As shown in Figure 1, two XOR Gates, 2 AND Gates, and 1 OR Gate are used to construct this circuit.

1.2 Results

The truth table for the full adder is shown in Table 1.

Table 1

Inputs			Outputs	
A	B	C _{in}	C _{out}	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0

1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The test results are shown in Figure 2.

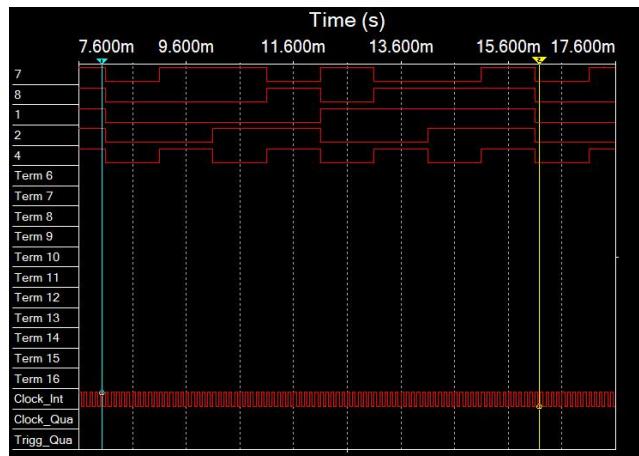


Figure 2 The Test Results for the Full Adder Circuit

As shown in Figure 2, the test results lie between the blue line and the yellow line, the top signal represents Sum, the second top signal represents C_{out} , and the rest three signal represent A, B, and C_{in} from the third signal to the lowest signal, respectively. We can see that the Sum signal is at a high level when there are one or three high-level input signals, and the C_{out} signal is at a high level when there are two or three high-level input signals, which all go well with the truth table. This means our design successfully verified the two-bit full adder.

2. Experiment B

2.1 Design

To verify the 7-segment display, a circuit was designed according to the 74LS47 truth table. The designed circuit diagram is shown in Figure 3.

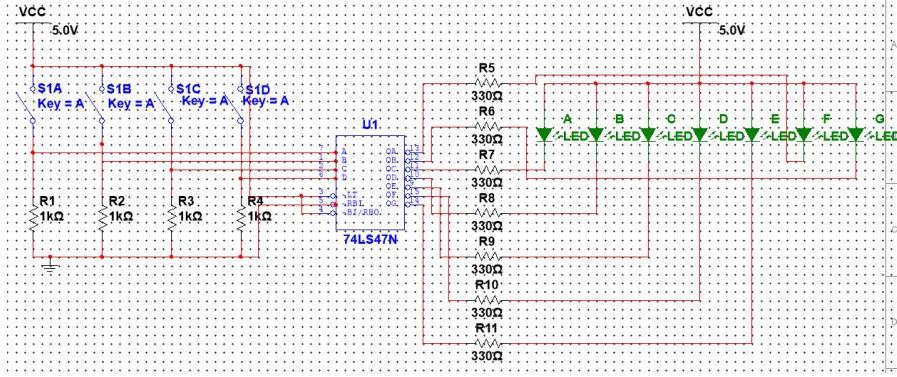


Figure 3 The Designed Circuit for the 7-Segment Display

As shown in Figure 3, four SIMs are used to produce the BCD codes and they are connected to the inputs of the 74LS47 IC, 7 outputs of the 74LS47 IC are connected to 7 LEDs, which represent 7 LEDs on the 7-segment display.

2.2 Results

A circuit was assembled according to the circuit diagram shown in Figure 3. Different BCD signals are given to the input of the circuit, the results are shown in Figure 4.

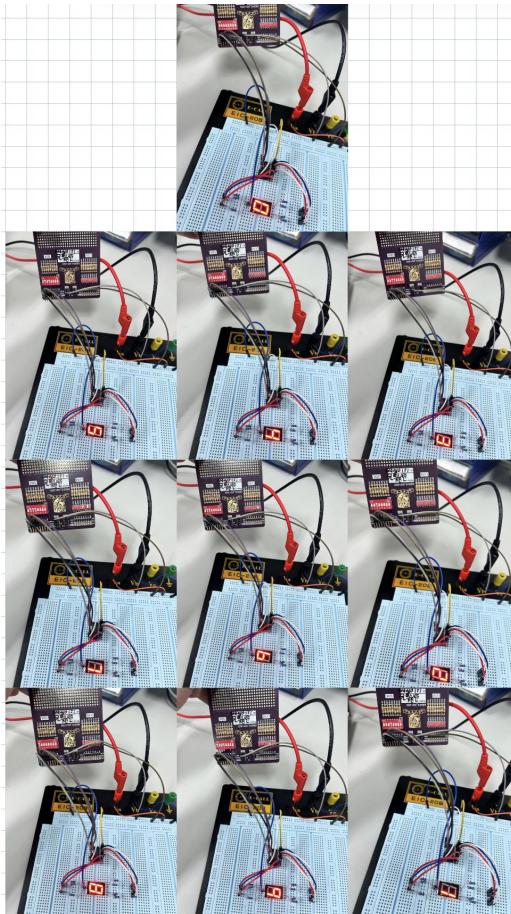


Figure 4 The 7-Segment Display With Different Input BCD Signals

As shown in Figure 4, when the input BCD signal is 0000, the 7-segment display is 0; when the input BCD signal is 0001, the 7-segment display is 1; when the input BCD signal is 0010, the 7-segment display is 2; when the input BCD signal is 0011, the 7-segment display is 3; when the input BCD signal is 0100, the 7-segment display is 4; when the input BCD signal is 0101, the 7-segment display is 5; when the input BCD signal is 0110, the 7-segment display is 6; when the input BCD signal is 0111, the 7-segment display is 7; when the input BCD signal is 1000, the 7-segment display is 8; when the input BCD signal is 1001, the 7-segment display is 9., which are all correct. This means we successfully verified the 7-segment display circuit.

2.3 Questions

Observation: I notice variations in current and power consumption as different numbers are displayed.

Explanation: This phenomenon occurs because different numbers require lighting up a different number of segments on the 7-segment display. For example, displaying '1' lights up fewer segments than displaying '8'. Therefore, more segments being lit means higher current consumption, as each segment draws current. The power consumption, given by $P=VI$ (where P is power, V is voltage, and I is current), also varies accordingly. The resistance of 330 ohms limits the current through each segment, but the total current drawn by the display will still depend on the number of segments lit at any given time.

3. Experiment C

3.1 Design

To verify the 2-bits * 2-bits multiplier with IC 74HC154 (4-line-to-16-line decoder), a circuit was designed according to the multiplier truth table. The truth table of the multiplier is shown in Table 2, and the output of the decoder corresponding to different inputs is shown in Table 3 (the decoder is always enabled to get the results).

Table 2

A0	A1	B0	B1		Y3	Y2	Y1	Y0
0	0	0	0		0	0	0	0
0	0	0	1		0	0	0	0
0	0	1	0		0	0	0	0
0	0	1	1		0	0	0	0
0	1	0	0		0	0	0	0

0	1	0	1			0	0	0	1
0	1	1	0			0	0	1	0
0	1	1	1			0	0	1	1
1	0	0	0			0	0	0	0
1	0	0	1			0	0	1	0
1	0	1	0			0	1	0	0
1	0	1	1			0	1	1	0
1	1	0	0			0	0	0	0
1	1	0	1			0	0	1	1
1	1	1	0			0	1	1	0
1	1	1	1			1	0	0	1

Table 3

A 0	A 1	B 0	B 1	Outputs															
				O 0	O 1	O 2	O 3	O 4	O 5	O 6	O 7	O 8	O 9	O 10	O 11	O 12	O 13	O 14	O 15
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1

1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

According to Table 2 and Table 3, we can get the relationship between the output signal (Y_3, Y_2, Y_1, Y_0) and the output of the decoder (O_0, O_1, \dots, O_{15}).

$$Y_3 = O_{15} = \overline{O_{15}}$$

$$Y_2 = O_{14} + O_{11} + O_{10} = \overline{O_{14}} \overline{O_{11}} + \overline{O_{10}}$$

$$Y_1 = O_6 + O_7 + O_9 + O_{11} + O_{13} + O_{14} = \overline{O_6} \overline{O_7} + \overline{O_9} \overline{O_{11}} + \overline{O_{13}} \overline{O_{14}}$$

$$Y_0 = O_5 + O_7 + O_{13} + O_{15} = \overline{O_5} \overline{O_7} + \overline{O_{13}} \overline{O_{15}}$$

With all of these relationships, we can design a circuit as shown in Figure 5.

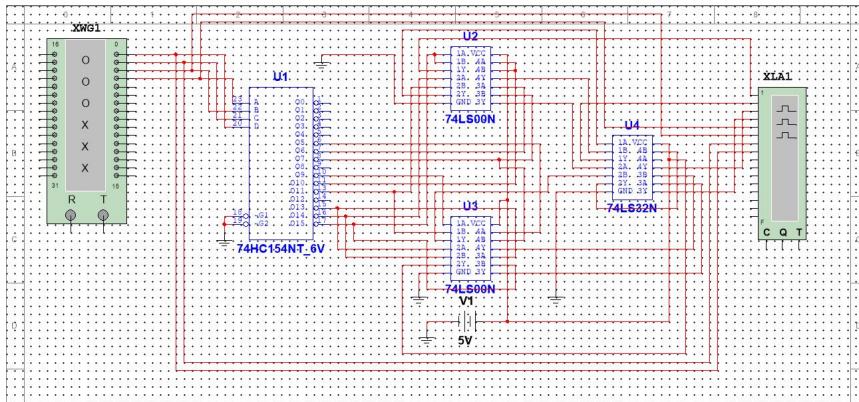


Figure 5 The IC Level Designed Circuit Diagram

As shown in Figure 5, one NAND Gate is used to produce $\overline{O_{15}}$; 2 NAND Gates and 1 OR Gate are used to produce $\overline{O_{14}} \overline{O_{11}} + \overline{O_{10}}$; 3 NAND Gates and 2 OR Gates are used to produce $\overline{O_6} \overline{O_7} + \overline{O_9} \overline{O_{11}} + \overline{O_{13}} \overline{O_{14}}$; and 2 NAND Gates and 1 OR Gates are used to producing $\overline{O_5} \overline{O_7} + \overline{O_{13}} \overline{O_{15}}$.

3.2 Results

The finished circuit for the circuit diagram in Figure 5 is shown in Figure 6.

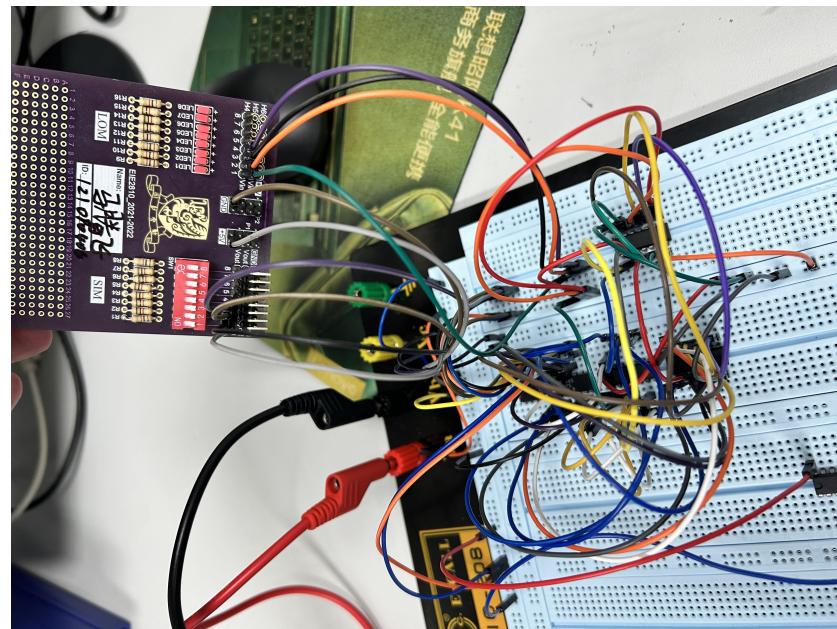


Figure 6 The Finished Circuit for the Multiplier With Decoder

Give the SIM different input and check the luminous condition of the LOM. The luminous conditions for different input logic are shown in Figure 7 and Figure 8.

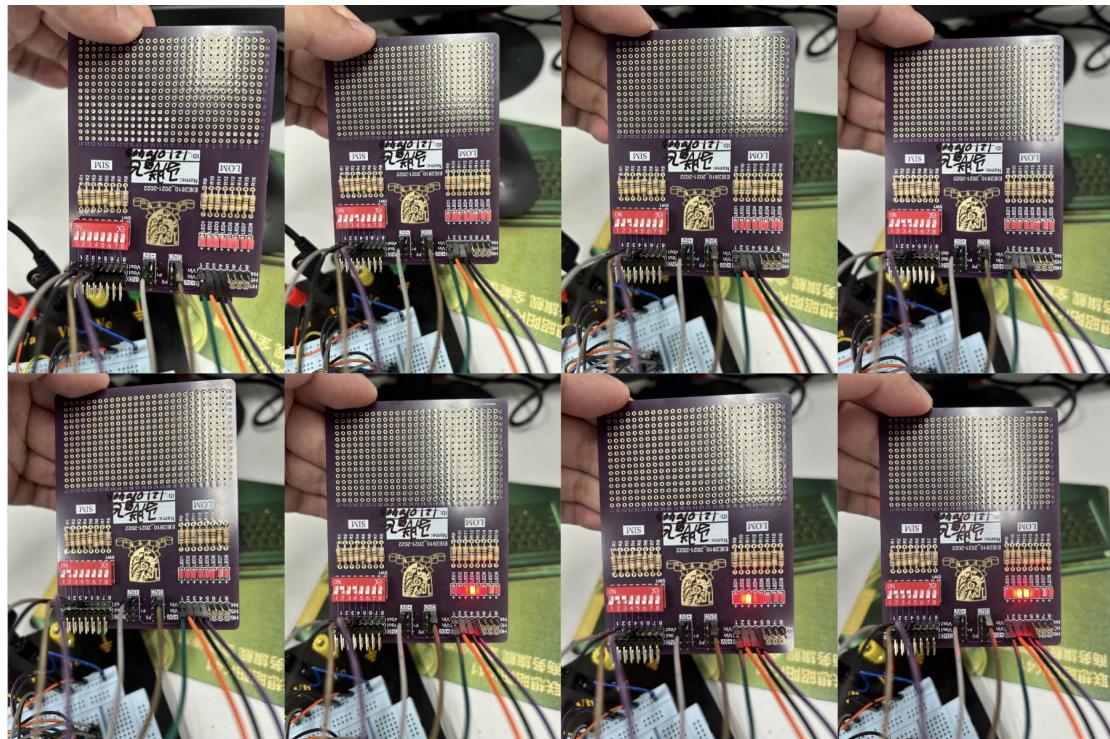


Figure 7 The Luminous Condition for First 8 Input Logic (0000 to 0111)

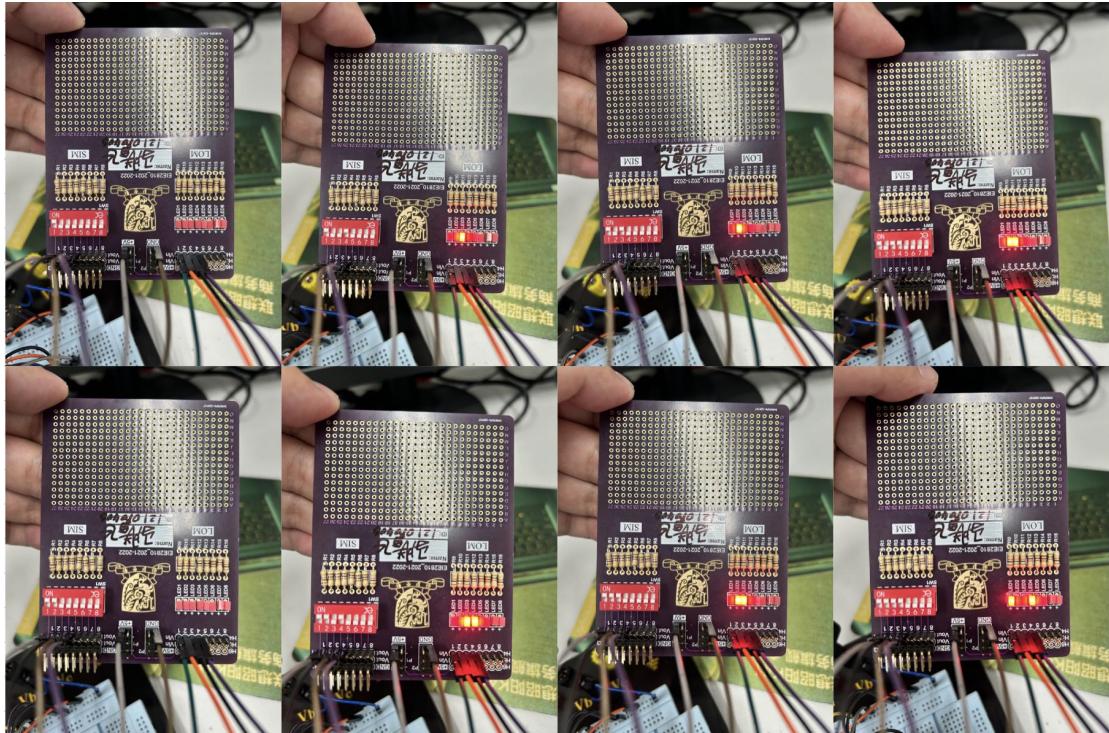


Figure 8 The Luminous Condition for Rest of the Input Logic (1000 to 1111)

As shown in Figure 7 and Figure 8, the output is 0001_2 (1_{10}) when the input is 01_2 and 01_2 (1_{10}), the output is 0010_2 (2_{10}) when one input is 01_2 (1_{10}) and another is 10_2 (2_{10}), the output is 0100_2 (4_{10}) when both inputs are 10_2 (2_{10}), the output is 0011_2 (3_{10}) when one input is 11_2 and another is 01_2 (1_{10}), the output is 0110_2 (6_{10}) when one input is 11_2 (3_{10}) and another is 10_2 (2_{10}), the output is 1001_2 (9_{10}) when both two inputs are 11_2 (3_2), and the output is 0000_2 (0_{10}) otherwise. All of the results go well with the truth table, which means we successfully constructed the multiplier with a decoder.

3.3 Questions

Step 1: Work out the truth table, a 2-bit binary number adding another 2-bit binary number will not give a result that exceeds 3 bits. So, 3 outcome bits are used. The truth table is shown in Table 4.

Table 4

A0	A1	B0	B1	Y2 (or carry bit)	Y1	Y0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1

0	1	0	1		0	1	0
0	1	1	0		0	1	1
0	1	1	1		1	0	0
1	0	0	0		0	1	0
1	0	0	1		0	1	1
1	0	1	0		1	0	0
1	0	1	1		1	0	1
1	1	0	0		0	1	1
1	1	1	0		1	0	0
1	1	1	1		1	0	1
1	1	1	1		1	1	0

Step 2: Construct the relationship between the truth table (Y2, Y1, and Y0) and the outputs of the decoder (O0, O1,..., O15).

$$Y_2 = 07 + 010 + 011 + 013 + 014 + 015 = \overline{07} \overline{010} \overline{011} \overline{013} \overline{014} \overline{015}$$

$$\begin{aligned} Y_1 &= 02 + 03 + 05 + 06 + 08 + 09 + 012 + 015 \\ &= \overline{02} \overline{03} \overline{05} \overline{06} \overline{08} \overline{09} \overline{012} \overline{015} \end{aligned}$$

$$\begin{aligned} Y_0 &= 01 + 03 + 04 + 06 + 09 + 011 + 012 + 014 \\ &= \overline{01} \overline{03} \overline{04} \overline{06} \overline{09} \overline{011} \overline{012} \overline{014} \end{aligned}$$

Step 3: Design the logic symbol level circuit diagram. The designed circuit diagram is shown in Figure 9.

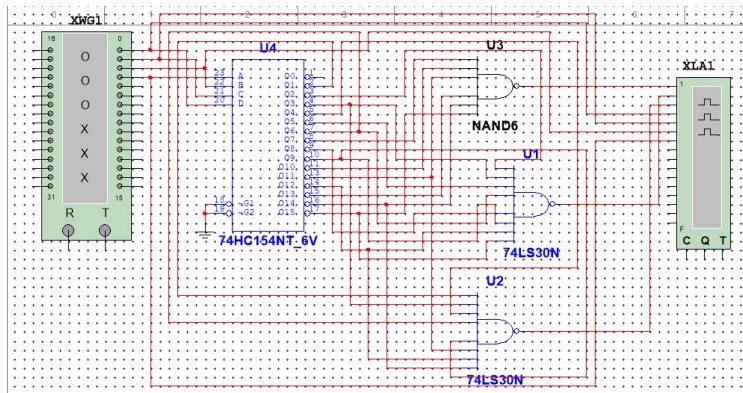


Figure 9 The Designed Circuit Diagram for the 2-bit+2-bit Adder

4. Experiment D

4.1 Design

To combine the 7-segment display and the 4-line-to-16-line decoder, a circuit was designed according to the 74LS47 truth table and 74HC154 truth table. The designed circuit diagram is shown in Figure 10.

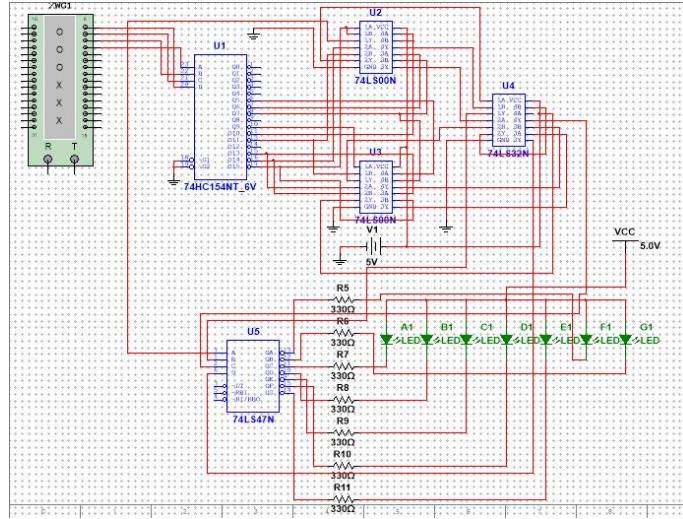


Figure 10 The Designed Circuit for the Combination of the 7-Segment Display and the 4-Line-to-16-Line Decoder

4.2 Results

The results of the 7-segment display corresponding to different input 2-bit*2-bit signals are shown in Figure 11 and Figure 12.

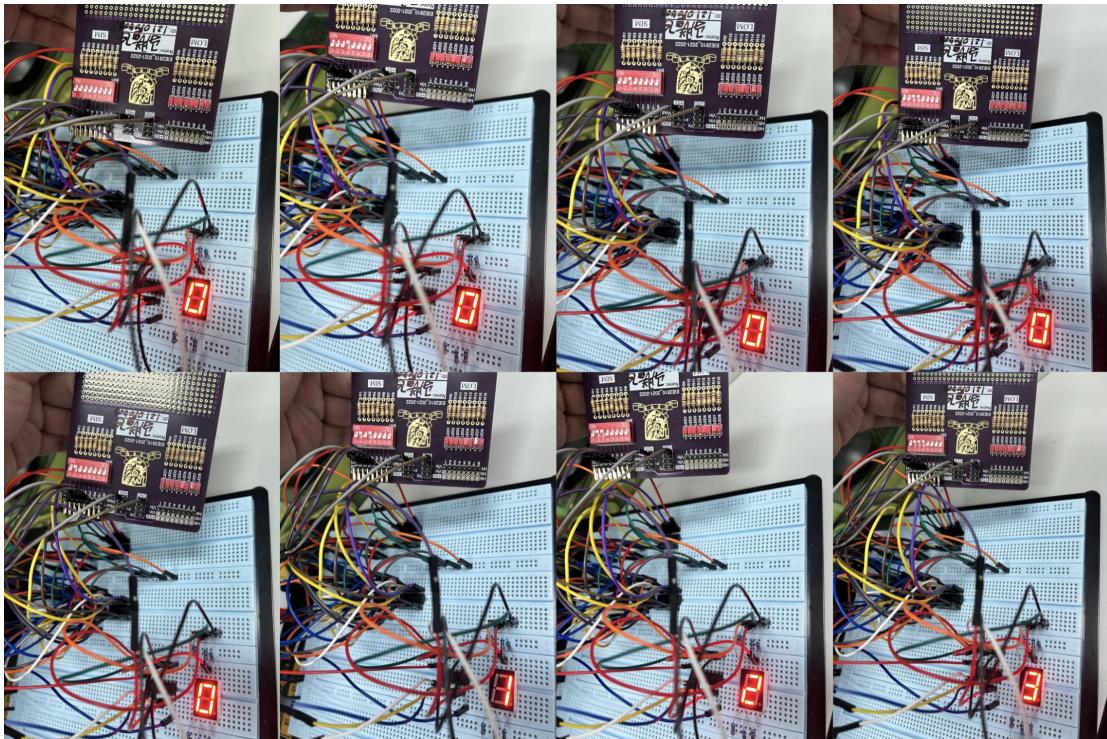


Figure 11 The 7-Segment Outputs for First 8 Input Logic (0000 to 0111)

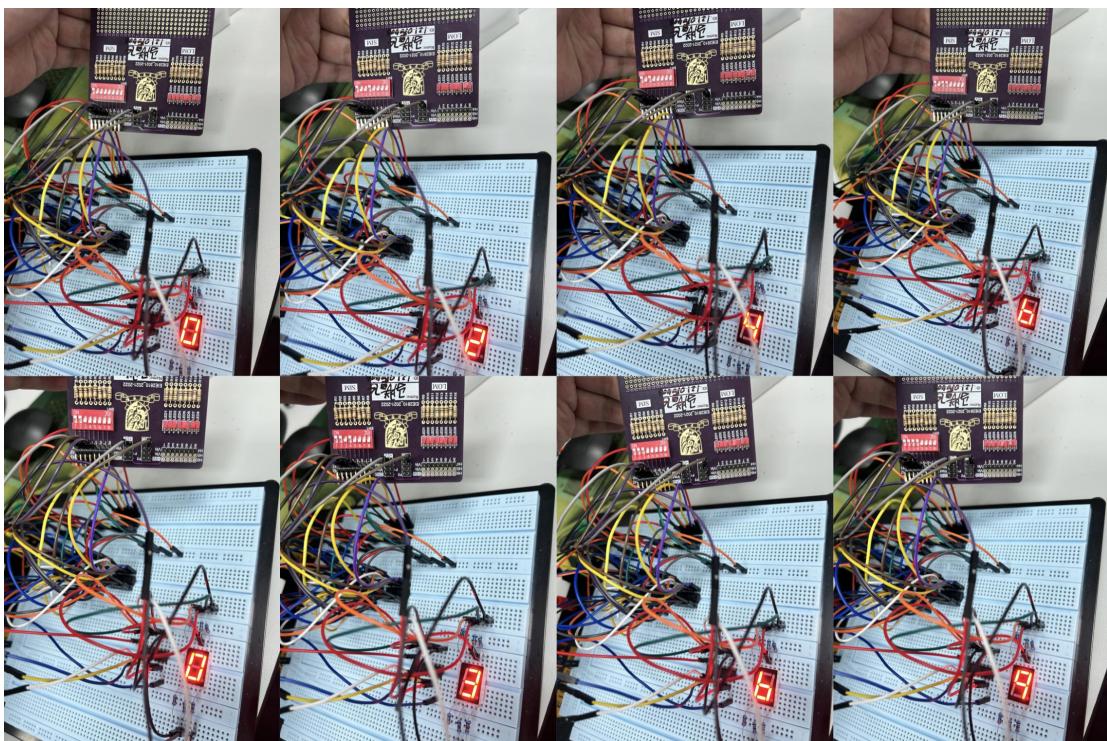


Figure 12 The 7-Segment Outputs for Rest of the Input Logic (1000 to 1111)

As shown in Figure 11 and Figure 12, the output is 1_{10} when the input is 01_2 and 01_2 (1_{10}), the output is 2_{10} when one input is 01_2 (1_{10}) and another is 10_2 (2_{10}), the output is 4_{10} when both inputs are 10_2 (2_{10}), the output 3_{10} when one input is 11_2 and another is 01_2 (1_{10}), the output is 6_{10} when one input is 11_2 (3_{10}) and another is 10_2 (2_{10}), the output is 9_{10} when both two inputs are 11_2 (3_2). and the output is 0_{10} otherwise. All of

the results go well with the truth table, which means we successfully constructed the multiplier with a decoder and combined it with the 7-segment display.

5. Conclusion

In this lab, we did a full-adder simulation, verified the 7-segment display and a multiplier with a decoder, and we combined the 7-segment display and the multiplier with a decoder. From the lab, we know:

- 1) The inner principle of the full adder.
- 2) The way to use the 7-segment display circuit element.
- 3) The way to make use of the logic of the decoder.
- 4) The way to construct a multiplier with a decoder.
- 5) The way to combine the constructed multiplier to the 7-segment display.