EIE2810 Digital Systems Design Laboratory

Laboratory 4

Functions of Combinational Logic, Adder, 7-Segment Display, Decoder

School of Science and Engineering

The Chinese University of Hong Kong, Shenzhen

2023-2024 Term 2

1. Objectives

In the Laboratory 4, we will spend the 2-week sessions on the following:

- Learn to build up a full-adder in Multisim.
- Learn to use 7-segment display, and BCD-to-7-segment decoder (74LS47).
- Learn to use 4-line-to-16-line decoder (74HC154).
- Learn to build up an integrated 2-bit x 2-bit multiplier with SIM, 74HC154, 74LS47, and 7-segment indicator.

2. Introduction

2.1 Full-adder

The truth table of the full-adder can be listed in Table 1. There are 3 inputs (A, B, and input carry) and 2 outputs (sum and output carry).

Table 1. Truth table of a full adder

Input			**Output**	
A	**B**	**C_{in}**	**C_{out}**	**Sum**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The logics for Sum and C_{out} are:

- Sum=(A XOR B) XOR C_{in}
- C_{out}=AB+(A XOR B) C_{in}

2.2 7-segment display and BCD-to-7-segment decoder (74LS47)

7-segment displays are widely used in digital clocks, electronic meters, basic calculators, and other electronic devices that display numerical information. Fig. 1 shows one typical 7-segment display. It has 1 LED for each segment and another LED for the decimal point.

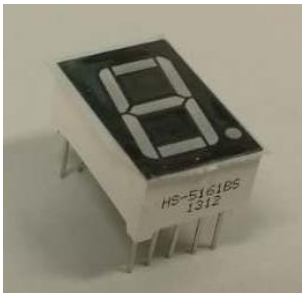


Fig. 1 7-segment display

In a simple LED package, typically all of the cathodes (negative terminals) or all of the anodes (positive terminals) of the segment LEDs are connected and brought out to a common pin; this is referred to as a "common cathode" or "common anode" device.

In our experiment, we are using a common anode 7-segment display, with circuit as below. If the pin of the corresponding segment has low voltage, it is on. Otherwise with high voltage, it is off.

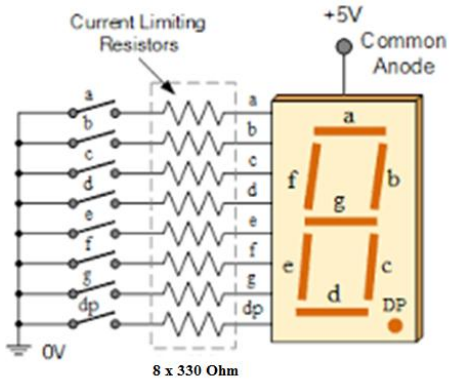


Fig. 2 Pin connection with 330 Ohm resistors of a common anode 7-segment display

To limit the current and protect the display, in normal practice, we will use a resistor (typically 330 Ohm) to connect the segment pin to the switch. The pin arrangement of the component in this experiment is illustrated as below. The 2 pins for 5V are inter-connected inside the display.

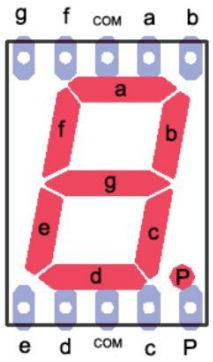


Fig. 3 Pin arrangement of a 7-segment display

To make it easier to control the 7 segments, a BCD-to-7-segment decoder (74LS47) can be used to change the BCD code to the 7-segment code. The figure below illustrates the pin arrangement. $A_3A_2A_1A_0$ are the input BCD code from MSB to LSB.

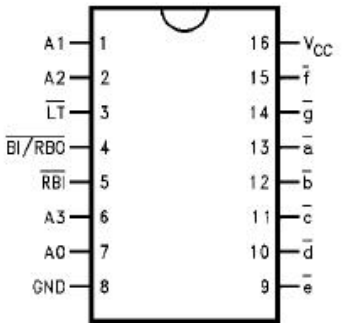


Fig. 4 Pin arrangement of 74LS47

The normal Vcc for 74LS47 is 5V in the datasheet.

It is important to observe the truth table (Table 2) and understand it.

Table 2. Truth table of 74LS47

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	

$\overline{LT}$ is the lamp test. $\overline{RBI}$ is ripple blanking input. $\overline{BI}$/ $\overline{RBO}$ (blanking input/ripple blanking output) can work as either input or output.

- When $\overline{LT}$ and $\overline{BI}$/ $\overline{RBO}$ are both high, you will enable the 7-segment display from 0 to 14 (10-14 are indicated by other symbol). The $\overline{\ }$ in $\overline{a}$~$\overline{g}$ indicates that, when

logic is activated, the output is “low” rather than “high”. This fits appropriately to the common anode 7-segment display.

- When $\overline{LT}$ is low and $\overline{BI}/\overline{RBO}$ is high, it turns on all the segments, and you can test if any segment is burnt.
- For $\overline{BI}/\overline{RBO}$, it has feature for zero suppression. We will not test that in this lab. You may refer to page 339 the text book *Digital Fundamentals*.

2.3 4-line-to-16-line decoder (74HC154)

74HC154 is another decoder to map a 4-digit input into one of 16 outputs. Typical Vcc=5V. The pin arrangement and logic symbol are shown in Fig. 5.

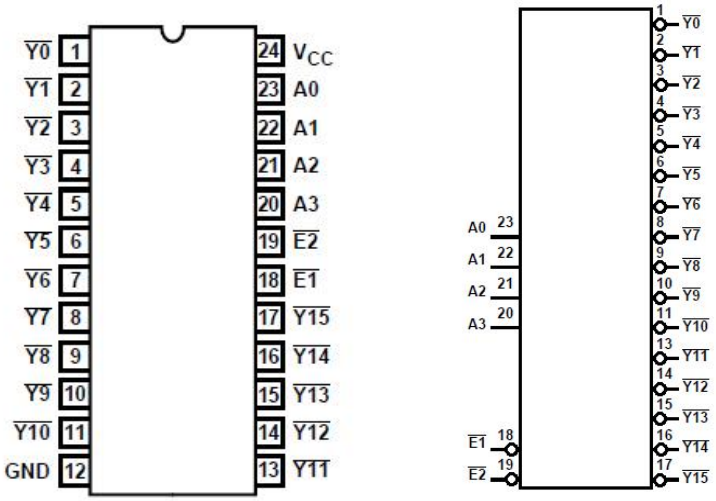


Fig. 5 Pin arrangement and logic symbol of 74HC154

Table 3. Truth table of 74HC154

INPUTS						OUTPUTS														
$\overline{E1}$	$\overline{E2}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

- From the truth table above, you can observe that the chip is enabled when both $\overline{E1}$ and $\overline{E2}$ are low.
- The first 16 row from the top indicates the 16 input–output relations. E.g. when $A_3A_2A_1A_0 = 0110$, the pin $\overline{Y6} = 0$ while all other output are high.

3. Experiments

3.1 Use Multisim to build up the full adder in 2.1 based on gate symbols (not chips). You can feel free to choose gate types. Use Word Generator to generate the wave form to test verify the truth table.

[DEMONSTRATION] Show instructor or TA when you have completed this.

[IN REPORT] Include all your design, test result, and analysis in the verification.

3.2 This step is hardware implementation. Design your circuit first. Use 4 channels of SIM to generate a 4-bit BCD code, input this code to 74LS47, and feed the output of 74LS47 to the 7-segment display. Verify that all the BCD codes can be displayed correctly. Do not forget to wire a 330 ohm resistor between each segment pin and 74LS47 output pin.

After your completion of this stage, take away SIM and LOM, but keep the rest of circuit. You will need it in Experiment 3.4.

[DEMONSTRATION] Show instructor or TA when you have completed this.

[IN REPORT] Include your chip level circuit diagram (drawn by hand) for this experiment. Your test result, which can verify your successful completion.

[QUESTION] Observe the current and power consumption from DC power supply when you change the BCD code. What phenomena can you observe roughly? Try to explain why.

3.3 2-bit x 2-bit multiplier (*AGAIN*)

You have built up a 2-bit x 2-bit multiplier by basic logic gates in lab 3. A_1A_0 x B_1B_0 = $X_3X_2X_1X_0$. This time, you are asked to re-design the circuit based on the 4-line-to-16-line decoder (74HC154) and a number of simple logic gates (74HC00 x 2 and 74HC32 x 1). Though the number of chips is not reduced significantly, the design process is easier. Truth table is needed but no Karnaugh map is necessary. Use SIM to control the 4 inputs, and LOM to show the 4-bit outputs.

After your completion of this state, take away LOM, but keep the rest of circuit. You will need it in Experiment 3.4.

[DEMONSTRATION] Show instructor or TA when you have completed this.

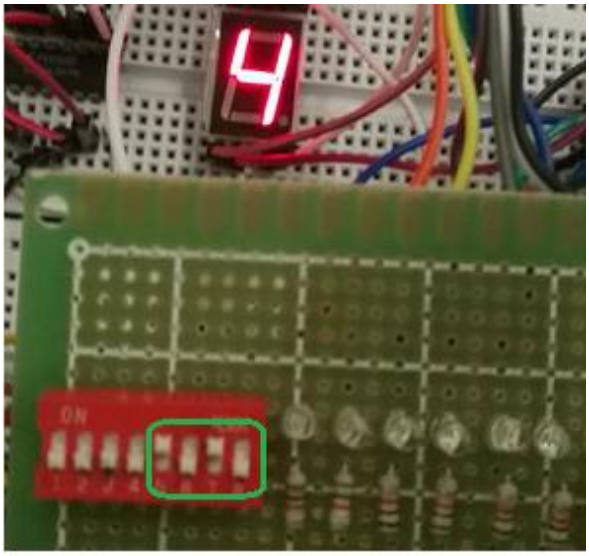
[IN REPORT] Include your design steps (Truth table, how you map the truth table to the decoder's output, how you derive the logic functional expressions for each output, the circuit diagram for wiring, etc.). Include your test result.

[QUESTION] If you are required to build into a 2-bit + 2-bit summation, how will design the circuit? Put down the intermediate steps of your design, and the final designed logic symbol level circuit diagram (Not chip level. Hand drawn is allowed.). No need to implement it. You will need to use NAND to connect the output pins of 74HC154. At this time, you do not have limit of using only 74HC00. You can use NAND with any number of inputs.

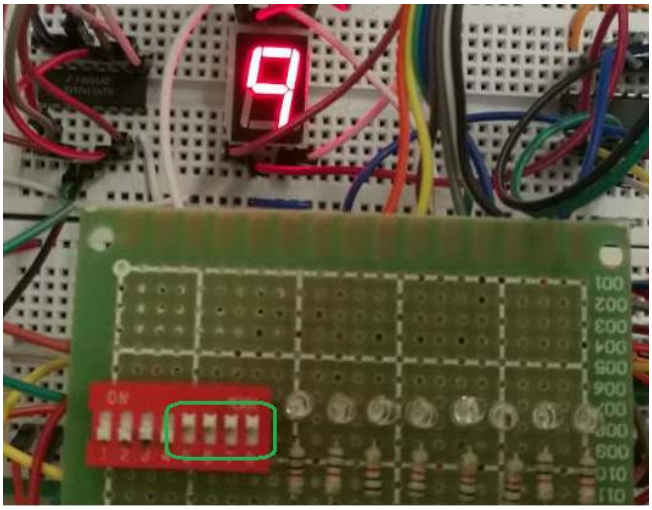
3.4 Combine multiplier with 7-segment display.

In this step, you will practice to implement a multiplier which can display a number as output. Two examples are shown in the Fig. 6 below. SIM will generate four bits as input, while display show the output.

Integrate the circuits in Experiment 3.3 and 3.4 together.



0b10 x 0b10 = 0b0100 = 4



0b11 x 0b11 = 0b1001 = 9

Fig. 6 Two states in Experiment 3.4

[DEMONSTRATION] Show instructor or TA when you have completed this.

[IN REPORT] Include the images of your test results.

4. Lab Report

Write the lab report comprehensively. A template has been provided on Blackboard. You can find it in the folder named Digital Systems Design Lab/Report Template.

Submit the report of Lab 4 in **PDF** to the folder **Digital Systems Design Lab/Report Submission/Lab 4** on Blackboard by the deadline below:

- **23:59, Friday, April 12th, 2024**

Each day of late submission will result in 10% deduction in the report raw marks.

Appendix:

IC needed for this lab:

1. 74HC00 x2
2. 74HC32 x1
3. 74LS47 x1
4. 74HC154 x1
5. 7-segment display x1
6. 330 Ohm resistor x7

Remember to sort and return items 1-6 back to the storeroom after lab.

For any malfunctioning component, report to instructor or TA, and DO NOT put it back.