ECE2810 Digital Systems Design Laboratory

Lab 1: Logic analyzer / CMOS and TTL / Datasheet / Basic Experiments on AND and NOT Gates

School of Science and Engineering

The Chinese University of Hong Kong, Shenzhen

2023-2024 Term 2

1. Objectives

In Lab 1, we will spend the 2-week session to understand the following:

- Learn to use a logic analyzer.
- Understand the difference in CMOS and TTL
- Learn to read the datasheet of ICs
- Basic experiments on AND gate and NOT gate
  - Learn to build simple AND circuit by diode and transistors
  - Learn to measure voltage transfer characteristics (VTC) of AND gate
  - Understand the different voltage levels by CMOS and TTL AND gates
  - Understand chip propagation delay time, and learn the way to measure it

2. Logic Analyzer

The oscilloscope Tektronix MSO2022B has the functionality of logic analyzer.

- To enable this, press the button D15-D0. You will find 8 lines of signals indicating 8 digital channels.
- The timeline may be too fast to observe. To slow down, use the 'Horizontal-scale'.

Figure 1. Buttons for Logic Analyzer

- Generate approximately 0V as "0" and 5V as "1", to output by your SIM. Think about how to do this.
- Connect SIM output pins with logic analyzer through the socket below. Before the connection, make sure that SIM is powered off. The ground signal of SIM should be connected to G of the logic probe. As you can see from the requirement on the socket, NEVER exceed the voltage range of ±40V.

Figure 2. Probes in Logic Analyzer

- Now you will be able to test the logic analyzer by your SIM. Manually turn on/off each switch and generate and save an image on the logic analyzer screen.
- **[IN REPORT]** Include:
    - A circuit diagram of the connection of SIM (including the switches, resistors, etc.), power supply, and logic analyzer.
    - The image of the 8 channel digital signals on the logic analyzer interface.

3. CMOS and TTL

To represent digital logic "0" and "1", there are different voltage levels. TTL and CMOS are two of them.

TTL stands for Transistor-Transistor Logic. It is a class of integrated circuits (ICs). The name is derived from the use of two Bipolar Junction Transistors (BJTs) in the design of each logic gate. CMOS (Complementary Metal Oxide Semiconductor) is another classification of ICs that uses Field Effect Transistors in the design. Some comparison in their features are listed as below:

- The primary advantage of CMOS chips to TTL chips is in the greater density of logic gates within the same material.
- TTL chips tend to consume a lot more power compared to CMOS chips, especially at rest.
- CMOS chips are a bit more delicate compared to TTL chips when it comes to handling as it is quite susceptible to electrostatic discharge.

The voltage levels of TTL and CMOS are different.

Table 1. Voltage levels of TTL and CMOS

Technology	L voltage	H voltage	Notes
CMOS	0 V to 1/3 V_{CC}	2/3 V_{CC} to V_{CC}	V_{CC} = supply voltage
TTL	0 V to 0.8 V	2 V to V_{CC}	V_{CC} = 5 V ±10%

In this lab, we will examine the difference between CMOS and TTL based on the two ICs, 74HC08 and 74LS08, both with the functionality of AND gate.

4. Datasheet of IC

To understand how to use a digital logic IC, it is crucial to have the capability to read its datasheet, which provides enriched information of the chip, sometimes too much for a beginner. In the appendix of this lab handout, we have provided a complete datasheet of 74LS08, 74HC08 and 74HC04.

For beginners, the most important specifications include:

- *Supply voltage*, in Table of Recommended Operating Conditions
- *Input voltages V_{IH} and V_{IL}, output voltages V_{OH} and V_{OL},* in Table of Electrical Characteristics
- *PIN arrangement*

[IN REPORT] Find the specifications above in the datasheet of 74LS08 and 74HC08, and fill them into the report. For pin arrangement, you can cut the image from the datasheet, and should explain the meaning of each pin.

5. Basic experiments on AND logic and inverter

5.1 AND logic

AND logic is shown in the table below, with input A and B, and output AB.

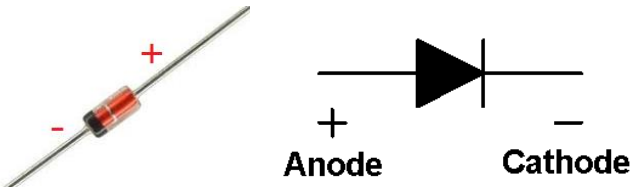
Table 2. Truth Table for AND Gate

Input		**Output**
A	**B**	**AB**
0	0	0
0	1	0
1	0	0
1	1	1

To realize the AND logic (AB), we can use different electronic components.

5.1.1 Diode-based Circuit

Wire the breadboard based on the circuit diagram below. Pay attention to the polarity of the diode. When there is a positive voltage above a certain threshold (approximated 0.7v) applied to the diode, the current can pass through it. Otherwise, the diode behaves like disconnected. The polarity is illustrated in the image below.



(a) Diode component (b) Diode symbol

Figure 3. Diode

Based on this diode, we can construct a simple AND logic circuit based on the diagram below. Wire it up in the breadboard. Use 1kΩ for R_1. Use 2 channels of SIM as the inputs, i.e. A, B. Do not use LOM for this experiment.

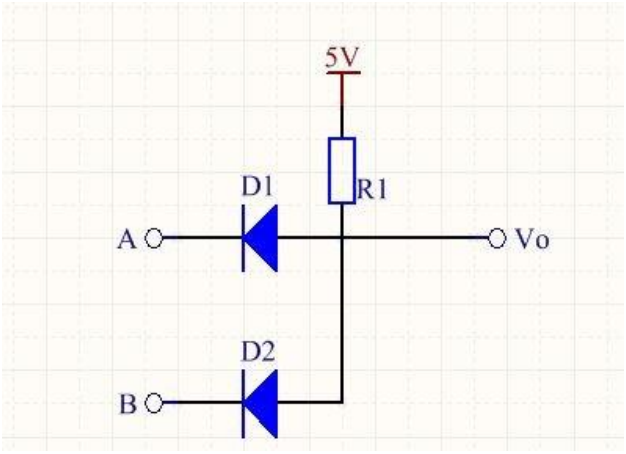


Figure 4. Circuit diagram of AND logic circuit by diodes

[QUESTION IN REPORT] Explain how the circuit above realize AND logic.

[IN REPORT] Use a multimeter to measure the voltages in the input and output pins, and fill in the form. Include this measured data in your report.

Table 3. Signal Measured for AND Based on Diodes

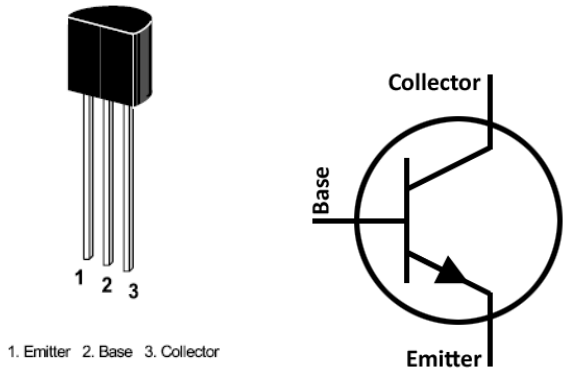
	A (V)	B (V)	V_O (V)
(0,0)			
(0,1)			
(1,0)			
(1,1)			

[QUESTION IN REPORT] Explain the voltage observed, i.e. the voltage of A, B, and V_O in the 4 cases. Hint: the diode, when activated by a positive voltage across the two ends, can assume to have a constant voltage. Measure the voltage on the activated diode, and you will have some idea.

[DEMOSTRATION - 1] Show TA your Table 3, and demonstrate 1-2 rows using your circuit.

5.1.2 Transistor-based Circuit

Transistor is formed by packaging two PN joint back-to-back. There are two types, NPN and PNP. The figure below shows one NPN transistor. A concise understanding is that, when $V_{Base\text{-}Emitter}$ is above a threshold, e.g. 0.7V in major cases, Collector and Emitter are connected; otherwise, they are disconnected.



(a) Pin arrangement (b) Circuit symbol

Figure 5. NPN Transistor

Wire the breadboard based on the circuit diagram below. You can build another simple AND circuit. R_1=R_2=33kΩ, R_3=1kΩ. Use SIM as the input.

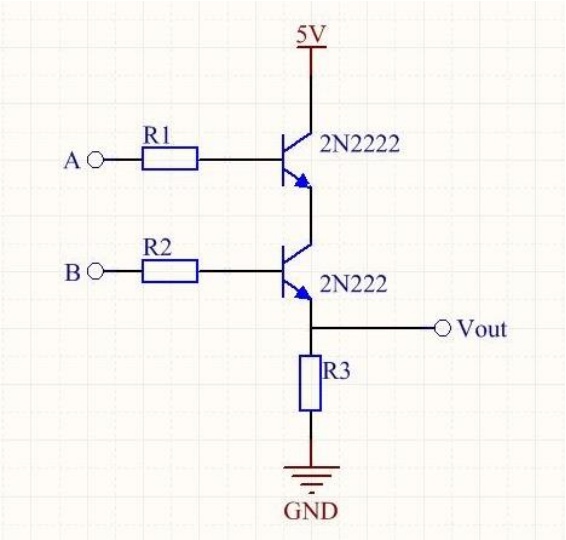


Figure 6. Circuit diagram of AND logic circuit by transistors

[IN REPORT] Use a multimeter to measure the voltages in the input and output pins, and fill in the form below. Include it in your report.

Table 4. Signal Measured for AND Based on Transistors

	A (V)	B (V)	V_O (V)
(0,0)			
(0,1)			
(1,0)			
(1,1)			

[DEMOSTRATION - 2] Show TA your Table 4, and demonstrate 1-2 rows using your circuit.

5.1.3 AND Gate

Scientists, engineers, and IC manufacturer have done a great effort in developing a large category of digital logic ICs with higher performance and improved durability. Hereafter, we will utilize them directly. 74HC08 and 74LS08 are two AND gates, in CMOS and TTL categories respectively.

5.1.3.1 74HC08

- Input-output logic
  (1) Read the datasheet of 74HC08, and understand the pin arrangement.
  (2) Select the AND gate #1. The pins to be wired include VCC, ground, 1A, 1B, and 1Y.
  (3) Connect two channels of SIM, 1 channel of LOM, with 74HC08 in the breadboard. You can select VCC=5.0V.
  (4) Investigate the logic, and verify that it is an AND gate
  (5) Measure and fill the form below

Table 5. IO for CMOS AND Gate

	1A (V)	**1B (V)**	**1Y (V)**
(0,0)			
(0,1)			
(1,0)			
(1,1)			

[IN REPORT] Draw the gate level circuit diagram. Include the data and the form above.

[DEMOSTRATION - 3] Show TA your Table 5.

- Measure the voltage transfer characteristic (VTC)

  (1) Set Vcc=6.0V based on channel 2 in the DC power supply. Vcc is generally 5.0V in digital circuit design. But here we set to 6.0V[1] for this experiment. Connect it to both Vcc pin and 1A pin of 74HC08. DO NOT output the voltage at this moment.

  (2) Use channel 1 of DC power supply as input to 1B. Initialize it with 0.0V. We will adjust the voltage in the following steps.

  (3) Connect 1Y to CH1 of the oscilloscope (NOT logic analyzer). Do not forget about the ground in the probe.

  (4) Output channel 2 and 1 of the DC power supply. Measure both 1B and 1Y by a multimeter.

  (5) Adjust the voltage of 1B based on the table below. Fill it with the data. When you find 1Y is unstable in the oscilloscope, mark it as “unstable”.

[1] In the Electrical Characteristics table of 74HC08 datasheet, the tests are carried out when Vcc= 2.0, 4.5 and 6.0V, rather than 5.0V.

Table 6. VTC Data

Rough 1B	0.0	1.0	1.9	2.1	2.3	2.5	2.7	2.8	2.9
Measured 1B									
Measured 1Y									
Rough 1B	3.0	3.1	3.2	3.3	3.4	3.6	4.0	5.0	6.0
Measured 1B									
Measured 1Y									

If you think there shall be more data point to measure, you may draw your own data table.

[IN REPORT] Draw the chip level circuit diagram (using the rectangular chip with all pins, rather than the gates) with the wire connection. Include the data table above. Plot the VTC diagram (2 dimensional diagram, with 1B and 1Y as horizontal and vertical axes.). For the part of unstable 1Y, you can mark it by a shadow area. Compare the VTC diagram with the datasheet. Explain that the V_{IH}, V_{IL} V_{OH}, V_{OL} in datasheet comply with measurement in the experiment.

- CMOS voltage levels
  Now we are ready to check the CMOS voltage levels.
  (1) Wire the circuit based on the diagram below. Do not forget V_{CC} and ground pins in the chip.

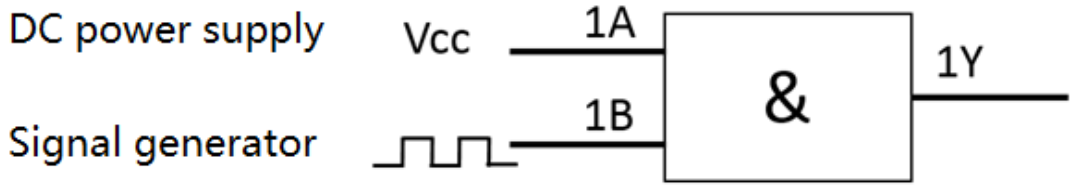


Figure 7. Circuit diagram

(2) Connect DC power supply, signal generator, and oscilloscope (CH1 for 1B and CH2 for 1Y) into the circuit. Set V_{CC}=6.0V in power supply. DO NOT output now.
(3) Use the signal generator to output a 10Hz square wave with 6.0V is for "1", and 0V for "0". Pay attention when setting the wave. Do you set it by high-low voltages, or DC voltage + offset?
(4) Output power supply, and the signal generator. Measure the observed input and output in the oscilloscope.
(5) Gradually reduce the level of high voltage of the wave sequence at appropriate steps, and reach a point that the unstable reading occurs. Record the unstable wave image and voltage of this high level.
(6) Reset high voltage to 6.0V. Gradually increase the level of low voltage at appropriate steps, and reach another unstable reading. Record the unstable wave image and voltage of this low level.

[IN REPORT] Include the necessary data and wave images needed to verify that CMOS voltage levels. Discuss if the V_{IH} and V_{IL} in datasheet comply with the

observation in this experiment. Include some typical wave images (one image each for low, high and unstable in 1Y) in steps (5)-(6).

5.1.3.2 74LS08

- Input-output logic
  (1) Connect two channels of SIM, 1 channel of LOM, and 74LS08 in the breadboard. Select V_{CC}=5.0V.
  (2) Investigate the logic, and verify that it is an AND gate
  (3) Measure and fill the form below

Table 7. IO for TTL AND Gate

	1A (V)	**1B (V)**	**1Y (V)**
(0, 0)			
(0, 1)			
(1, 0)			
(1, 1)			

[IN REPORT] Include the data and the form above.

- TTL voltage levels
  Now we can check the TTL voltage levels.
  (1) Wire the circuit similarly to experiment on CMOS voltage levels.
  (2) Connect DC power supply, signal generator, and oscilloscope (CH1 for 1B and CH2 for 1Y) into the circuit. Set V_{CC}=5.0V in power supply. DO NOT output now.
  (3) Use the signal generator to output a 10Hz square wave with 5.0V is for "1", and 0V for "0".
  (4) Output power supply, and the signal generator. Observe input and output in the oscilloscope.
  (5) Gradually reduce the level of high voltage of the wave sequence of 1B at appropriate steps, and reach a point that the unstable reading occurs. Record the unstable wave image and voltage of high level.
  (6) Reset high voltage to 5.0V. Gradually increase the level of low voltage at appropriate steps, and reach another unstable reading. Record the unstable wave image and voltage of low level.

[IN REPORT] Record the necessary data and wave images needed to verify that TTL voltage levels. Discuss if the V_{IH} and V_{IL} in datasheet comply with the observation in this experiment. Include some typical wave images (one image each for low, high and unstable in 1Y) in steps (5)-(6).

5.2 NOT Gate (Inverter)

The inverter has the logic table below. It simply inverts the input. Its logic symbol is shown below.

Table 8. Truth Table for NOT Gate

A	$\overline{\mathbf{A}}$
0	1
1	0

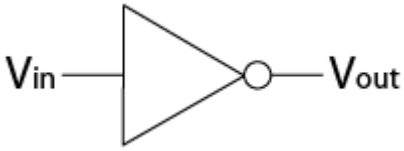


Figure 8. Inverter symbol

74HC04 contains 6 inverter gates. Its datasheet is also included in the appendix.

- Input-output logic

Design the input-output logic testing circuit. It is not difficult to design based on the AND gate steps. Pay attention to the V_{CC}.

[IN REPORT] Write down your steps. Include the data of the signals measured.

[DEMOSTRATION - 4] Show instructor or TA that your circuit works.

- Propagation delay time

Logic gates have a propagation delay time, which is the result of the limitation on switching speed or frequency at which a logic circuit can operate. The shorter the propagation delay, the higher the switching speed of the circuit and thus the higher the frequency at which it can operate.

There are two delay time, t_{PHL} specifying the time delay of output from high to low, and, t_{PLH} indicating the time delay of output from low to high. Generally, 50% points are used in both input and output signals, as shown in the figure below.

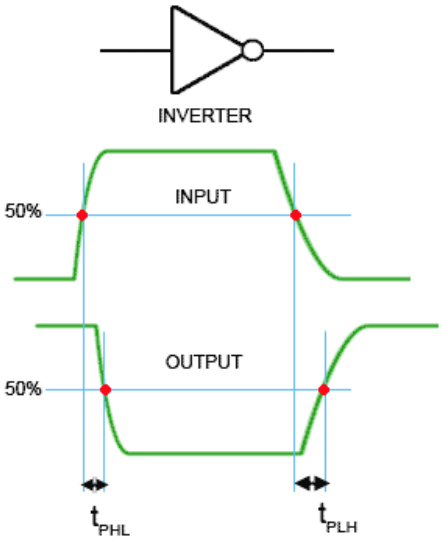


Figure 9. Inverter symbol and propagation delay

In this part, you will learn two methods to measure the propagation time.

(1) Ring Oscillator

A ring oscillator is a circuit composed of an odd number of inverter gates connected in a ring, the output of the last inverter is fed into the first one. A finite amount of time after the first input is asserted, the final output occurs, which changes the state of the first input.

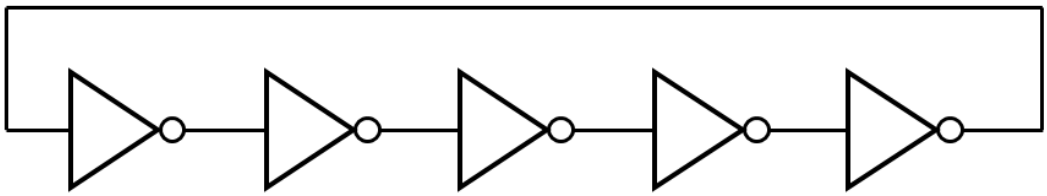


Figure 10. The circuit of a ring oscillator

Wire 5 NOT gates into the circuit. Vcc=5V. Connect the CH1 or CH2 probe to any inverter output, and you will see an oscillating signal. Measure the period as T. The propagation delay t_p = T/(2x5), which can be regarded as the mean of t_{PHL} and t_{PLH}.

[IN REPORT] Include the image of the oscillating signals. Measure T in the image and calculate t_p.

[DEMOSTRATION - 5] Show your result to instructor or TA.

[QUESTION IN REPORT] Why t_p = T/(2x5)? What happens if we take one inverter out of the ring?

(2) Measure propagation directly by an oscilloscope.

Generate a square wave at a certain frequency, and input it into a sequence of connected inverters. Measure the input and the final output by CH1 and CH2 of the oscilloscope. Try to read t_{PHL} and t_{PLH}. (Hint: to allow you to magnify the timeline, use some high frequency, e.g. 1MHz will help.)

[IN REPORT] Include the image of the oscillating signals, $t_{PHL,}$ and t_{PLH}. How do you obtain the propagation delay in this method? Compare the measured propagation delay with the datasheet.

[QUESTION IN REPORT] Based on two 74HC04 chips, what are the highest and lowest frequencies of oscillating signals which you can form?

6. Lab Report

Write the lab report comprehensively. A template has been provided on Blackboard. You can find it in the folder named ***Digital Systems Design Lab/Report Template***.

Submit the report of Lab 1 in ***PDF*** to the folder ***Digital Systems Design Lab/Report Submission/Lab 1*** on Blackboard by the deadline below:

- ***23:59, Friday, February 2nd, 2024***

Each day of late submission will result in 10% deduction in the report raw marks.

Appendix:

Components needed for this lab.

1. 20 Dupont cables (double male terminals)
2. Diode x2
3. 1 kΩ resistor x1
4. 33 kΩ resistor x2
5. 2N2222 transistor x2
6. 74HC08 x1
7. 74LS08 x1
8. 74HC04 x1

Remember to sort and return items 2-8 back to the store shelf after lab. You can keep item 1 in your box for usage in the future.

For any malfunctioning component, report to instructor or TA, and DO NOT put it back.