EIE2810 Digital Systems Design Laboratory

Laboratory Report #1

Name: Tengfei Ma

Student ID: 121090406

Date: 2024/1/29

The Chinese University of Hong Kong, Shenzhen

Lab 1 (Logic analyzer/ CMOS and TTL/ Datasheet/ Basic Experiment on AND and NOT Gates) contains the following experiments.

- Experiment A: Realizing the usage of the logic analyzer with a switch input module (SIM)
- Experiment B: Getting information of the chips from the datasheets
- Experiment C: Building and analyzing an AND Gate circuit with diodes
- Experiment D: Building and analyzing an AND Gate circuit with transistors
- Experiment E: Verifying the AND Gate effects of 74HC08 chip
- Experiment F: Verifying the AND Gate effects of 74LS08 chip
- Experiment G: Verifying the NOT Gate effects of 74HC04 chip

1. Experiment A

1.1 Results

1.1.1 Assembling the Circuit

Figure 1 shows the circuit diagram of the connection of SIM, DC (direct current) voltage source, and the logic analyzer. Figure 2 shows the finished circuit for the circuit mentioned above. Figure 3 shows the detailed connection of the circuit elements.

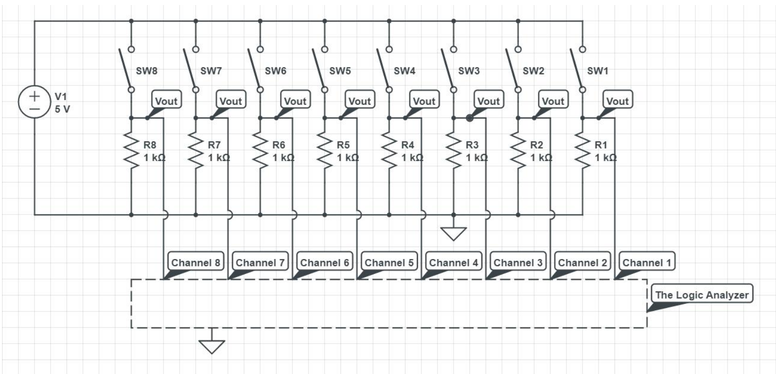

Figure 1 The Circuit Diagram for the SIM, DC Voltage Source, and Logic Analyzer

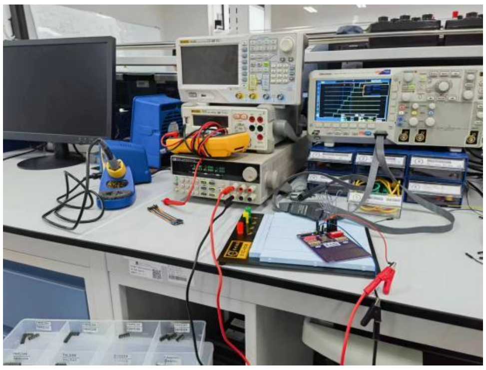

Figure 2 The Finished Circuit for the SIM, DC Voltage Source, and Logic Analyzer

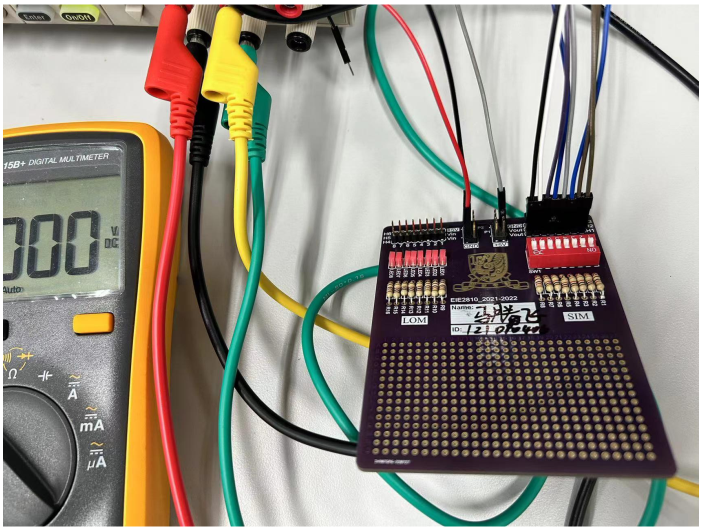

Figure 3 The Detailed Connection of the Circuit

As shown in Figure 3, the red wire connect the SIM to the DC voltage source, the blue wire connected the SIM to the ground. The wires in the red ellipse connected the V_{out}s, the output voltages of the 8 channels of the SIM, to the 8 channels of the logic analyzer, and the wires in the blue ellipse connect the logic analyzer to the ground so that the signals shown on the logic analyzer are stable and clear.

1.1.2 The Signals Shown on the Logic Analyzer

Figure 4 shows the signals shown on the logic analyzer.

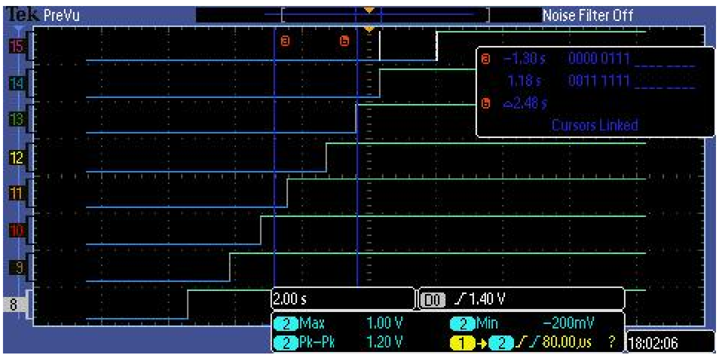

Figure 4 The Signals Shown on the Logic Analyzer

As shown in Figure 4, Channel 8 to Channel 15 of the logic analyzer were used in the experiment. When we turned on the switches for the 8 channels one by one, the signals provided by the eight channels changed from LOW to HIGH one by one, which means the SIM and the logic analyzer were both working properly.

We need to notice that there is an isolated white line segment on Channel 15. It appeared because there was a mistaken touch on the switch of Channel 15 when turning the switch of Channel 14 on.

2. Experiment B

2.1 Results

2.1.1 Get Information From the Datasheets

As required, the supply voltages, input voltages, and pin arrangements of IC 74LS08, 74HC08, and 74HC04 were found in the corresponding datasheets. The needed data are fitted in Table 1.

Table 1

		74LS08	74HC08	74HC04
Supply Voltage (V)		Typically 5.00	2 to 6	Typically 5.00
Input Voltage (V)	V_{IL}	0.8 (max.)	0.5 or 1.35 or 1.8 (max.)(2)	0.5 or 1.35 or 1.8 (max.)(6)
	V_{IH}	2.0 (min.)	1.5 or 3.15 or 4.2 (min.)(3)	1.2 or 3.15 or 4.2(min.)(7)
Output Voltage (V)	V_{OL}	0.5 or 0.4 (max.)(1)	0.1 or 0.26 or 0.33(max.)(4)	0.1 or 0.26 or 0.33(max.)(8)
	V_{OH}	2.7 (min.)	1.9 or 4.4 or 5.9 or 4.18 or 5.68 or 4.13 or 5.63(min.)(5)	1.9 or 4.4 or 3.98 or 5.9 or 5.48 or 3.84 or 5.34 (min.)(9)

Note: (max.) means the maximum value of the physics quantity, e.g. the maximum value of V_{IL}, while (min.) means the minimum value of the physics quantity, e.g. the minimum value of V_{IH}.

(1): When I_{OL} = 8mA, V_{CC} = 4.75 V, and V_{IL} = 0.8 V, temperature varies from -20℃ to +75℃, V_{OLmax} = 0.5V; when I_{OL} = 4mA, V_{CC} = 4.75 V, and V_{IL} = 0.8 V, temperature varies from -20℃ to +75℃, V_{OLmax} = 0.4V.

(2): When V_{CC} = 2.0V, no matter at normal atmospheric temperature (25°C or so) or extreme temperature(-40°C to +85°C), V_{ILmax} = 0.5V; when V_{CC} = 4.5V, no matter at normal atmospheric temperature or extreme temperature, V_{ILmax} = 1.35V; when V_{CC} = 6.0V, no matter at normal atmospheric temperature or extreme temperature, V_{ILmax} = 1.8V.

(3): When V_{CC} = 2.0V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 1.5V; when V_{CC} = 4.5V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 3.15V; when V_{CC} = 6.0V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 4.2V.

(4): When I_{OL} = 20μA, V_{in} = V_{IH} or V_{IL}, no matter under what V_{CC}, no matter at normal atmospheric temperature or extreme temperature, V_{OLmax} = 0.1V; when I_{OL} = 4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at normal atmospheric temperature, V_{OLmax} = 0.26V; when I_{OL} = 5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at normal atmospheric temperature, V_{OLmax} = 0.26V; when I_{OL} = 4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at extreme temperature, V_{OLmax} = 0.33V; when I_{OL} = 5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at extreme temperature, V_{OLmax} = 0.33V.

(5): When I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 2.0V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 1.9V; when I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 4.4V; when I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 5.9V; when I_{OL} = -4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at normal atmospheric temperature, V_{OHmin} = 4.18V; when I_{OL} = -5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at normal atmospheric temperature, V_{OHmin} = 5.68V; when I_{OL} = -4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at extreme temperature, V_{OHmin} = 4.13V; when I_{OL} = -5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at extreme temperature, V_{OHmin} = 5.63V.

(6): When V_{CC} = 2.0 V, no matter at normal atmospheric temperature or extreme temperature, V_{ILmax} = 0.5 V; when V_{CC} = 4.5 V, V_{ILmax} = 1.35 V; when V_{CC} = 6.0 V, V_{ILmax} = 1.8 V.

(7): When V_{CC} = 2.0V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 1.2V; when V_{CC} = 4.5V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 3.15V; when V_{CC} = 6.0V, no matter at normal atmospheric temperature or extreme temperature, V_{IHmin} = 4.2V.

(8): When I_{OL} = 20μA, V_{in} = V_{IH} or V_{IL}, no matter under what V_{CC}, no matter at normal atmospheric temperature or extreme temperature, V_{OLmax} = 0.1V; when I_{OL} = 4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at normal atmospheric temperature, V_{OLmax} = 0.26V; when I_{OL} = 5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at normal atmospheric temperature, V_{OLmax} = 0.26V; when I_{OL} = 4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at extreme temperature, V_{OLmax} = 0.33V; when I_{OL} = 5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at extreme temperature, V_{OLmax} = 0.33V.

(9): When I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 2.0V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 1.9V; when I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 4.4V; when I_{OL} = -20μA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, no matter at normal atmospheric temperature or extreme temperature, V_{OHmin} = 5.9V; when I_{OL} = -4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at normal atmospheric temperature, V_{OHmin} = 4.18V; when I_{OL} = -5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at normal atmospheric temperature, V_{OHmin} = 5.68V; when I_{OL} = -4mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 4.5V, at extreme temperature, V_{OHmin} = 3.84V; when I_{OL} = -5.2mA, V_{in} = V_{IH} or V_{IL}, V_{CC} = 6.0V, at extreme temperature, V_{OHmin} = 5.34V.

2.1.2 The Pin Arrangements

For 74LS08, its pin arrangement is shown in Figure 5.

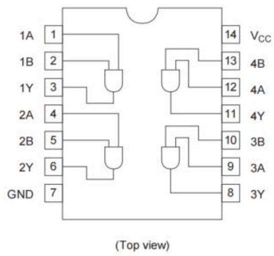

Figure 5 The Pin Arrangement For 74LS08

As shown in Figure 5, Pin 14 should be connected to the positive pole of a source while Pin 7 should be connected to the ground. There are 4 AND Gates in a single 74LS08, Pin 1 and Pin 2 are the input of the first gate, Pin 3 is the output of the first gate; Pin 4 and Pin 5 are the input of the second gate, Pin 6 is the output of the second gate; Pin 10 and Pin 9 are the input of the third gate, Pin 8 is the output of the third gate; Pin 13 and Pin 12 are the input of the fourth gate, Pin 11 is the output of the fourth gate.

For 74HC08, its pin arrangement is shown in Figure 6.

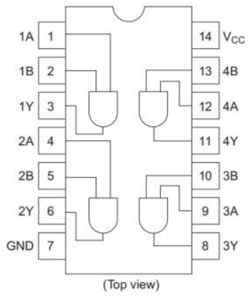

Figure 6 The Pin Arrangement for 74HC08

As shown in Figure 6, Pin 14 should be connected to the positive pole of a source while Pin 7 should be connected to the ground. There are 4 AND Gates in a single 74HC08, Pin 1 and Pin 2 are the input of the first gate, Pin 3 is the output of the first gate; Pin 4 and Pin 5 are the input of the second gate, Pin 6 is the output of the second gate; Pin 10 and Pin 9 are the input of the third gate, Pin 8 is the output of the third gate; Pin 13 and Pin 12 are the input of the fourth gate, Pin 11 is the output of the fourth gate.

For 74HC04, its pin arrangement is shown in Figure 7.

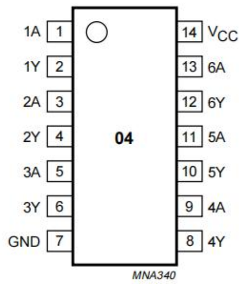

Figure 7 The Pin Arrangement for 74HC04

As shown in Figure 7, Pin 14 should be connected to the positive pole of a source while Pin 7 should be connected to the ground. There are 6 Inverters in 74HC04, Pin 1 is the input for the first inverter while Pin 2 is the output for the first inverter, Pin 3 is the input for the second inverter while Pin 4 is the output for the second inverter, Pin 5 is the input for the third inverter while Pin 6 is the output for the third inverter, Pin 9 is the input for the fourth inverter while Pin 8 is the output for the fourth inverter, Pin 11 is the input for the fifth inverter while Pin 10 is the output for the fifth inverter, Pin 13 is the input for the sixth inverter while Pin 12 is the output for the sixth inverter.

3. Experiment C

3.1 Results

3.1.1 Results of the Signal Measured for AND Gate Based on Diodes

The circuit diagram for the AND Gate based on diodes is shown in Figure 8, and the finished circuit correspond to the circuit diagram is shown in Figure 9. The node that gives V_O is called Node O in the following report.

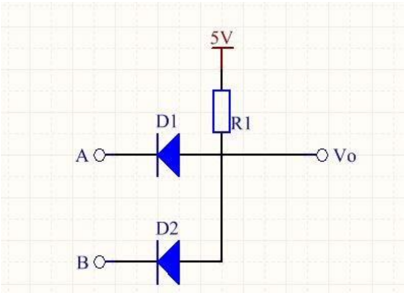

Figure 8 The Circuit Diagram for the AND Gate Based on Diodes

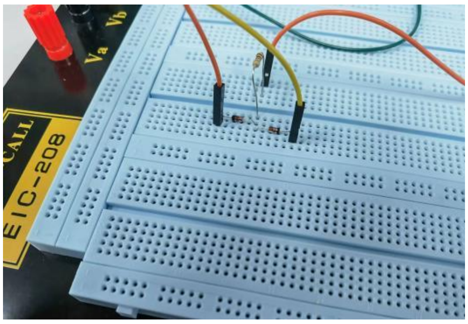

Figure 9 The Finished Circuit for the AND Gate Based on Diodes

As shown in Figure 9, the red wire is connected to Node A, the yellow wire is connected to Node B,and the orange wire is connected to Node O. Measure the voltage of the nodes mentioned above using a multimeter in different situations, fit the results in Table 2.

Table 2

	A (V)	B (V)	V_O (V)
(0,0)	1.454	1.454	2.076
(0,1)	2.172	5.00	2.816
(1,0)	5.00	2.172	2.815
(1,1)	5.00	5.00	5.00

3.2 Questions

3.2.1 Explain how the circuit above realize AND logic

When Node A and Node B both have "0" logic:

Both diodes are in positive direction. Theoretically, when in positive direction, diodes act like wires, then the current will directly goes to the ground through the diodes. So, there is no current flows through Node O, which means Node O is in “0” logic in this situation.

When Node A or Node B has “0” logic:

One of the diode is in positive direction while another one is not. Theoretically, when in positive direction, a diode act like a wire, when in negative direction, a diode acts like a open circuit. So, the current will directly goes to the ground through the diode that is in positive diode, and there is no current flows through Node O, which means Node O is in “0” logic in this situation.

When Node A and B both have “1” logic:

Both diodes are in negative direction. Theoretically, when in negative direction, diodes act like open circuits. So, the current will flow to Node O after flowing from V_{CC} to the resistor, which means Node O is in “1” logic in this situation.

3.2.2 Explain the voltage observed.

When Node A and Node B both have “0” logic:

In this situation, two diodes are both in the positive direction. First, when crossing the resistor, there exists a voltage drop. So, $V_O = 2.076$, which is smaller than 5V. Second, in the real case, the diode has a 0.7V or so activation voltage in the positive direction. So, when flowing through the diodes, there will exist a 0.7V voltage drop. As shown in Table 2, when Node A and Node B both have “0” logic, $V_A = V_B = 1.454V$, $V_O = 2.076V$. The voltage difference between Node A and Node O is 0.622V, which is quite closed to 0.7V . The voltage difference between Node B and Node O is also 0.622V, which is quite closed to 0.7V, too. So, the empirical data goes well with the theoretical data.

When Node A has “1” logic and Node B has “0” logic:

When crossing the resistor, there exists a voltage drop. So, $V_O = 2.816$, which is smaller than 5V. When Node A has “1” logic, it is connected to a 5V DC voltage source. So, $V_A = 5.00V$. In this case, the diode on Node A’s branch is in the negative direction while the diode on Node B’s branch is in the positive direction. So, Node A’s branch can be seen as open circuit while Node B’s branch acts like a wire. As mentioned above, in the real case, the diode has a 0.7V or so activation voltage in the positive direction. So, theoretically, when current flows through Node B’s branch, there will have a 0.7V voltage drop. As shown in Table 2, the voltage difference between Node B and Node O is 0.644V, which is quite closed to 0.7V. So, the empirical data goes well with the theoretical data.

When Node A has “0” logic and Node B has “1” logic:

When crossing the resistor, there exists a voltage drop. So, V_O = 2.815, which is smaller than 5V. Similar to the situation that Node A has “1” logic and Node B has “0” logic. When Node B has “1” logic, it is connected to a 5V DC voltage source. So, V_B = 5.00V. In this case, the diode on Node B’s branch is in the negative direction while the diode on Node A’s branch is in the positive direction. So, Node B’s branch can be seen as open circuit while Node A’s branch acts like a wire. As mentioned above, in the real case, the diode has a 0.7V or so activation voltage in the positive direction. So, theoretically, when current flows through Node A’s branch, there will have a 0.7V voltage drop. As shown in Table 2, the voltage difference between Node B and Node O is 0.643V, which is quite closed to 0.7V. So, the empirical data goes well with the theoretical data.

When Node A and Node B both have “1” logic:

When both Node A and Node B have “1” logic, both Node A and Node B are connected to the 5V DC voltage. So, $V_A = V_B$ = 5.00V. In this situation, two diodes are both in the negative direction, which means both branches can be seen as open circuits. So, we can remove the branches that diodes are on when analyzing V_O. Then, we have a circuit that only contains V_{CC}, resistor, multimeter, and ground. In this circuit, multimeter will show the value of V_{CC} because the multimeter can be seen as open circuit when measuring DC voltage. So, $V_O = V_{CC}$ = 5.00V. As shown in Table 2, the empirical data goes well with theoretical data.

4. Experiment D

4.1 Results

The circuit diagram for the AND Gate based on diodes is shown in Figure 10, and the finished circuit correspond to the circuit diagram is shown in Figure 11. The node that gives V_O is called Node O in the following report.

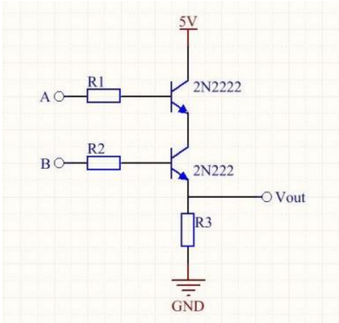

Figure 10 The Circuit Diagram for the AND Gate Based on Transistors

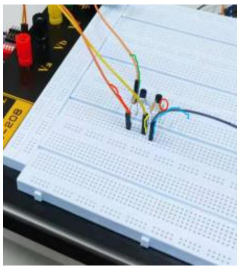

Figure 11 The Finished Circuit for the AND Gate Based on Transistors

As shown in Figure 11, the wire highlighted with green color connected the circuit to a 5V DC voltage source, the wire highlighted with red color connected SIM to Node A, the wire highlighted with yellow color connected the SIM to Node B, the wire highlighted with blue color connected the circuit to the ground. The pin signed with a red ellipse is the Node O. Use a multimeter to measure the voltage of Node A, Node B, and Node O with respect to different situations. Fit the results in Table 3.

Table 3

	A (V)	B (V)	V_O (V)
(0,0)	0	0.001	0
(0,1)	0	5.01	0.128
(1,0)	5.00	0.001	0.009
(1,1)	5.01	5.01	3.361

As shown in Table 3, if and only if two nodes both have “1” logic will V_O has a obvious voltage value, i.e., high level voltage or logic “1”.

5. Experiment E

5.1 Results

5.1.1 Output Voltage of the 74HC08 IC

The circuit diagram for testing the 74HC08 IC is shown in Figure 12, and the finished circuit correspond to the circuit diagram is shown in Figure 13.

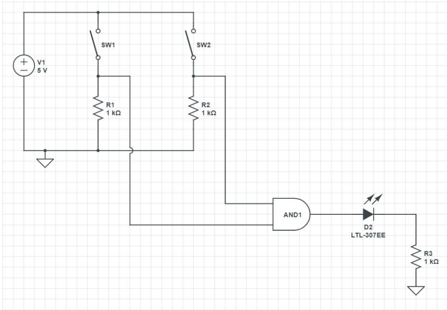

Figure 12 The Circuit Diagram for the 74HC08 Testing Circuit

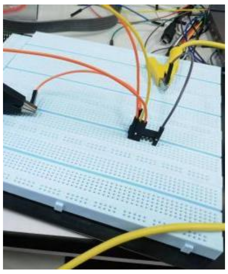

Figure 13 The Finished Circuit for the 74HC08 Testing Circuit

As shown in Figure 13, two channels of SIM are connected to Pin 1A and Pin1B of 74HC08, one channel of LOM is connected to the Pin 1Y. Pin 7 is connected to the ground and Pin 14 is connected to V_{CC} = 5V. Use a multimeter to measure the voltage of Pin 1A, Pin 1B, and Pin 1Y with respect to different situations. Fit the results in Table 4.

Table 4

	1A (V)	1B (V)	1Y (V)
(0,0)	0	0.001	0
(0,1)	0	5.01	0
(1,0)	5.00	0.001	0
(1,1)	5.01	5.00	4.90

5.1.2 Results of Measuring the Voltage Transfer Characteristics (VTC)

The chip level circuit diagram for the circuit is shown in Figure 15.

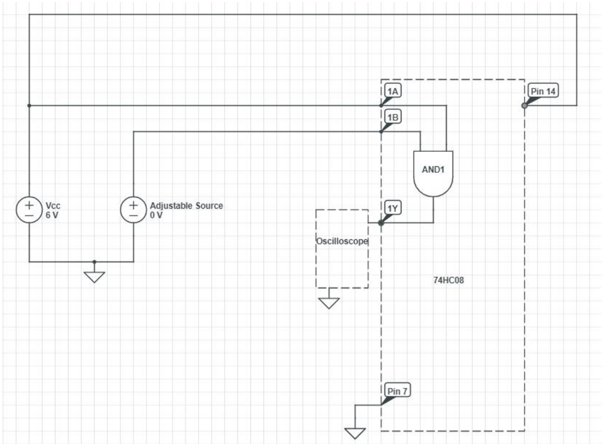

Figure 15 The Chip Level Circuit Diagram of the Circuit

The empirical VTC is obtained by setting V_{CC} = 6V and varying the input voltage of Pin 1B. The results are fitted in Table 5.

Table 5

Rough 1B (V)	0.0	1.0	1.9	2.1	2.3	2.5	2.7	2.8	2.9
Measured 1B (V)	0	1.00	1.901	2.101	2.30	2.50	2.70	2.80	2.902
Measured 1Y (V)	0.001	0.001	0	0	0	0.001	0.001	0	3.187
Rough 1B (V)	3.0	3.1	3.2	3.3	3.4	3.6	4.0	5.0	6.0
Measured 1B (V)	3.005	3.104	3.201	3.303	3.402	3.601	4.00	5.00	6.01
Measured 1Y (V)	3.331	3.369	3.438	3.471	3.554	3.662	4.004	6.01	6.01

A VTC diagram is plotted according to Table 5 and is shown in Figure 16. The unstable area is marked with shadow in Figure 16.

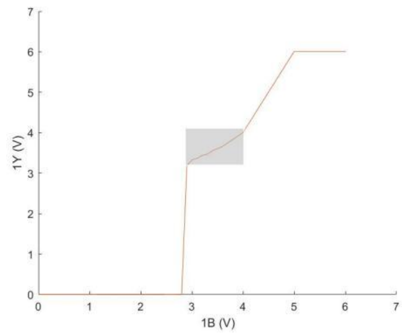

Figure 16 The VTC Diagram

As shown in Table 5 and Figure 16, (1B, 1Y) = (2.902, 3.187) is the first point that the voltage of 1Y becomes unstable, and (1B, 1Y) = (3.601, 3.662) is the last point that the voltage of 1Y is unstable. This means that empirical V_{IL} = 2.80, V_{IH} = 4.00V, V_{OL} = 0.01V, and V_{OH} = 4.004V. According to the 74HC08 datasheet, when V_{CC} = 6.0V and at normal temperature, V_{IL} = 1.8, V_{IH} = 4.2V, V_{OL} = 0.26V, and V_{OL} = 5.9V. We can see that the difference between the theoretical V_{IL} and V_{IH} is 2.4V, the difference between the theoretical V_{OL} and V_{OH} is 5.64V, the difference between the empirical V_{IL} and V_{IH} is 1.20V, and the difference between the empirical V_{IL} and V_{IH} is 4.003V. With both empirical input difference (V_{IH} - V_{IL}) and empirical output difference (V_{OH} -V_{OL}) being smaller than the theoretical ones, we can conclude that our empirical data complies with the theoretical data.

5.1.3 The Results of COMS Voltage Levels

The figure shown on the oscilloscope when V_{IL} = 0V, V_{IH} = 4.2V (theoretical V_{IH}) is shown in Figure 17, the figure shown on the oscilloscope when V_{IL} = 1.8V (theoretical V_{IL}), V_{IH} = 6.0V is shown in Figure 18, the figure shown on the oscilloscope when V_{IH} is low enough to make the figure become unstable (V_{IL} = 0V) is shown in Figure 19, and the figure shown on the oscilloscope when V_{IL} is high enough to make the figure become unstable (V_{IH} = 6.0V) is shown in Figure 20.

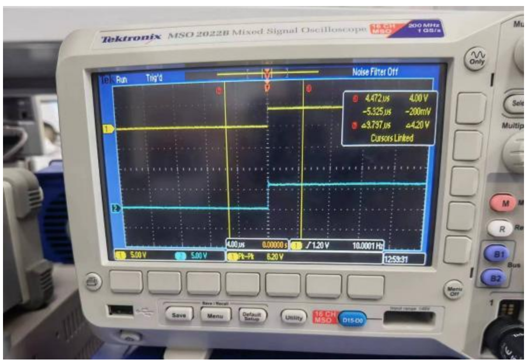

Figure 17 The Figure When V_{IL} = 0V and V_{IH} = 4.2V

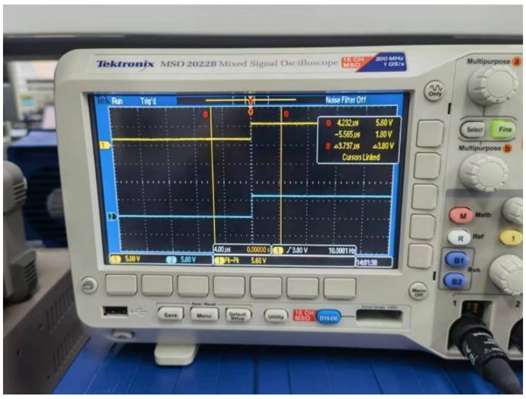

Figure 18 The Figure When V_{IL} = 1.8V and V_{IH} = 6.0V

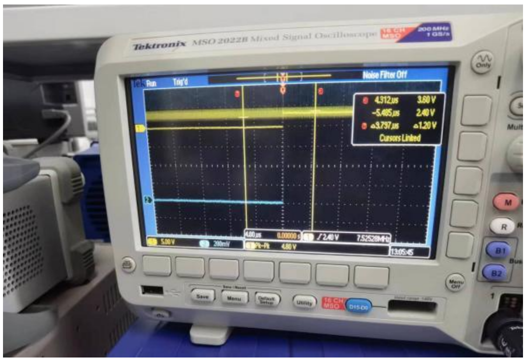

Figure 19 The Figure When V_{IH} is Low Enough to Make the Figure Become Unstable (V_{IL} = 0V)

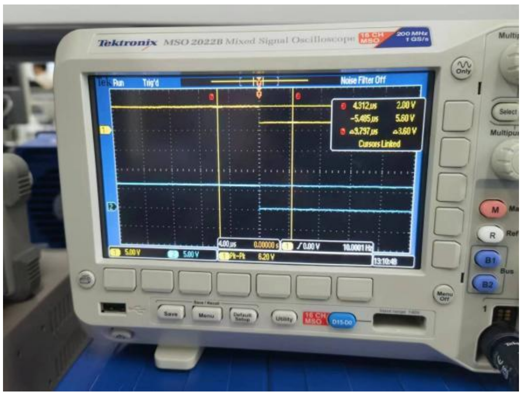

Figure 20 The Figure When V_{IL} is High Enough to Make the Figure Become Unstable (V_{IH} = 6.0V)

In the experiment, when V_{IL} = 0, the figure shown on the oscilloscope became unstable when the high level voltage generated by the signal generator dropped to 3.6V. When V_{IH} = 6.0V, the figure shown on the oscilloscope became unstable when the low level voltage generated by the signal generator rose to 2.0V. So, the empirical V_{IL} = 2.0V while empirical V_{IH} = 3.0V. The relative error for V_{IL} is 11.1% and the relative error for V_{IH} is 14.3%, which are relatively high. The possible reasons for the error are:

1) Unstable Voltage

As shown on Figure 17, the high level voltage is not exactly 6.0V. The high level voltage and low level generated by the signal generator is not stable. The voltages may shift a little bit when given to the circuit. This leads to the different testing condition, which means the results may be different.

2) Different Temperature

The testing temperature given by the datasheet is 25℃, while the temperature when the experiment was conducted was not exactly 25℃. This leads to the different testing condition, which means the results may be different.

3) Not Ideal Elements

Although the tools and circuit elements we used were pretty accurate, they were not ideal. This means that it is hard to get exactly the same results as the datasheet.

6. Experiment F

6.1 Results

6.1.1 Results of Input-Output Logic

The circuit diagram for testing the 74LS08 IC is shown in Figure 21, and the finished circuit correspond to the circuit diagram is shown in Figure 22.

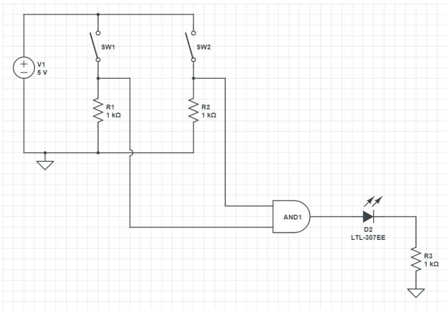

Figure 21 The Circuit Diagram for the 74LS08 Testing Circuit

Figure 22 The Finished Circuit for the 74LS08 Testing Circuit

As shown in Figure 22, two channels of SIM are connected to Pin 1A and Pin1B of 74LS08, one channel of LOM is connected to the Pin 1Y. Pin 7 is connected to the ground and Pin 14 is connected to V_{CC} = 5V. Use a multimeter to measure the voltage of Pin 1A, Pin 1B, and Pin 1Y with respect to different situations. Fit the results in Table 6.

Table 6

	1A (V)	1B (V)	1Y (V)

(0,0)	0.105	0.108	0.080
(0,1)	0.213	5.01	0.580
(1,0)	5.01	0.210	0.080
(1,1)	5.01	5.01	3.481

As shown in Table 6, if and only if two nodes both have “1” logic will Pin 1Y has a obvious voltage value, i.e., high level voltage or logic “1”.

6.1.2 The Results of TTL Voltage Levels

The figure shown on the oscilloscope when V_{IL} = 0V, V_{IH} = 2.0V (theoretical V_{IH}) is shown in Figure 24, the figure shown on the oscilloscope when V_{IL} = 0.8V (theoretical V_{IL}), V_{IH} = 5.0V is shown in Figure 25, the figure shown on the oscilloscope when V_{IH} is low enough to make the figure become unstable (V_{IL} = 0V) is shown in Figure 26, and the figure shown on the oscilloscope when V_{IL} is high enough to make the figure become unstable (V_{IH} = 5.0V) is shown in Figure 27.

Figure 24 The Figure When V_{IL} = 0V and V_{IH} = 2.0V

Figure 25 The Figure When V_{IL} = 0.8V and V_{IH} = 5.0V

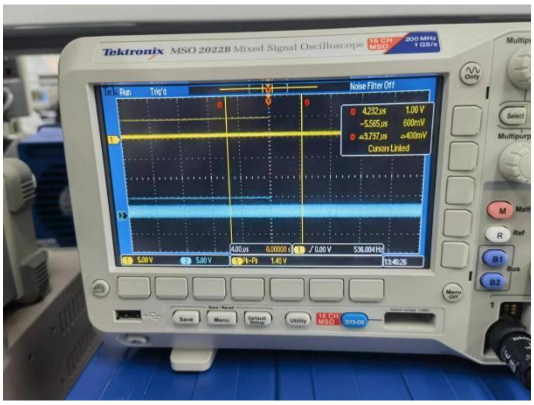

Figure 26 The Figure When V_{IH} is Low Enough to Make the Figure Become Unstable (V_{IL} = 0V)

Figure 27 The Figure When V_{IL} is High Enough to Make the Figure Become Unstable (V_{IH} = 5.0V)

In the experiment, when V_{IL} = 0, the figure shown on the oscilloscope became unstable when the high level voltage generated by the signal generator dropped to 1.05V. When V_{IH} = 5.0V, the figure shown on the oscilloscope became unstable when the low level voltage generated by the signal generator rose to 0.8V. So, the empirical V_{IL} = 0.8V while empirical V_{IH} = 1.05V. The relative error for V_{IH} is 47.5%, which are relatively high. The possible reasons for the error are:

1) Unstable Voltage

As shown on Figure 24, the high level voltage is not exactly 2.0V. The high level voltage and low level generated by the signal generator is not stable. The voltages may shift a little bit when given to the circuit. This leads to the different testing condition, which means the results may be different.

2) Different Temperature

The testing temperature given by the datasheet is 25℃, while the temperature when the experiment was conducted was not exactly 25℃. This leads to the different testing condition, which means the results may be different.

3) Not Ideal Elements

Although the tools and circuit elements we used were pretty accurate, they were not ideal. This means that it is hard to get exactly the same results as the datasheet.

7. Experiment G

7.1 Design

The circuit diagram designed for the testing circuit is shown in Figure 28.

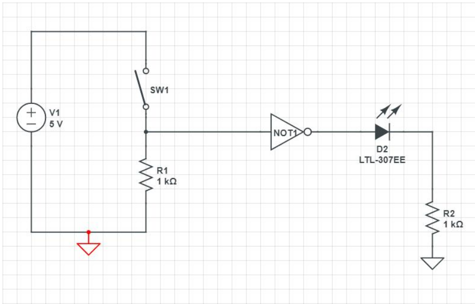

Figure 28 The Circuit Diagram Designed for the NOT Gate Testing Circuit

7.2 Results

7.2.1 The Results for Testing the Input-Output Logic

The testing circuit was built according to Figure 28 and the finished circuit is shown in Figure 29.

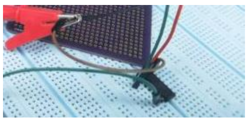

Figure 29 The Finished Circuit for the NOT Gate Testing Circuit

As shown in Figure 29, one channel of SIM is connected to Pin 1A of 74HC04, one channel of LOM is connected to the Pin 1Y. Pin 7 is connected to the ground and Pin 14 is connected to V_{CC} = 5V. Use a multimeter to measure the voltage of Pin 1A and Pin 1Y with respect to different situations. Fit the results in Table 7.

Table 7

	1A (V)	1Y (V)
Input Logic “1”	4.99	0.001
Input Logic “0”	0	4.89

As shown in Table 7, when the input has a high level voltage, the output has a low level voltage, when the input has a low level voltage, the output has a highlevel voltage. This means we successfully verified the NOT Gate function of 74HC04.

7.2.2 The Results of Propagation Delay Time

7.2.2.1 Measuring the Propagation Delay Time Using Ring Oscillator

Put 5 inverters into output-to-input order, set V_{CC} to 5.0V. Connect the channel 1 of the oscilloscope to any inverter output, and observe the oscillating signal shown on the oscilloscope. The oscillating signal of a ring oscillator is shown in Figure 31.

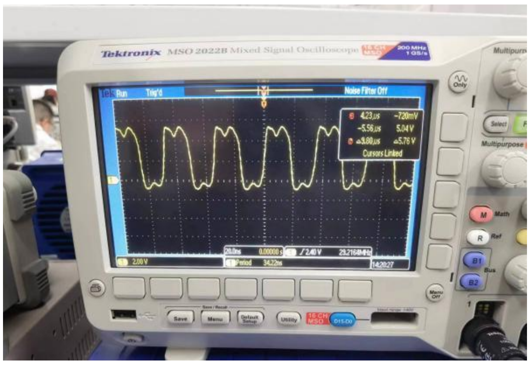

Figure 31 The Oscillating Signal of a Ring Oscillator

As shown on Figure 31, the period for the oscillation signal is 34.22ns, that is, T = 34.22ns. Using the relationship equation $t_p = T/(2\times5)$, we can compute that t_p = 3.422ns.

7.2.2.2 Measuring the Propagation Delay Using Oscilloscope

Put 5 inverters into output-to-input order, set V_{CC} to 5.0V. Use the signal generator generate a square wave with 10MHz frequency as input signal, measure the input using channel 1 of the oscilloscope and measure the output using channel 2 of the oscilloscope. Let the oscilloscope measure the t_{PHL} and t_{PLH}. The results are shown in Figure 32.

Figure 32 The Input Signal, Output Signal, t_{PHL}, and t_{PLH} Shown on the Oscilloscope

As shown in Figure 32, t_{PHL} = 18.86ns, and t_{PLH} = 22.27ns. The propagation delay t_p can be regarded as the mean of t_{PHL} and t_{PLH}. Then the empirical propagation delay t_p

= 20.565ns ≈ 20.57ns. According to the datasheet, the typical propagation delay should be 7ns, which is much smaller than the empirical one. The possible reasons for the error are:

1) Incorrect Testing Condition

According to the datasheet, the testing condition should be V_{CC} = 6.0V and 25℃ temperature. However, the V_{CC} used in the experiment was 5.0V and the temperature was not exactly 25℃. Having different testing condition, the results are likely to have relatively large biases.

2) The Oscilloscope is Not Accurate Enough

During the experiment, there were question mark near the data sometimes, which means the machine was not sure about the data. In other words, the oscilloscope was not accurate enough to give us exact results. This will lead to biased data.

3) Not Ideal Elements

Although the tools and circuit elements we used were pretty accurate, they were not ideal. This means that it is hard to get exactly the same results as the datasheet.

7.3 Questions

7.3.1 Why t_p = T/(2*5) ? What happens if we take one inverter out of ring?

First, the ring oscillator will give us a periodical signal because the output voltage would change its voltage level every time the signal passes a sequence of inverters. So, T is the time that signal passes through a whole sequence of the inverters, which means to get the propagation delay, we need to divide T by 5 first. Second, T/5 is actually a combination of t_{PLH} and t_{PHL}. The propagation delay t_p can be regarded as the mean of t_{PHL} and t_{PLH}. So, we need to divide T/5 by 2 to get t_p. Then we have the relationship: $t_p = T/(2\times5)$.

If we take one inverter away from the ring, the relationship would become $t_p = T/(2\times4)$. However, with even number of inverters in the ring, it is hard for us to observe a periodical signal on the oscilloscope because the signal will not change its voltage level after passing four times of the inverter.

7.3.2 Based on two 74HC04 chips, what are the highest and lowest frequencies of oscillating signals which you can form?

$$f = \frac{1}{T} = \frac{1}{((t_{PHL} + t_{PLH}) \times (\text{number of inverters}))}$$

To generate highest frequency, we need to have smallest T. To have smallest T, we need to reduce the number of inverter that the signal passes. So, we only need to connect the input pin and output pin of one of the inverters, we can have the highest frequency. Use t_p from the datasheet, we can know that the highest frequency $f_h = \frac{1}{1\times2\times7} = \frac{1}{14} \approx 0.0714$(Hz).

To generate lowest frequency, we need to have biggest T. To have biggest T, we need to increase the number of inverter that the signal passes. So, we only need to connect the output pins to input pins one by one for all of the inverters, we can have the lowestest frequency. Use t_p from the datasheet, we can know that the highest frequency $f_h = \frac{1}{12\times2\times7} = \frac{1}{168} \approx 5.95 \times 10^{-3}$(Hz).

8. Conclusion

In conclusion, the lab provided an excellent opportunity to learn about the basic building blocks of digital circuits. Through this lab, I have acquired a deeper understanding of the properties and differences between TTL and CMOS logic families, the process of reading and understanding datasheets, and how to build simple circuits using logic gates. I have also gained experience using various testing equipment, such as the oscilloscope and logic analyzer, to capture and analyze digital signals in the circuit. The lab was organized in a way that allowed us to observe the process of building a digital circuit from the ground up. Starting with simple diode-based AND gate circuits, we moved on to more complex transistor-based AND gates and, finally, explored the behavior of integrated circuit-based AND and NOT gates. Through these experiments, we gained a better understanding of how the various components of a digital circuit interact with each other to produce a desired output.