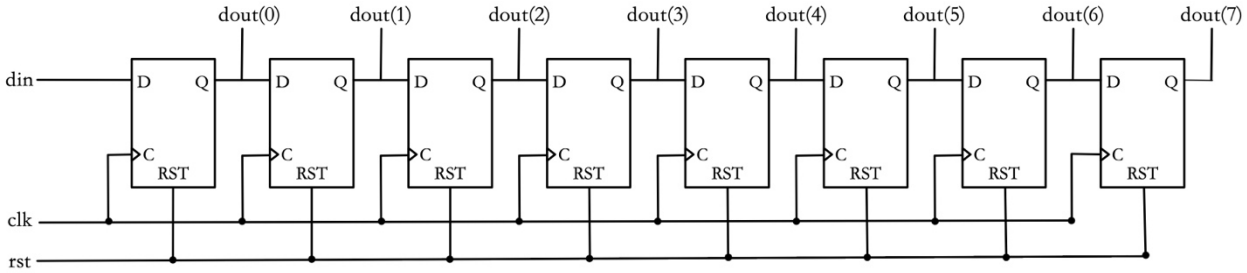
EIE2050 Digital Logic and Systems

Project: Serial-in-parallel-out shift register

- **Objectives and Aims:**
  - Get familiar with the hardware programming language VHDL
  - Study the use of different architectural design methods
  - Study the use of combinational and sequential logics

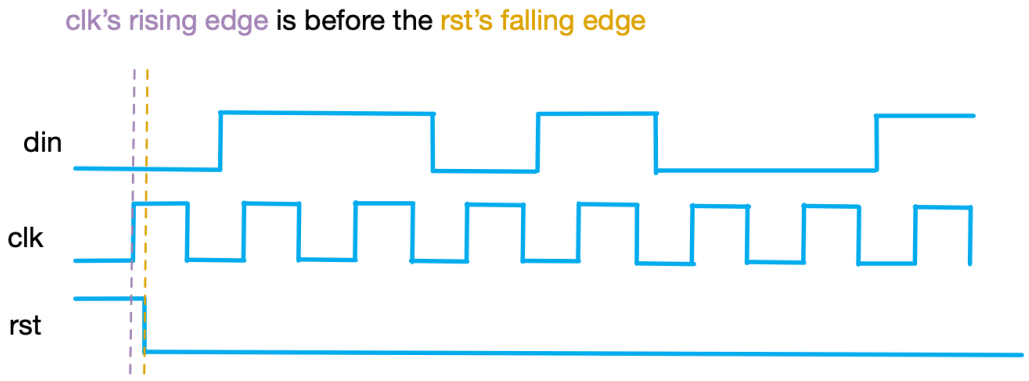
- **Exercise:** In this lab, you need to implement a **serial-in-parallel-out (SIPO) shift register**, which is composed of **8 D-Flip-Flops (D-FF)** as follows:



  - The SIPO shift register allows serial input (one bit after the other through a single data line **`din`**) and produces a parallel output (through **`dout(0)`** to **`dout(7)`**).
  - When **`rst`** equals to 1, all the **`dout(s)`** are reset to be zero.
  - Otherwise (when **`rst`** equals to 0), at every rising edge of **`clk`**, the signal of **`din`** is shifted into the "leftmost" D-FF; meanwhile the signal kept by each D-FF is shifted to the D-FF on its right; and the signal kept by the "rightmost" D-FF is shifted out from the SIPO shift register.

- **Requirements:**
  - Implement a serial-in-parallel-out (SIPO) shift register, which is composed of 8 D-Flip-Flops (D-FF), using the `structural design` (`port map`).
    - That is, implement the D-Flip-Flop first, and then use D-Flip-Flop to implement the SIPO shift register.
    - Write down a testbench to verify the SIPO function (waveform diagram). An input waveform diagram as below is provided for

reference. Note that the **`clk`**'s rising edge should be before the **`rst`**'s falling edge to eliminate uncertain outputs (U).



- Submission Rule:
  - Submit your (1) source code(s) (.vhd), (2) testbench (.vhd), and (3) the behavior simulation result (a screen shot) to BB
- Deadline: April 19, 2023