# TENZIN NORPHEL

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## EDUCATION

**University of California, Berkeley** Berkeley, CA
*Bachelor of Science in Electrical Engineering and Computer Science* *Expected Dec 2025*

- **Coursework:** Application-Specific Integrated Circuits, Machine Structures, Integrated-Circuit Devices, Microfabrication, Signal and Systems, Control Systems, Discrete Math, Robotics, IoT, Cybersecurity

## TECHNICAL SKILLS

- **Hardware Design & ASIC:** Verilog (HDL), RTL Design, Cadence Innovus, Skywater 130nm PDK, Floorplanning, Place & Route, Timing Closure, Synthesis, DRC Verification, System Verilog
- **PCB & Embedded:** KiCad, Altium, Schematic Capture, Multi-layer PCB Layout, Signal Integrity, Power Integrity, Microcontroller Programming
- **Programming & Tools:** Python, C/C++, Java, RISC-V Assembly, OpenMP, Git, GDB, Valgrind, MATLAB, ROS
- **Semiconductor:** Sentaurus TCAD (Synopsys), CAD Design, Control Systems, Computer Architecture

## EXPERIENCE

**Product & Research Intern** June 2025 – Aug 2025
*Custex Inc. – Berkeley SkyDeck ACE Program* *Remote*

- Developed Python-based Content Risk Analyzer detecting high-risk text patterns for AI-powered cybersecurity platform
- Implemented detection pipelines with CSV logging and dashboards, reducing security threat response time by 40%
- Created automated alert systems for recurring high-risk patterns, enhancing real-time threat monitoring

## TECHNICAL PROJECTS

**3-Stage Pipelined RISC-V CPU – EECS 151 ASIC Project** October 2025

- Designed 3-stage pipelined RISC-V CPU supporting RV32I instruction set and CSR operations in Verilog with ALU, pipeline control logic, and hazard resolution units
- Integrated processor with direct-mapped cache and SRAM memory interface, optimizing instruction/data access latency
- Performed backend synthesis, floorplanning, and timing closure using Cadence Innovus with Skywater 130nm technology, achieving target clock frequency through critical path optimization
- Verified design using System Verilog assertions and comprehensive testbenches

**Custom MIDI Keyboard PCB Design – Personal Project** October 2025

- Designed and fabricated custom MIDI keyboard PCB with microcontroller-based key scanning and USB communication
- Created multi-layer PCB layouts in KiCad with optimized component placement, footprints, pads, and via routing
- Implemented grounding strategies, decoupling capacitors, and power distribution for signal integrity and EMI reduction
- Performed board bring-up and debugging using oscilloscope and multimeter to verify signal paths

**5-Stage Pipelined RISC-V CPU Design** July 2024

- Designed 5-stage pipelined RISC-V processor (IF, ID, EX, MEM, WB) in Logisim supporting all instruction formats (R, I, S, B, U, J)
- Built ROM-based microcode control logic decoding opcodes, funct3, and funct7 into control signals (PCSel, ImmSel, RegWEn, BrUn, ASel, BSel, ALUSel, MemRW, WBSel)
- Implemented data forwarding and hazard detection units to resolve hazards, optimizing pipeline throughput