Tenzin Norphel

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Education

University of California, Berkeley *Expected December 2025*
BS in Electrical Engineering and Computer Science

- **Coursework:** Machine Structures, Discrete Math and Probability, Integrated-Circuit Devices, Introduction to Robotics, Signal and Systems, Microfabrication, Control system and feedback, Robot Manipulation and Vision, and Artificial Intelligence

Skills

CAD (Computer Aided Design), MATLAB, ROS (Robot Operating System), Python, Sentaurus (Synopsys), C++, C, Java, Git, RISC-V, MuJoCo (Multi-Joint dynamics with Contact), Keysight's EasyEXPERT(GUI-based interface for device setup/device characterization)

Projects

Control System Engineer *Berkeley, CA*
Visual Servoing & Grasping Control *April 2025*

- Developed PD-based joint-space and torque controllers for 7-DOF Sawyer arm to track AR tags. Tuned controller gains to reduce trajectory error and motion jitter.
- Designed IK solver and grasp synthesis for Allegro Hand in MuJoCo using Levenberg–Marquardt and force closure metrics.

Process Integration Engineer *Berkeley, CA*
Microfabrication Technology *April 2025*

- Fabricated NMOS devices from bare silicon wafers over a 12-week cleanroom process flow.
- Performed photolithography, gate oxidation, ion implantation, contact etch, and metal deposition.
- Characterized resistors, capacitors, MOS capacitors, and long-channel NMOS transistors.
- Used 4155B semiconductor analyzer and 4284A LCR meter for I-V and C-V measurements.

Robotics System Developer *Berkeley, CA*
TurtleBot Path Planning & State Estimation *March 2025*

- Built RRT, sinusoidal, and Dubins path planners for a unicycle-model TurtleBot.
- Implemented Lyapunov-based tracking controller in ROS. Applied Kalman Filter (KF) and Extended Kalman Filter (EKF) for state estimation and compared MSE vs. dead reckoning.

Semiconductor Device Designer *Berkeley, CA*
N-MOSFET Design Project *Oct 2024*

- Utilized semiconductor device simulation software (Synopsys' Sentaurus package) to design an N-channel Si MOSFET with gate length, LG = 25 nm (relevant for the "20 nm generation" of CMOS technology).
- Met specified performance requirements within constraints using Synopsys (Sentauraus Package)

Robotics Software Engineer *Berkeley, CA*
TurtleBot Maze Solver *Oct 2024*

- Given an arbitrary maze, Turtlebot 2.0 has the capability to traverse through the maze, scan the maze for its most optimal path from a starting point S, and save its layout into memory using ROS (Robotic Operating System) in Python.

CPU Designer *Berkeley, CA*
CS61CPU *March 2024*

- Developed a processor capable of executing RISC-V machine code, implementing instruction fetch, decode, execute, memory access, and write-back stages.
- Integrated pipelining techniques to improve performance and increase throughput.
- Built the CPU from basic logic gates and registers, demonstrating a deep understanding of computer architecture.

Work Experience

Project Intern *Remote*
NASA - MCA (Mission Concept Academy) *May 2021*

- Used Siemen CAD tools to design a Rover and RIMFAX payload deployment system for lunar landing
- Planned how to descent maneuver and vehicle design specific for the moon's environment with low gravitational force and its surface.