Tenzin Norphel

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Education

University of California, Berkeley *Expected December 2025*
Bachelor of Science in Electrical Engineering and Computer Science

- **Coursework:** Machine Structures, Discrete Math and Probability, Integrated-Circuit Devices, Introduction to Robotics, Signal and Systems, Microfabrication, Control system and feedback, Robot Manipulation and Vision, and Artificial Intelligence, Internet Architecture/Internet of things (IoT), Cybersecurity, Application-Specific Integrated Circuits (An introduction to digital and system design)

Skills

- Verilog (HDL), Application-Specific Integrated Circuits (ASIC), RTL Design (Register Transfer Level), Cadence/Innovus, Floorplanning and Place & Route (P&R)
- PCB Design (schematic capture, layout, DRC verification) using KiCad and Altium
- MATLAB, ROS (Robot Operating System), Python, Sentaurus TCAD (Synopsys), C/C++, Java
- RISC-V Assembly, OpenMP, Git, GDB, Valgrind
- CAD (Computer-Aided Design), Multi-joint Dynamics with Contact, Control Systems, IoT (Internet of Things), and Cybersecurity/Cryptography

Experience

Product & Research Intern *Remote*
Custex Inc. — Berkeley SkyDeck ACE Program *June- Aug 2025*

- Developed a Python-based Content Risk Analyzer that detects and categorizes high-risk text, including self-harm, abuse, and violent language.
- Worked on keyword-based detection pipelines, implemented structured logging in CSV, and built visual dashboards to track flagged activity over time. Created rules for identifying recurring high-risk patterns and generating automated alerts.

Projects

3-Stage Pipelined RISC-V CPU — EECS 151 ASIC Project *Berkeley, CA*
Ongoing (Fall 2025)

- Designed and implemented a 3-stage pipelined RISC-V CPU supporting the base integer instruction set and CSR operations in Verilog. Built a functional ALU, pipeline control logic, and hazard resolution units; verified operation using System Verilog assertions and custom testbenches.
- Integrated the processor with a direct-mapped cache and SRAM-based memory interface to optimize instruction/data access latency.
- Used Skywater 130nm technology for backend synthesis, floorplanning, and timing closure in Cadence Innovus. Improved understanding of RTL design, hazard mitigation, and physical design flow, contributing to efficient low-latency RISC-V system architecture.

PCB Design Engineer *Berkeley, CA*
Custom MIDI Keyboard — Personal Project *August 2025*

- Designed and fabricated a custom MIDI keyboard PCB integrating microcontroller-based key scanning and USB communication.
- Interpreted circuit schematics and created multi-layer PCB layouts in KiCad, defining component footprints, pads, and vias for optimized routing and manufacturability.
- Implemented grounding and decoupling strategies to minimize signal noise and ensure power integrity across the digital and analog domains. Performed board bring-up, continuity testing, and debugging using an oscilloscope and multimeter to verify correct signal paths and component operation.

5-stage pipeline RISC-V CPU Design *Berkeley, CA*
July 2024

- Designed and implemented a fully functional 5-stage pipelined RISC-V processor (IF, ID, EX, MEM, WB) in Logisim.
- Built complete control logic using a ROM-based microcode table and priority encoders to decode opcodes, funct3, and funct7 into control signals (PCSel, ImmSel, RegWEn, BrUn, ASel, BSel, ALUSel, MemRW, WBSel).
- Optimized the logic flow by fixing forwarding, hazard detection, PCSel branch redirection logic, and immediate generation for all RISC-V instruction formats. Integrated ALU, register file, DMEM/IMEM, branch comparator, and pipeline registers using basic gates, muxes, and combinational logic.