

**University POLITEHNICA of Bucharest**

Faculty of Electronics, Telecommunications and Information Technology

# Project 1

## Negative Voltage Regulator

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## 1. Project requirements

It is required to design a negative voltage regulator with the following parameters:

**N = 17**

- Negative supply voltage between -30 ÷ -26 [V]
  - Negative programmable output voltage between -22 ÷ -20 [V]
  - The output current through the load between 0 ÷ 26 [mA]
  - Shortcircuit protection of the output terminals with foldback current limiting circuit
  - $S = \frac{\Delta V_i}{\Delta V_o} |_{RL} \geq 53$
  - $R_L = \frac{V_{outmax}}{I_{outmax}} = \frac{22V}{26mA} = 846 \Omega$
  - The output impedance of the regulator  $R_0 \leq 2 \Omega$
- 
- PCB dimensions: 40mm x 40mm;
  - Board is double sided, FR4, thickness of the copper foil 18 $\mu$ m, board thickness 1.5mm;
  - All components are placed on the TOP side;
  - There will be used only SMD passive components in 0805 packages;
  - There will be used only SMD FET, MOSFET and bipolar transistors (SOT-23, D-PAK packages);
  - Round test points (maximum 5) – justified by the test plan;
  - The design origin (0,0) must be placed in the bottom left corner of the PCB, all coordinates must have positive values;
  - A clearance of 1mm will be kept from the edges of the board;
  - The board will be provided with 2 global fiducial markers on the TOP layer, at a distance of 200mils from the edges of the board, conveniently placed; these markers will also exist on the Solder Paste Top layer (overlapping those on the TOP); they will be used when aligning the stencil with the PCB. The fiducial marker will be a circle with a minimum diameter of 1mm on the respective layer, located in a circular space with a minimum diameter double the inner circle, in which there will be nothing on any layer;
  - Careful attention should be paid to the Silk Screen TOP layer; the silkscreen should not appear on the pads of the components;
  - A mechanical layer will be generated. This will contain the board outline, the drill drawing, the drill chart/table, drill legend, the layer stack-up and mechanical information for PCB manufacturing.
  - The dimension quotes of the PCB shouldn't appear on the TOP layer. If these quotes exist, they should appear on a non-electrical mechanical layer;

- The board will be provided with identification information about the designer (Last Name, First Name, Group, PDCE I 2022-2023).

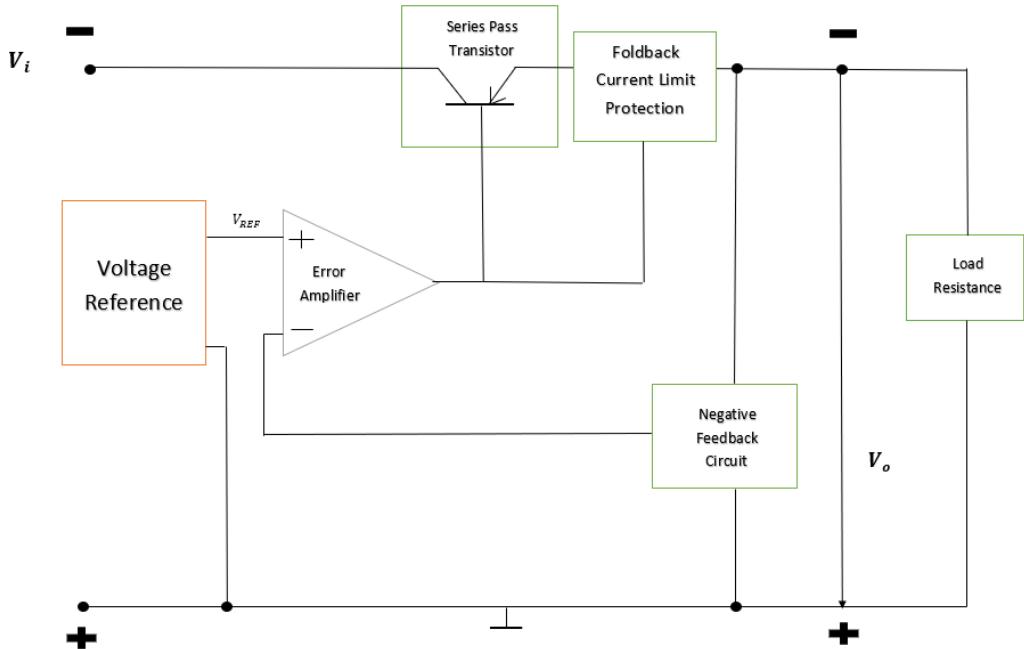
The Gerber files (274x standard) and the Excellon file should contain the following information:

- board outline;
- electrical layer TOP;
- electrical layer BOTTOM;
- non-electrical layer Silk Screen Top;
- non-electrical layer Solder Mask Top;
- non-electrical layer Solder Mask Bottom;
- non-electrical layer Solder Paste Top;
- the aperture list and the drilling file.

The following widths and spacings are given for the routing layers:

- 1A current – 28mils;
- Few hundreds mA currents - 22mils;
- Signal - 18mils;
- Spacing - 12mils;
- The via hole diameter is 0.4mm.

## 2. The block diagram of the circuit



(Fig. 2.1)

The Negative Voltage Regulator in this diagram presents an *Error Amplifier*, which has the role of comparing the reference voltage  $V_{REF}$  and the feedback voltage from the *Negative Feedback Circuit*, to ensure that the output voltage  $V_o$  is maintained at the required voltage.

To these, it is added a *Foldback Current Limit Protection*, which protects the regulator from damage by overcurrent in situations such as shorting the output with a wire.

A *Series Pass Transistor* is connected to the Error Amplifier, so that whenever the output voltage changes due to variation of the input voltage or load current, that change in output voltage (also called “error voltage”) is amplified and applied as negative feedback to the series element so that the voltage drop across the series pass element changes in such way as to compensate for the initial change in voltage.

At last, a *Load Resistance* is also added to the circuit.

### 3. Schematic diagram of the circuit (Fig. 3.1)

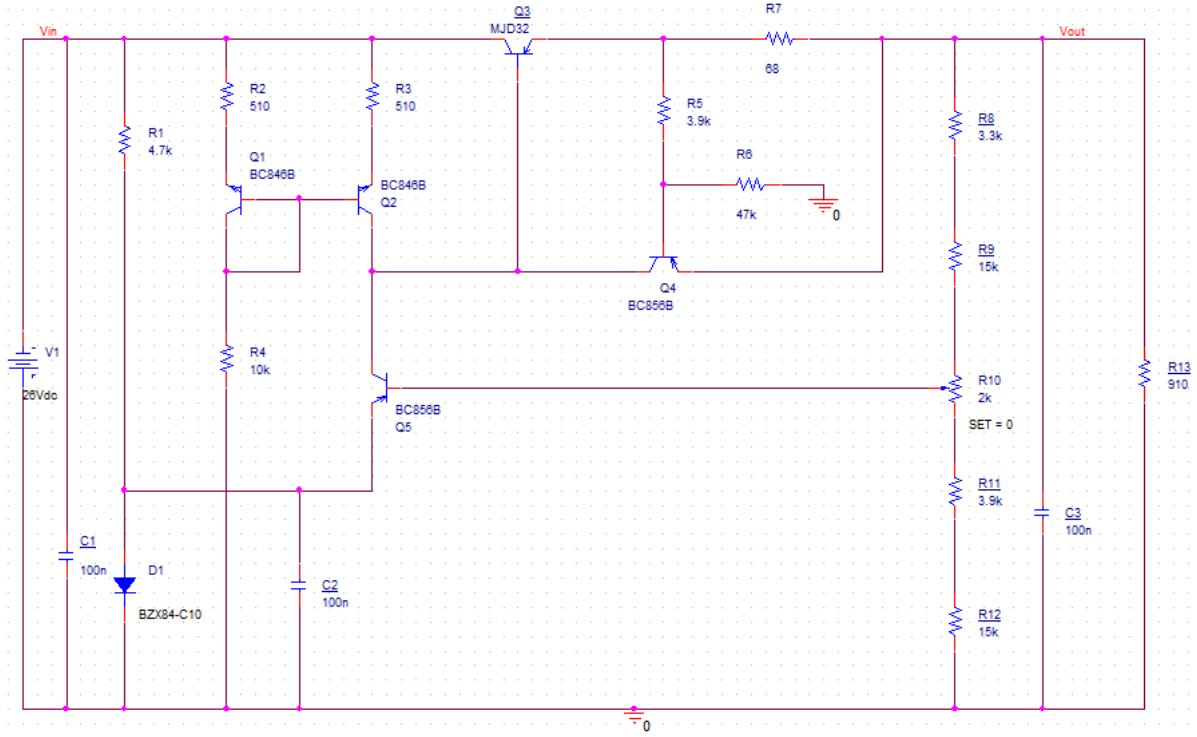


Fig. 3.1

#### Subblocks of the circuit:

- *Voltage reference:* Zener Diode D1 and resistance R1
- *Error Amplifier:* transistor Q5, the current mirror with transistors Q1 and Q2, and resistances R2, R3 and R4
- *Series Pass Transistor:* transistor Q3
- *Foldback Current Limit Protection:* transistor Q4 and resistances R5, R6, R7
- *Negative Feedback Circuit:* resistances R8, R9, R11, R12 and potentiometer R10
- *Load Resistance:* resistance R13

I also added 3 ceramic capacitors, C1, C2, C3, all having the value of 100 nF. They are used to filter some of the noise from Vsupply (Vin), Vref (the voltage reference) and Vout.

### The Voltage Reference (Fig. 3.2)

The Voltage Reference consists of a Zener Diode D<sub>1</sub> and a resistance R<sub>1</sub>.

The chosen Diode is of type BZX84-C10, which has a Zener voltage V<sub>Z</sub> = 10V and I<sub>Zmin</sub> = 5mA.

The value for R<sub>1</sub> = 4.7 kΩ was chosen to have the current flowing through D<sub>1</sub> greater than I<sub>Zmin</sub>.

The resistance R<sub>1</sub> was also chosen and added to the circuit to help and keep the current flowing through the diode D<sub>1</sub> constant.



Fig. 3.2

### The Error Amplifier (Fig. 3.3)

It is made of the current mirror Q<sub>1</sub>, Q<sub>2</sub>, transistor Q<sub>5</sub> and resistances R<sub>2</sub>, R<sub>3</sub> and R<sub>4</sub>.

The resistances R<sub>2</sub> and R<sub>3</sub> are used to equalize the base-emitter voltages of Q<sub>1</sub> and Q<sub>2</sub>.

For the current mirror I chose two BC846B NPN transistors, and the amplifier Q<sub>5</sub> is a PNP BC856B transistor.

For Q<sub>5</sub> to act as an amplifier, it needs to operate in the active mode, so it is safe to assume that V<sub>BE5</sub> = 0.6 V.

The emitter of Q<sub>5</sub> is biased at a fixed voltage of approximately 10 V because of the D<sub>1</sub> Zener diode.

In the base of Q<sub>5</sub> is applied the feedback voltage from the negative feedback circuit (NFC), which will try to equalize this voltage with the one from the emitter of Q<sub>5</sub> (10V) plus V<sub>BE5</sub> = 0.6V (so that Q<sub>5</sub> opens). This results in a base voltage of Q<sub>5</sub> of approximately 10.6 V.

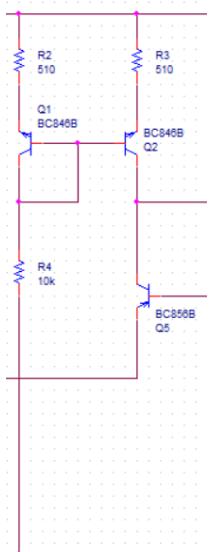


Fig. 3.3

### Series Pass Transistor (Fig. 3.4)

The series pass element is a PNP MJD32CG transistor. It has a maximum power dissipation of 15W.

This is where most of the current will pass through, approximately 25 mA when the potentiometer SET = 0 and 23mA when SET = 1.

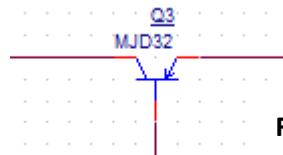


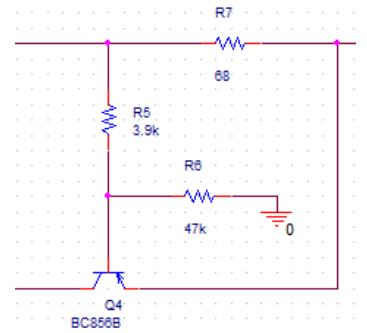
Fig. 3.4

If we change  $V_{in}$  or  $I_{load}$ ,  $V_{out}$  will also change. The amount of voltage with which  $V_{out}$  changes is called “error voltage”. This error voltage will be sampled by the NFC, compared to the reference voltage from D1, and amplified by Q5 and applied as negative feedback to the series pass transistor Q3. Consequently, the voltage drop on Q3 changes accordingly so that it compensates for the initial change in voltage.

### Foldback Current Limit Protection (Fig. 3.5)

It consists of a PNP BC856B transistor and 3 resistances, R5, R6 and R7.

In cases of overcurrent, for example when shorting the output, this Foldback Current Limit Protection activates and protects the circuit from any damage that might be caused by said overcurrent.



**Fig. 3.5**

R7 needs to have a small value ( $\leq 100 \Omega$ ) so I chose  $R7 = 68 \Omega$ . R6 must be 10-15 times greater than R5, so I chose a bigger resistance of  $47k\Omega$  and a smaller one of  $3.9k\Omega$ . Respecting the proportions,  $R6 \approx 12 * R5$ .

### Negative Feedback Circuit (Fig. 3.6)

It comprises resistances R8, R9, R11, R12 and a potentiometer R10.

The relations between the 5 components are given by the following system of equations:

$$V_E = \frac{R_{11} + R_{12}}{R_8 + R_9 + R_{10} + R_{11} + R_{12}} * V_{OUT_{MAX}}$$

$$V_E = \frac{R_{11} + R_{12} + R_{10}}{R_8 + R_9 + R_{10} + R_{11} + R_{12}} * V_{OUT_{MIN}}$$

For my project,  $V_{OUT_{MAX}} = 22V$ ,  $V_{OUT_{MIN}} = 20V$ , and  $V_E = V_{ZENER} + 0.6V$ .

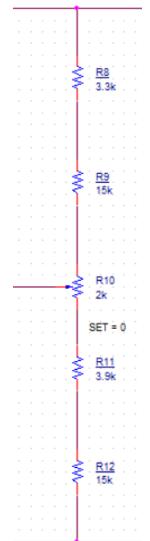
$$V_{ZENER} = V_{D1} = 10V$$

$$\Rightarrow V_E = 10.6V$$

I added 0.6 V to the Zener voltage so that I am sure that the transistor Q5 opens and operates in the active mode, as the potentiometer is connected to the base of Q5.

Following the computations, I reached the following relations:

$$R_{11} + R_{12} = 9.89 * R_{10}$$



**Fig. 3.6**

$$R_8 + R_9 = 9.58 * R_{10}$$

So, for a potentiometer of  $2k\Omega$ , I chose two resistances of  $15k\Omega$ , one resistance of  $3.9k\Omega$  and one of  $3.3k\Omega$ . This way, the relations are respected (with a small error) and the circuit works according to the imposed specifications.

$$R_{10} = 2k\Omega \Rightarrow R_{11} + R_{12} = 19.78k\Omega$$

$$\Rightarrow R_8 + R_9 = 19.16k\Omega$$

### Load Resistance (Fig. 3.7)

To choose an appropriate value for  $R_{13}$ , I used the following relation:

$$R_L = \frac{V_{OUT_{MAX}}}{I_{OUT_{MAX}}}$$

In my case,  $R_L = R_{13}$ ,  $V_{OUT_{MAX}} = 22V$ ,  $I_{OUT_{MAX}} = 26mA$

Substituting these values, I got the following result:

$$R_{13} = \frac{22V}{26 * 10^{-3}A} = 846 \Omega$$

Since there is no standard value of  $846 \Omega$ , I chose the standard value of  $910 \Omega$  for my load resistance  $R_{13}$ .

### Hand calculations:



Fig. 3.7

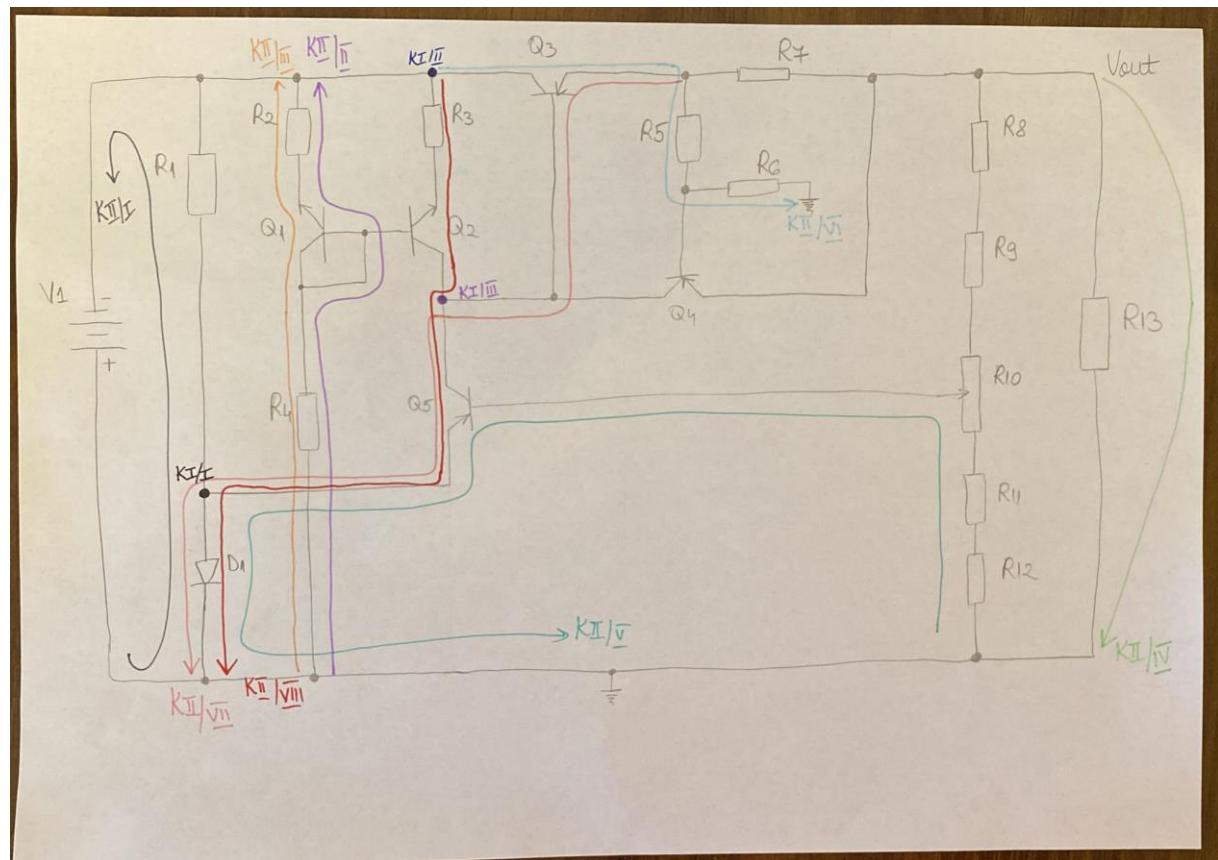


Fig. 3.8

### DC Bias Calculus:

$$KII/I: V_{IN} = V_{D1} + R_1 Y_{R1} \Rightarrow R_1 Y_{R1} = V_{IN} - V_{D1}$$

$$V_{diode} = V_{D1} = 10V$$

Two cases:

$$a) V_{IN} = 26V \Rightarrow R_1 Y_{R1} = 26 - 10 = 16V$$

$$b) V_{IN} = 30V \Rightarrow R_1 Y_{R1} = 30 - 10 = 20V$$

I choose  $R_1 = 4.7k\Omega$ , so  $Y_{R1}$  will be:

$$\begin{cases} a) Y_{R1} = \frac{16V}{4.7 \cdot 10^{-3}\Omega} = 3.4mA \\ b) Y_{R1} = \frac{20V}{4.7 \cdot 10^{-3}\Omega} = 4.25mA \end{cases}$$

### KII/II: For the current mirror:

$$Q_1 \text{ and } Q_2 \text{ are identical} \Rightarrow Y_{C1} = Y_{C2}, V_{BE1} = V_{BE2}, \beta_{F1} = \beta_{F2}$$

I chose  $R_2 = R_3 = 510\Omega$  for a good operation of the current mirror.

Also, I chose  $R_4 = 10k\Omega$ .

$V_{BE1} = V_{BE2} = 0.6V$  (so that both transistors operate in active mode)

$\beta_{F1} = \beta_{F2} = 200$  (This value was taken from the BC846B documentation files, where  $h_{FEmin} = 200$ )

Applying KII/II:

$$V_{IN} = R_4 Y_{R4} + V_{BE1} + R_2 Y_{E1}$$

$$V_{IN} = V_{BE1} + Y_{C1} \left( R_4 + \frac{\beta_{F1} + 1}{\beta_{F1}} R_2 \right)$$

$$Y_{R4} \cong Y_{C1}$$

$$Y_{E1} = \frac{\beta_{F1} + 1}{\beta_{F1}} \cdot Y_{C1}$$

$$Y_{C1} = \frac{V_{IN} - V_{BE1}}{R_4 + \frac{\beta_{F1} + 1}{\beta_{F1}} \cdot R_2}$$

Two cases:

$$a) V_{IN} = 26V \Rightarrow Y_{C1} = \frac{26 - 0.6V}{10 \cdot 10^3 + \frac{201}{200} \cdot 510\Omega} = 2.41mA \Rightarrow Y_{C1min} = 2.41mA$$

$$b) V_{IN} = 30V \Rightarrow Y_{C1} = \frac{30 - 0.6V}{10 \cdot 10^3 + \frac{201}{200} \cdot 510\Omega} = 2.79mA \Rightarrow Y_{C1max} = 2.79mA$$

(1)

$$K_{II/III}: V_{IN} = R_4 Y_{R4} + V_{CE1} + R_2 Y_{E1}$$

$$V_{CE1} = V_{IN} - R_4 Y_{C1} - R_2 Y_{C1} \cdot \frac{\beta_{F+1}}{\beta_F}$$

$$V_{CE1} = V_{IN} - Y_{C1} \left( R_4 + \frac{\beta_{F+1}}{\beta_F} R_2 \right)$$

Two cases:

$$a) V_{IN} = 26V \Rightarrow V_{CE1} = 26 - 2,41 \cdot 10^{-3} \left( 10 \cdot 10^3 + \frac{201}{200} \cdot 510 \right) \Rightarrow V_{CE1} = 0,66V > V_{CE1,\text{sat}}$$

$$b) V_{IN} = 30V \Rightarrow V_{CE1} = 30 - 2,79 \cdot 10^{-3} \left( 10 \cdot 10^3 + \frac{201}{200} \cdot 510 \right) \Rightarrow V_{CE1} = 0,67V > V_{CE1,\text{sat}}$$

$$K_{II/IV}: R_{13} = \frac{V_{out\max}}{I_{out\max}} = \frac{22V}{26mA} = 846\Omega$$

I chose  $R_{13} = 910\Omega$  (standard value)

$$Y_{R4} \cong Y_{C1}; Y_{E1} = \frac{\beta_{F+1}}{\beta_F} Y_{C1}$$

$V_{CE1,\text{sat}} = 90\text{mV}$  (from BC846B documentation files)

$$R_{13} = R_{load}$$

$I_{out\max} = 26\text{mA}$  (from my project requirements)

$$\begin{cases} V_{out\max} = V_E \left( 1 + \frac{R_8 + R_9 + R_{10}}{R_{11} + R_{12}} \right) \\ V_{out\min} = V_E \left( 1 + \frac{R_8 + R_9}{R_{10} + R_{11} + R_{12}} \right) \end{cases}$$

$$\begin{cases} 22 = 10,6 \left( 1 + \frac{R_8 + R_9 + R_{10}}{R_{11} + R_{12}} \right) \\ 20 = 10,6 \left( 1 + \frac{R_8 + R_9}{R_{10} + R_{11} + R_{12}} \right) \end{cases} \Rightarrow \begin{cases} 2,04 = 1 + \frac{R_8 + R_9 + R_{10}}{R_{11} + R_{12}} \\ 1,88 = 1 + \frac{R_8 + R_9}{R_{10} + R_{11} + R_{12}} \end{cases}$$

Consider  $R_8 + R_9 = R_1$  and  $R_{11} + R_{12} = R_2$ , with  $R_{10} = P$ .

$$\Rightarrow \begin{cases} 1,04 = \frac{R_1 + P}{R_2} \\ 0,88 = \frac{R_1}{R_2 + P} \end{cases} \Rightarrow \begin{cases} 1,04 R_2 = R_1 + P \\ -0,88 R_2 - 0,88 P = -R_1 \end{cases} \quad \begin{matrix} \oplus \\ 1,04 R_2 - 0,88 R_2 - 0,88 P = P \end{matrix}$$

$$0,16 R_2 = 1,88 P$$

$$R_2 = 9,89 P \Rightarrow R_{11} + R_{12} = 9,89 R_{10}$$

$$1,04 R_2 = R_1 + P \Rightarrow 1,04 \cdot 9,89 P = R_1 + P$$

$$\Rightarrow R_1 = 9,58 P \Rightarrow R_8 + R_9 = 9,58 \cdot R_{10}$$

$$\text{For } R_{10} = 2k\Omega \Rightarrow R_8 + R_9 = 19,16 k\Omega$$

$$R_{11} + R_{12} = 19,48 k\Omega$$

I chose

$$\begin{cases} R_8 = 3,3k\Omega, R_9 = 15k\Omega \\ R_{11} = 3,9k\Omega, R_{12} = 15k\Omega \end{cases}$$

(2)

$$K \bar{I} / VI: V_{IN} = V_{CE3} + R_5 I_{R5} + R_6 I_{R6}$$

The transistor Q<sub>4</sub> opens only in cases of overcurrent, such as when shorting the output.

In our case, Q<sub>4</sub> is not open so the currents passing through it are negligible.

This means that  $I_{R5} = I_{R6} = I$

For a current  $I_{R5} = I_{R6} = 467.2 \mu A$  ( $V_{IN} = 26V$ ,  $V_{out} = 22V$ ), we have:

$$V_{CE3} = V_{IN} - I(R_5 + R_6)$$

$$V_{CE3} = 26 - 467.2 \cdot 10^{-6} (R_5 + R_6)$$

For the foldback current limit protection:

$R_7 < 100\Omega$ , so I chose  $R_7 = 68\Omega$

$$I_{load} = \frac{1}{R_7} \left[ \left(1 + \frac{R_5}{R_6}\right) V_{BE} + \frac{R_5}{R_6} V_{out} \right]; \text{ I consider } R_6 = 12 \cdot R_5$$

$$R_5 = 3.9 k\Omega$$

$$R_6 = 47 k\Omega$$

$$\Rightarrow I_{load} = \frac{1}{68} \left[ \left(1 + \frac{R_5}{12R_5}\right) V_{BE} + \frac{R_5}{12R_5} V_{out} \right]$$

$$I_{load} = \frac{1}{68} \left[ \frac{13}{12} V_{BE} + \frac{1}{12} V_{out} \right]$$

Two cases:

$$a) V_{out} = 20V \Rightarrow I_{load} = \frac{1}{68} \left[ \frac{13}{12} \cdot 0.6 + \frac{1}{12} \cdot 20 \right]$$

$$I_{load} = 34.06 \text{ mA} > I_{out,max} = 26 \text{ mA}$$

$$b) V_{out} = 22V \Rightarrow I_{load} = \frac{1}{68} \left[ \frac{13}{12} \cdot 0.6 + \frac{1}{12} \cdot 22 \right]$$

$$I_{load} = 36.51 \text{ mA} > I_{out,max} = 26 \text{ mA}$$

$$I_{SC} = \frac{1}{R_7} \left(1 + \frac{R_5}{R_6}\right) V_{BE} = \frac{1}{68} \left(1 + \frac{3.9 \cdot 10^3}{47 \cdot 10^3}\right) \cdot 0.6 \Rightarrow I_{SC} = 15.9 \text{ mA}$$

(3)

$$V_{CE3} = V_{IN} - \gamma(R_5 + R_6)$$

$V_{CE3,sat} = 1.2 \text{ V}$  (from ~~BC856B~~ documentation files) MJD32CG

Two cases:

a)  $V_{IN} = 26 \text{ V} \Rightarrow V_{CE3} = 26 - 46,2 \cdot 10^{-6} (3,9 + 4,7) \cdot 10^3$

$$V_{CE3} = 2,21 \text{ V} > V_{CE3,sat}$$

b)  $V_{IN} = 30 \text{ V} \Rightarrow V_{CE3} = 30 - 46,2 \cdot 10^{-6} (3,9 + 4,7) \cdot 10^3$

$$V_{CE3} = 6,21 \text{ V} > V_{CE3,sat}$$

For both of these cases, I considered  $V_{out} = 22 \text{ V}$ .

K<sub>II</sub> / VII:  $V_{IN} - V_{CE3} = V_{EB3} + V_{CE5} + V_{DI}$

$$V_{CE5,sat} = 300 \text{ mV}$$

$$V_{CE5} = V_{IN} - V_{CE3} + V_{BE3} - V_{DI}$$

(Q5 - BC856B)

$$V_{BE5} = 0,6 \text{ V}$$

Two cases:

a)  $V_{IN} = 26 \text{ V} \Rightarrow V_{CE5} = 26 - 2,21 + 0,6 - 10 \Rightarrow V_{CE5} = 14,39 \text{ V} > V_{CE5,sat}$

b)  $V_{IN} = 30 \text{ V} \Rightarrow V_{CE5} = 30 - 6,21 + 0,6 - 10 \Rightarrow V_{CE5} = 14,39 \text{ V} > V_{CE5,sat}$

K<sub>II</sub> / VIII:

$$V_{IN} = R_3 Y_{E2} + V_{EC2} + V_{CE5} + V_{DI}$$

$$\left. \begin{aligned} Y_{E2} &= \frac{\beta_f + 1}{\beta_f} Y_{C2} \\ Y_{C1} &= Y_{C2} \end{aligned} \right\} \Rightarrow$$

$$V_{CE2} = -V_{IN} + R_3 \frac{\beta_f + 1}{\beta_f} Y_{C1} + V_{CE5} + V_{DI}$$

$$\Rightarrow Y_{E2} = \frac{201}{200} Y_{C1}$$

Two cases:

a)  $V_{IN} = 26 \text{ V}$

$$\Rightarrow V_{CE2} = -26 + 510 \cdot \frac{201}{200} \cdot 2,41 \cdot 10^{-3} + 14,39 + 10 \Rightarrow V_{CE2} = 0,374 \text{ V} > V_{CE2,sat}$$

" 30mV

b)  $V_{IN} = 30 \text{ V}$

$$\Rightarrow V_{CE2} = -30 + 510 \cdot \frac{201}{200} \cdot 2,49 \cdot 10^{-3} + 14,39 + 10 \Rightarrow V_{CE2} = 4,14 \text{ V} > V_{CE2,sat}$$

For transistor Q<sub>4</sub>:

Being part of the foldback circuit, Q<sub>4</sub> will open only in cases of overcurrent. In the other cases, it will stay blocked and barely any current will flow through it. This is why  $I_{B4}$ ,  $I_{C4}$  and  $I_{E4}$  are very small (pA, fA). ④

For  $V_{IN} = 26 \text{ V} \Rightarrow I_{B4} \approx I_{C4} = 198 \mu\text{A}$   
 $I_{E4} = 642 \mu\text{A}$

The same is for  $V_{IN} = 30 \text{ V} \Rightarrow I_{B4} \approx I_{C4} = 198 \mu\text{A}$   
 $I_{E4} = 643 \mu\text{A}$

For transistor Q3 (~~Q3055B~~):

According to the documentation files,  $\beta_F = \frac{10}{\downarrow}$

$$K_I/I: I_{D1} = I_{R1} + I_{E5}$$

For Zener diode D<sub>1</sub>,  $I_Z \text{ min} = 5 \text{ mA}$

Two cases:

a)  $V_{IN} = 26 \text{ V}$

$$\left. \begin{array}{l} I_{D1} = 5,4 \text{ mA} > I_Z \text{ min} \\ I_{R1} = 3,4 \text{ mA} \end{array} \right\} \Rightarrow I_{E5} = I_{D1} - I_{R1} = 5,4 - 3,4 = 2,3 \text{ mA}$$

$$I_{C5} = \frac{220}{221} \cdot 2,3 = 2,28 \text{ mA}$$

b)  $V_{IN} = 30 \text{ V}$

$$\left. \begin{array}{l} I_{D1} = 6,9 \text{ mA} > I_Z \text{ min} \\ I_{R1} = 4,2 \text{ mA} \end{array} \right\} \Rightarrow I_{E5} = I_{D1} - I_{R1} = 6,9 - 4,2 = 2,7 \text{ mA}$$

$$I_{C5} = \frac{220}{221} \cdot 2,7 = 2,68 \text{ mA}$$

K<sub>I</sub> II:  $I_{C3} = I_{IN} - I_{R1} - I_{R2} - I_{R3}$

Two cases:

a)  $V_{IN} = 26 \text{ V} \Rightarrow I_{IN} = 33,41 \text{ mA}, I_{R1} = 3,4 \text{ mA}, I_{R2} = I_{R3} = 2,4 \text{ mA}$

$$\Rightarrow I_{C3} = 33,41 - 3,4 - 2,4 - 2,4 = 25,21 \text{ mA}$$

b)  $V_{IN} = 30 \text{ V} \Rightarrow I_{IN} = 35,08 \text{ mA}, I_{R1} = 4,253 \text{ mA}, I_{R2} = I_{R3} = 2,8 \text{ mA}$

$$I_{C3} = 35,08 - 4,253 - 2,8 - 2,8 = 25,224 \text{ mA}$$

! For Q5 PNP BC856B SMD, SOT23, 80V, 100mA

$$\beta_F = 220$$

(5)

$$KII\bar{III}: J_{C2} = J_{E5} + J_{B3}$$

Two cases:

$$a) V_{IN} = 26V \Rightarrow J_{E5} = 2.3 \text{ mA} \quad J_{B3} = 103 \mu\text{A} \quad J_{C2} = 2.3 \text{ mA} + 103 \mu\text{A} \quad J_{C2} = 2.403 \text{ mA}$$

$$b) V_{IN} = 30V \Rightarrow J_{E5} = 2.4 \text{ mA} \quad J_{B3} = 96 \mu\text{A} \quad J_{C2} = 2.4 \text{ mA} + 96 \mu\text{A} \quad J_{C2} = 2.496 \text{ mA}$$

Calculus of powers:

$$a) V_{IN} = 26V$$

$$P_{diode} = V_{D1} \cdot J_{D1} = 10V \cdot 5,698 \mu\text{A} \Rightarrow P_{diode} = 56,98 \mu\text{W}$$

$$P_{R1} = R_1 \cdot J_{R1}^2 = 4,7 \cdot 10^3 \Omega \cdot 3,4^2 \cdot 10^{-6} \text{ mA}^2 \Rightarrow P_{R1} = 54,33 \text{ mW}$$

$$P_{R2} = R_2 \cdot J_{R2}^2 = 510 \cdot 2,4^2 \cdot 10^{-6} \Rightarrow P_{R2} = 2,93 \text{ mW}$$

$$P_{R3} = R_3 \cdot J_{R3}^2 = 510 \cdot 2,4^2 \cdot 10^{-6} \Rightarrow P_{R3} = 2,93 \text{ mW}$$

$$P_{R4} = R_4 \cdot J_{R4}^2 = 10 \cdot 10^3 \cdot 2,4^2 \cdot 10^{-6} \Rightarrow P_{R4} = 54,6 \text{ mW}$$

$$P_{R5} = R_5 \cdot J_{R5}^2 = 3,9 \cdot 10^3 \cdot 4,67^2 \cdot 10^{-12} \Rightarrow P_{R5} = 850,5 \mu\text{W}$$

$$P_{R6} = R_6 \cdot J_{R6}^2 = 4,7 \cdot 10^3 \cdot 4,67^2 \cdot 10^{-12} \Rightarrow P_{R6} = 10,25 \text{ mW}$$

$$P_{R7} = R_7 \cdot J_{R7}^2 = 68 \cdot 24,28^2 \cdot 10^{-6} \Rightarrow P_{R7} = 41,82 \text{ mW}$$

$$P_{R8} = R_8 \cdot J_{R8}^2 = 3,3 \cdot 10^3 \cdot 566^2 \cdot 10^{-12} \Rightarrow P_{R8} = 1,057 \text{ mW}$$

$$P_{R9} = R_9 \cdot J_{R9}^2 = 15 \cdot 10^3 \cdot 566^2 \cdot 10^{-12} \Rightarrow P_{R9} = 418 \text{ mW}$$

$$P_{R10} = R_{10} \cdot J_{R10}^2 = 2 \cdot 10^3 \cdot 566^2 \cdot 10^{-12} \Rightarrow P_{R10} = 624 \mu\text{W}$$

$$P_{R11} = R_{11} \cdot J_{R11}^2 = 3,9 \cdot 10^3 \cdot 566^2 \cdot 10^{-12} \Rightarrow P_{R11} = 1,223 \text{ mW}$$

$$P_{R12} = R_{12} \cdot J_{R12}^2 = 15 \cdot 10^3 \cdot 566^2 \cdot 10^{-12} \Rightarrow P_{R12} = 4,7 \text{ mW}$$

$$P_{R13} = R_{13} \cdot J_{R13}^2 = 910 \cdot 24,28^2 \cdot 10^{-6} \Rightarrow P_{R13} = 536,46 \text{ mW}$$

$$P_{Q1} = J_{C1} \cdot V_{CE1} = 2,41 \cdot 10^{-3} \text{ A} \cdot 0,66 \text{ V} \Rightarrow P_{Q1} = 1,59 \text{ mW}$$

$$P_{Q2} = J_{C2} \cdot V_{CE2} = 2,403 \cdot 10^{-3} \text{ A} \cdot 0,344 \Rightarrow P_{Q2} = 898,72 \mu\text{W}$$

$$P_{Q3} = J_{C3} \cdot V_{CE3} = 25,21 \cdot 10^{-3} \text{ A} \cdot 2,21 \text{ V} \Rightarrow P_{Q3} = 55,41 \text{ mW}$$

$$P_{Q5} = J_{C5} \cdot V_{CE5} = 2,28 \cdot 10^{-3} \text{ A} \cdot 14,39 \text{ V} \Rightarrow P_{Q5} = 32,8 \text{ mW}$$

$P_{Q4}$  is very small, of the order of  $\mu\text{W}$  ( $491,6 \mu\text{W}$ ).

(6)

b)  $V_{IN} = 30V$

$$P_{diode} = V_{D1} \cdot I_{D1} = 10V \cdot 6,9mA \Rightarrow P_{diode} = 69mW$$

$$P_{R1} = R_1 \cdot I_{R1}^2 = 4,4 \cdot 10^3 \Omega \cdot 4,25 \cdot 10^{-6} A = 84,89mW \Rightarrow P_{R1} = 84,9mW$$

$$P_{R2} = R_2 \cdot I_{R2}^2 = 510 \cdot 2,44^2 \cdot 10^{-6} \Rightarrow P_{R2} = 3,91mW$$

$$P_{R3} = R_3 \cdot I_{R3}^2 = 510 \cdot 2,44^2 \cdot 10^{-6} \Rightarrow P_{R3} = 3,91mW$$

$$P_{R4} = R_4 \cdot I_{R4}^2 = 10 \cdot 10^3 \cdot 2,44^2 \cdot 10^{-6} \Rightarrow P_{R4} = 44,2mW$$

$$P_{R5} = R_5 \cdot I_{R5}^2 = 3,9 \cdot 10^3 \cdot 468^2 \cdot 10^{-12} \Rightarrow P_{R5} = 854,2 \mu W$$

$$P_{R6} = R_6 \cdot I_{R6}^2 = 47 \cdot 10^3 \cdot 468^2 \cdot 10^{-12} \Rightarrow P_{R6} = 10,3mW$$

$$P_{R7} = R_7 \cdot I_{R7}^2 = 68 \cdot 24,3^2 \cdot 10^{-6} \Rightarrow P_{R7} = 42,16mW$$

$$P_{R8} = R_8 \cdot I_{R8}^2 = 3,3 \cdot 10^3 \cdot 568^2 \cdot 10^{-12} \Rightarrow P_{R8} = 1,06mW$$

$$P_{R9} = R_9 \cdot I_{R9}^2 = 15 \cdot 10^3 \cdot 568^2 \cdot 10^{-12} \Rightarrow P_{R9} = 4,83mW$$

$$P_{R10} = R_{10} \cdot I_{R10}^2 = 2 \cdot 10^3 \cdot 560^2 \cdot 10^{-12} \Rightarrow P_{R10} = 62,2 \mu W$$

$$P_{R11} = R_{11} \cdot I_{R11}^2 = 3,9 \cdot 10^3 \cdot 560^2 \cdot 10^{-12} \Rightarrow P_{R11} = 1,223mW$$

$$P_{R12} = R_{12} \cdot I_{R12}^2 = 15 \cdot 10^3 \cdot 560^2 \cdot 10^{-12} \Rightarrow P_{R12} = 4,4mW$$

$$P_{R13} = R_{13} \cdot I_{R13}^2 = 910 \cdot 24,33^2 \cdot 10^{-6} \Rightarrow P_{R13} = 538,6mW$$

$$P_{Q1} = I_{C1} \cdot V_{CE1} = 2,79 \cdot 10^{-3} A \cdot 0,67V \Rightarrow P_{Q1} = 1,86mW$$

$$P_{Q2} = I_{C2} \cdot V_{CE2} = 2,496 \cdot 10^{-3} A \cdot 4,14V \Rightarrow P_{Q2} = 11,6mW$$

$$P_{Q3} = I_{C3} \cdot V_{CE3} = 25,224 \cdot 10^{-3} A \cdot 6,21V \Rightarrow P_{Q3} = 156,65mW$$

$$P_{Q5} = I_{C5} \cdot V_{CE5} = 2,68 \cdot 10^{-3} \cdot 14,39V \Rightarrow P_{Q5} = 38,56mW$$

$P_{Q4}$  is very small, of the order of  $pW$  ( $492\mu W$ )

The maximum values from the datasheets:

- For the Zener diode :  $P_{tot} = 250mW$

$$I_{fmax} = 200mA$$

$$P_{dmin} = 57mW, P_{dmax} = 69mW$$

$$I_{D1min} = 57mA, I_{D1max} = 6,9mA$$

from my project

$\Rightarrow$  The Zener diode  $D_1$  works reliably as it doesn't reach the maximum values from the datasheet ( $250mW, 200mA$ ).

- For the resistors:

$$P_{\max} = 125 \text{ mW}$$

All resistors have a reliable operation, as none of them have a dissipated power that reaches 125 mW.

- For the transistors:

$$\begin{aligned} \text{BC846B : } I_C &= 100 \text{ mA} \\ V_{CE(\text{MAX})} &= 65 \text{ V} \\ V_{CE(\text{sat})} &= 90 \text{ mV} \\ P_{\text{tot}} &= 250 \text{ mW} \end{aligned}$$

$$\begin{aligned} \text{BC856B : } I_C &= 100 \text{ mA} \\ V_{BE(\text{MAX})} &= 65 \text{ V} \\ V_{CE(\text{sat})} &= 300 \text{ mV} \\ P_{\text{tot}} &= 250 \text{ mW} \end{aligned}$$

All transistors work in a reliable manner, as none of their parameters reach these maximum values.

! Note : For  $R_{13}$ , the load resistance, the dissipated power is greater than 125 mW, being around 500-550 mW. However, this is the expected behaviour for Load, so we don't need to worry.

- For transistor Q<sub>3</sub>:

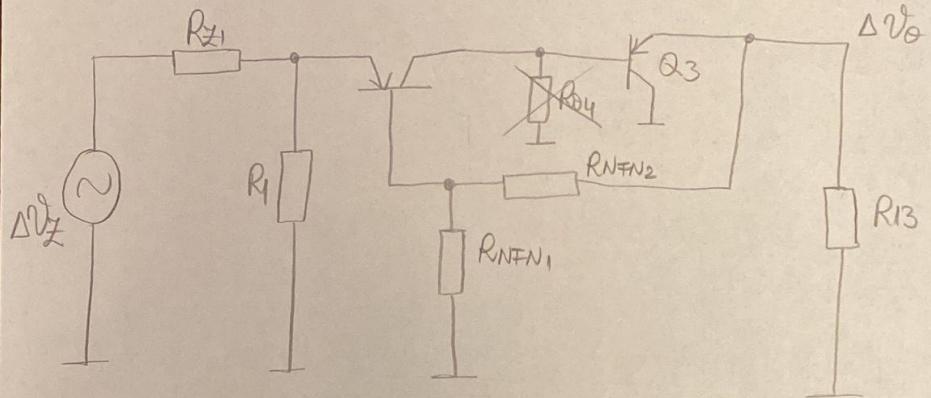
$P_{\text{tot}} = 15 \text{ W}$  for a MJ32CG PNP, SMD transistor  
From the computations,  $P_{Q3}$  was somewhere below 40 mW.

Even in the worst case scenario, the total dissipated power on Q<sub>3</sub> will be:

$$P_{Q3,\max} = V_{out,\max} \cdot I_{out,\max} = 22 \text{ V} \cdot 26 \text{ mA}$$

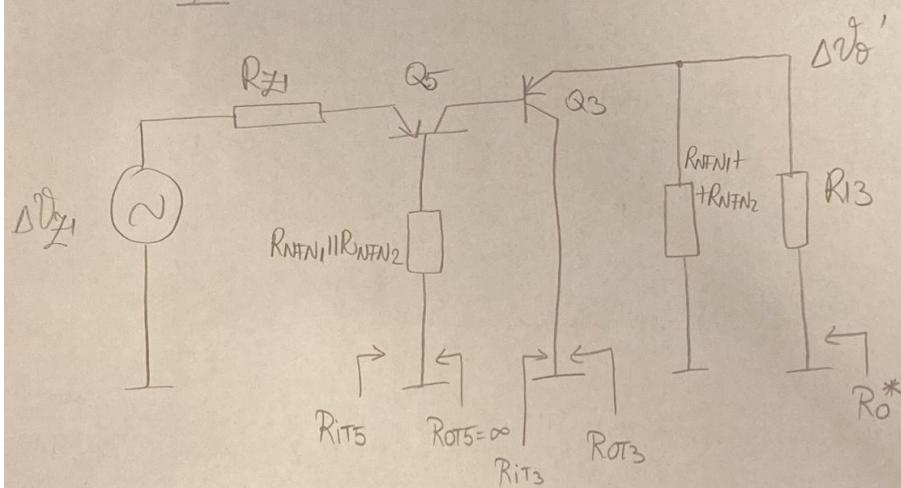
$$P_{Q3,\max} = 572 \text{ mW} < 15 \text{ W}$$

AC Calculus



I will denote  $R_{11} + R_{12} = R_{NFN1}$ ;  $R_{10} + R_9 + R_8 = R_{NFN2}$

$$R_{611}(R_5 + R_7) \parallel Q_4 \equiv R_{Q4} = \infty$$



Series-Shunt NFN:

$$\frac{f_V}{f_V} = \frac{R_{NFN1}}{R_{NFN1} + R_{NFN2}} = \frac{3,9k + 15k}{3,9k + 15k + 2k + 3,3k + 15k}$$

$$\boxed{f_V = 0,482}$$

(9)

$$g_{m3} = 40 \cdot \beta_{c3} = 40 \cdot 25 \cdot 10^{-3} \Rightarrow g_{m3} = 1 \text{ A/V}$$

$$g_{m5} = 40 \cdot \beta_{c5} = 40 \cdot 2,28 \cdot 10^{-3} \Rightarrow g_{m5} = 0,09 \text{ A/V}$$

$$r_{\pi 3} = \frac{\beta_{F3}}{g_{m3}} = \frac{10}{1} \Rightarrow r_{\pi 3} = 10 \Omega$$

$$r_{\pi 5} = \frac{\beta_{F5}}{g_{m5}} = \frac{220}{0,09} = 2,4 k\Omega$$

$$r_{iT5} = \frac{r_{\pi 5} + (R_{NFN1} \parallel R_{NFN2})}{1 + \beta_{F5}} = \frac{2,4 + 9,78}{1 + 220} = \frac{12,18}{221} = 0,0551 k\Omega$$

$$r_{iT5} = 55,1 \Omega$$

Consider  $r_{ce3} = 1 k\Omega$

$$r_{iT3} = r_{\pi 3} + (1 + \beta_{F3}) [r_{ce3} \parallel (\overbrace{R_{NFN1} + R_{NFN2}}^{R_{NFN}}) \parallel R_{i3}]$$

$$r_{ce3} \parallel (R_{NFN1} + R_{NFN2}) \parallel R_{i3} = \frac{r_{ce3} R_{NFN} R_{i3}}{r_{ce3} R_{NFN} + R_{NFN} R_{i3} + R_{i3} r_{ce3}} = 0,47 k\Omega$$

$$\Rightarrow r_{iT3} = 10 \Omega + (1 + 10) \cdot 0,47 \cdot 10^3 = 5180 \Omega$$

$$r_{OT3} = \cancel{r_{ce3}} \cancel{r_{ce3} \parallel \frac{r_{\pi 3}}{1 + \beta_{F3}}} = \frac{r_{ce3} \frac{r_{\pi 3}}{1 + \beta_{F3}}}{r_{ce3} + \frac{r_{\pi 3}}{1 + \beta_{F3}}} = 0,91 \Omega$$

~~$$\alpha_V = \frac{\Delta V_o}{\Delta V_{Z1}} = r_{ce3} \parallel (R_{NFN1} + R_{NFN2})$$~~

$$\alpha_V = \frac{\Delta V_o}{\Delta V_{Z1}} = [r_{ce3} \parallel (R_{NFN1} + R_{NFN2}) \parallel R_{i3}] (\beta_{F3} + 1) \cdot \frac{1}{R_{Z1} + R_{iT5}} \cdot \frac{\beta_{F5}}{\beta_{F5} + 1}$$

$$\alpha_V = 0,47 \cdot 10^3 \cdot 11 \cdot \frac{1}{10 + 55,1} \cdot \frac{220}{221}$$

$$\alpha_V = 49,05$$

$$T = \alpha_V \cdot f_V = 49,05 \cdot 0,482 = 38,10$$

(10)

$$\frac{1}{R_0} = \frac{1+T}{R_0^*} - \frac{1}{R_{13}} = \frac{1+38,1}{R_0^*} - \frac{1}{910}$$

$$R_0^* = R_{OT3} \parallel R_{NFN} \parallel R_{13} = \frac{R_{OT3} \cdot R_{NFN} \cdot R_{13}}{R_{OT3} \cdot R_{NFN} + R_{NFN} \cdot R_{13} + R_{13} \cdot R_{OT3}}$$

$$R_0^* = 0,90\Omega$$

$$\frac{1}{R_0} = \frac{38,1}{0,90} - \frac{1}{910} = 43,4 - 1,09 \cdot 10^{-3} = 43,39 \Omega^{-1}$$
$$\Rightarrow R_0 = 0,02\Omega < 2\Omega$$

(11)

## 4. Simulations

Bias Point Simulation for the Worst-Case Scenario Vin = 26 V, Vout = 22 V (SET = 0) (Fig. 4.1)

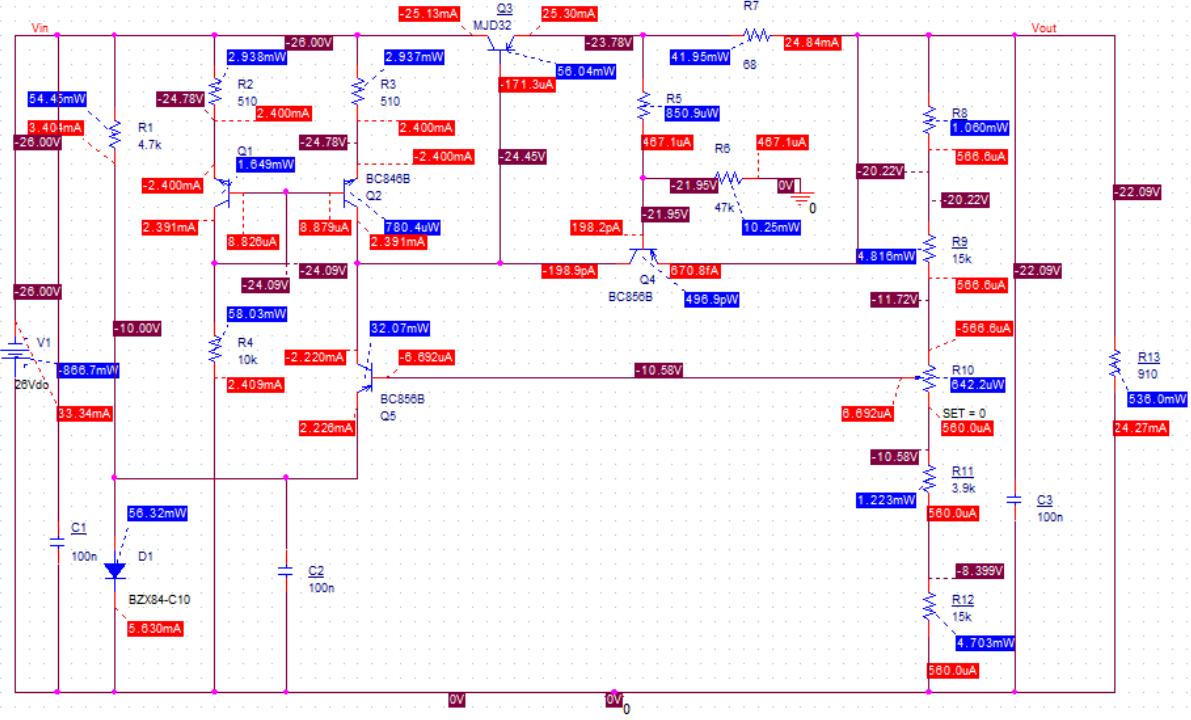


Fig. 4.1

Bias Point Simulation for Vin = 26 V, Vout = 20 V (SET = 1) (Fig. 4.2)

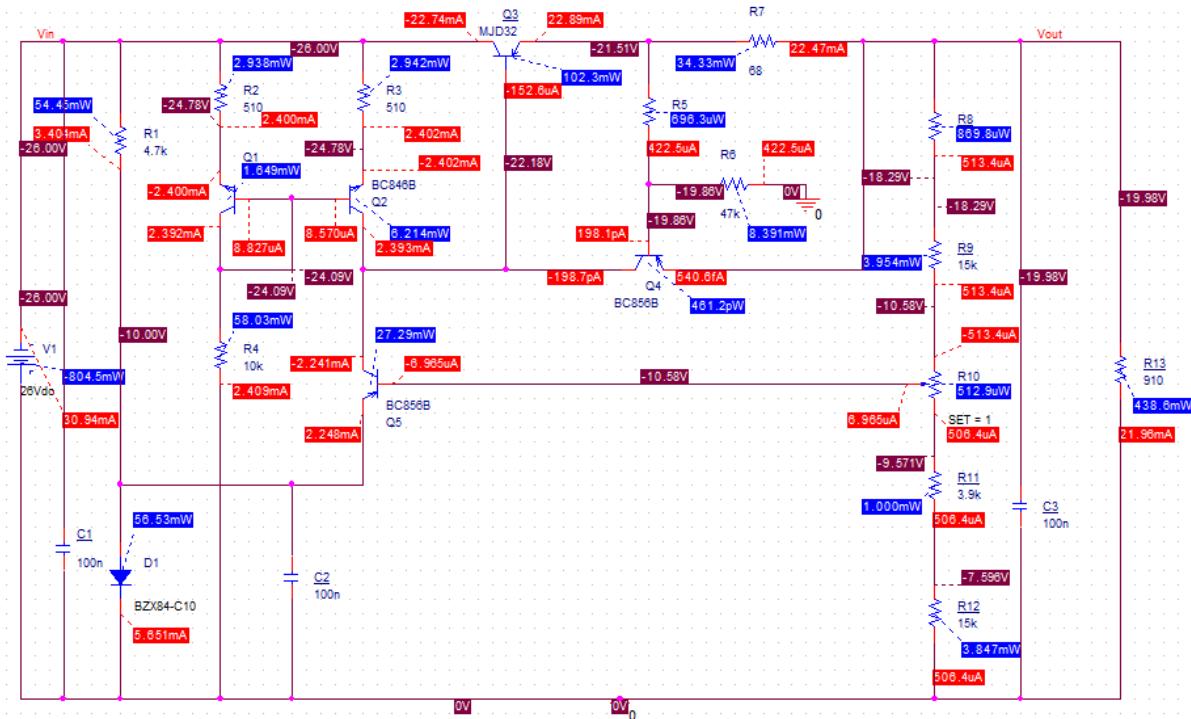


Fig. 4.2

## DC Sweep Simulation

For this simulation, I kept the circuit schematic as it was. No changes were made.

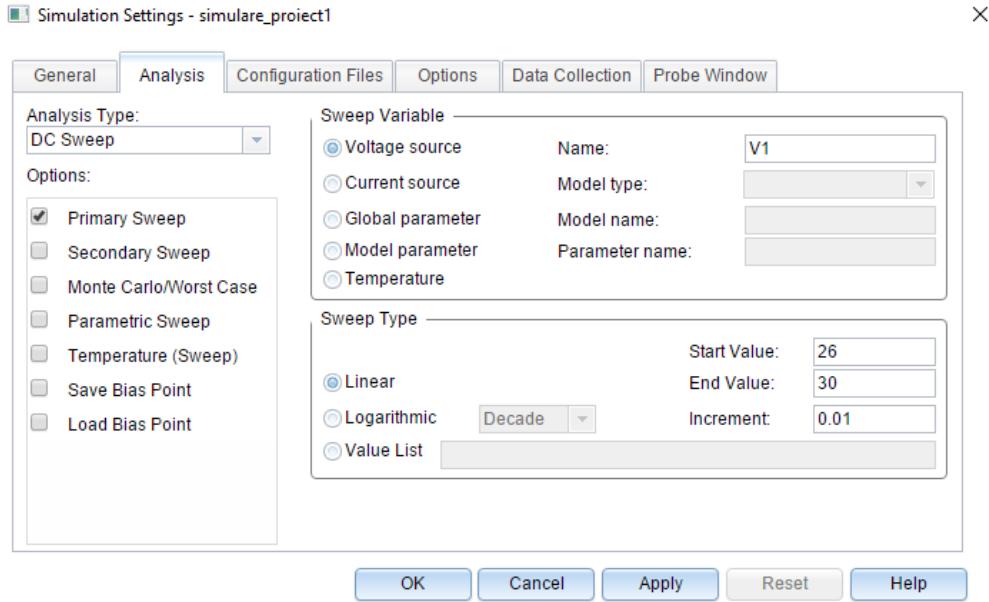


Fig. 4.3

In the figures 4.4 - 4.7, I plotted V(Vout).

For the **worst case scenario**, where **Vin = 26 V, Vout = 22 V (SET = 0)** (Fig. 4.3)

This simulation is saved as **sim1.dat**

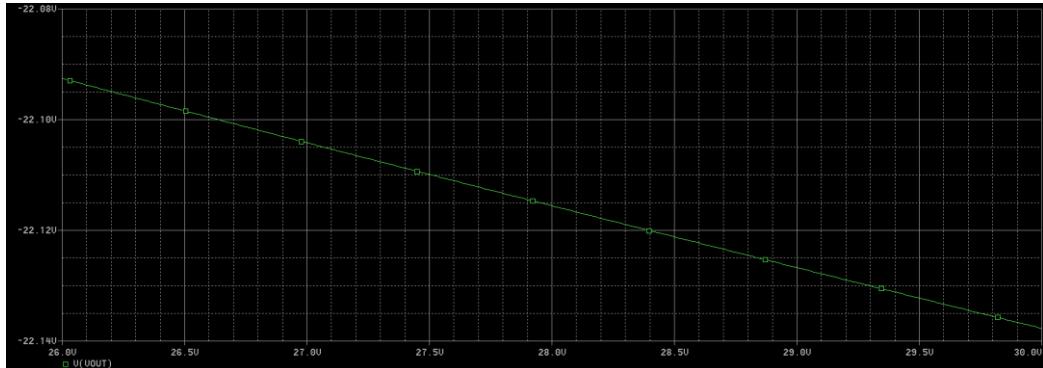


Fig. 4.4

For **Vin = 26 V, Vout = 20 V (SET = 1)** (Fig. 4.4)

This simulation is saved as **sim2.dat**

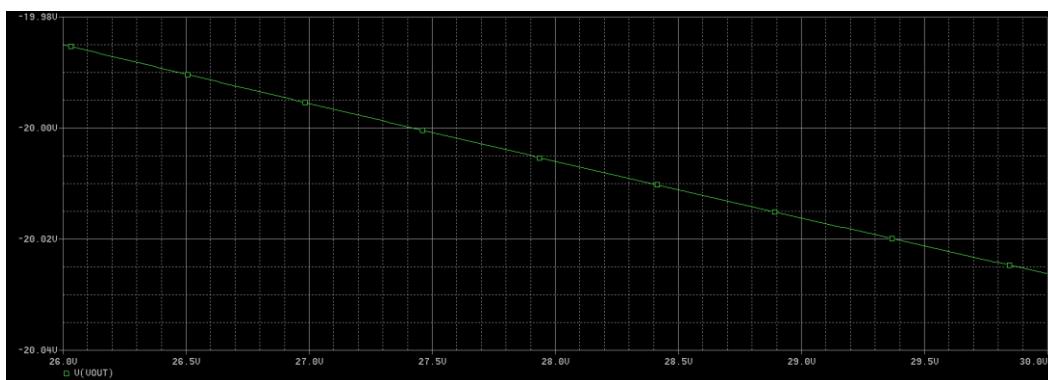


Fig. 4.5

For  $V_{in} = 30 \text{ V}$ ,  $V_{out} = 22 \text{ V}$  (SET = 0) (Fig. 4.5)

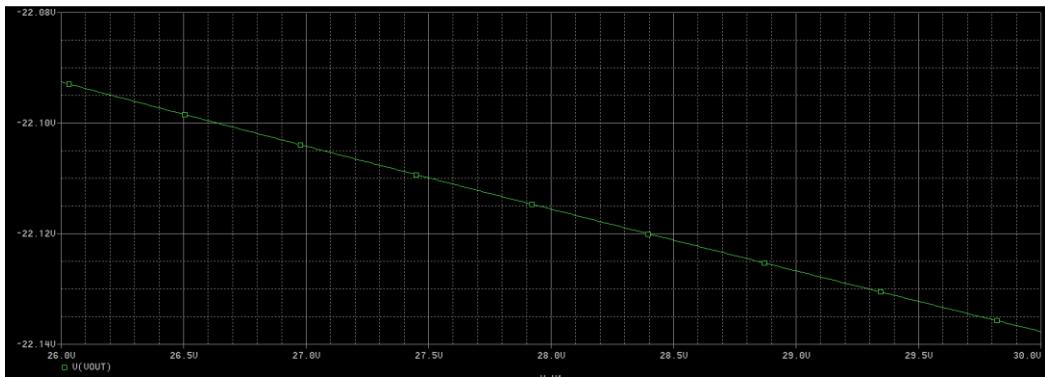


Fig. 4.6

For  $V_{in} = 30 \text{ V}$ ,  $V_{out} = 20 \text{ V}$  (SET = 1) (Fig. 4.6)

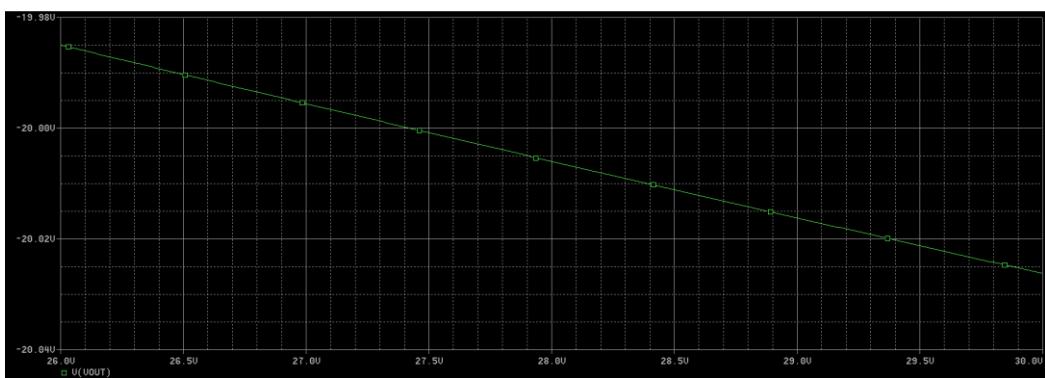


Fig. 4.7

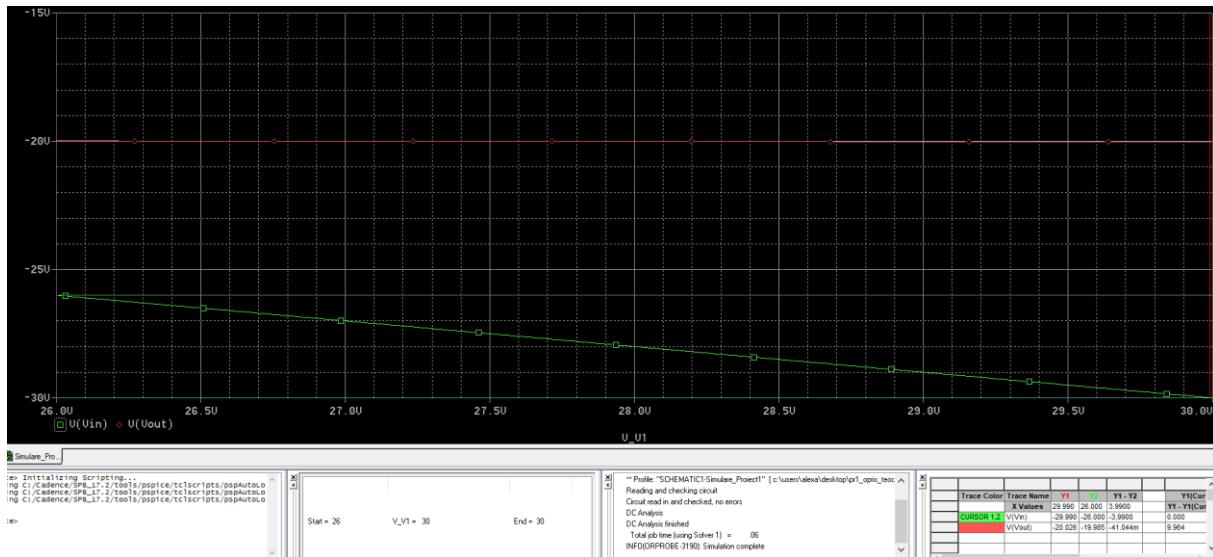
### Computing S using the graphs from the DC Sweep Simulation:

To find S, we need  $\Delta V_{in}$  and  $\Delta V_{out}$ . We find them by plotting the graph and adding the traces for both  $V_{in}$  and  $V_{out}$ .

Using the cursors, we find the initial and final values for  $V_{in}$  and  $V_{out}$ , and then we can find  $\Delta V_{in}$  and  $\Delta V_{out}$ .

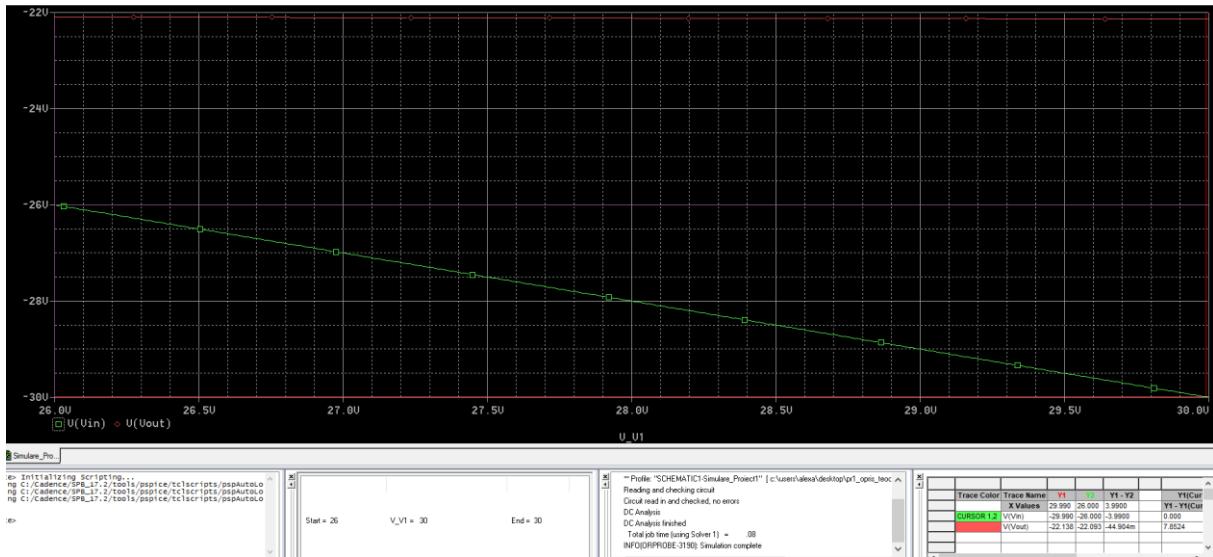
According to the graph for  $V_{in} = 26 \text{ V}$  and  $\text{SET} = 1$  (Fig. 4.8)

$$S = \frac{\Delta V_{in}}{\Delta V_{out}} = \frac{-3.99 \text{ V}}{-0.041 \text{ V}} = 97.31 > 53$$



**Fig. 4.8**

Then, I computed S for  $V_{in} = 26\text{ V}$  and  $SET = 0$  using the same principle (Fig. 4.9)



**Fig. 4.9**

From these graphs, it results:

$$S = \frac{\Delta V_{in}}{\Delta V_{out}} = \frac{-3.99\text{ }V}{-0.045\text{ }V} = 88.66 > 53$$

## AC Sweep Simulation

Finding S from the AC Sweep Simulation graph:

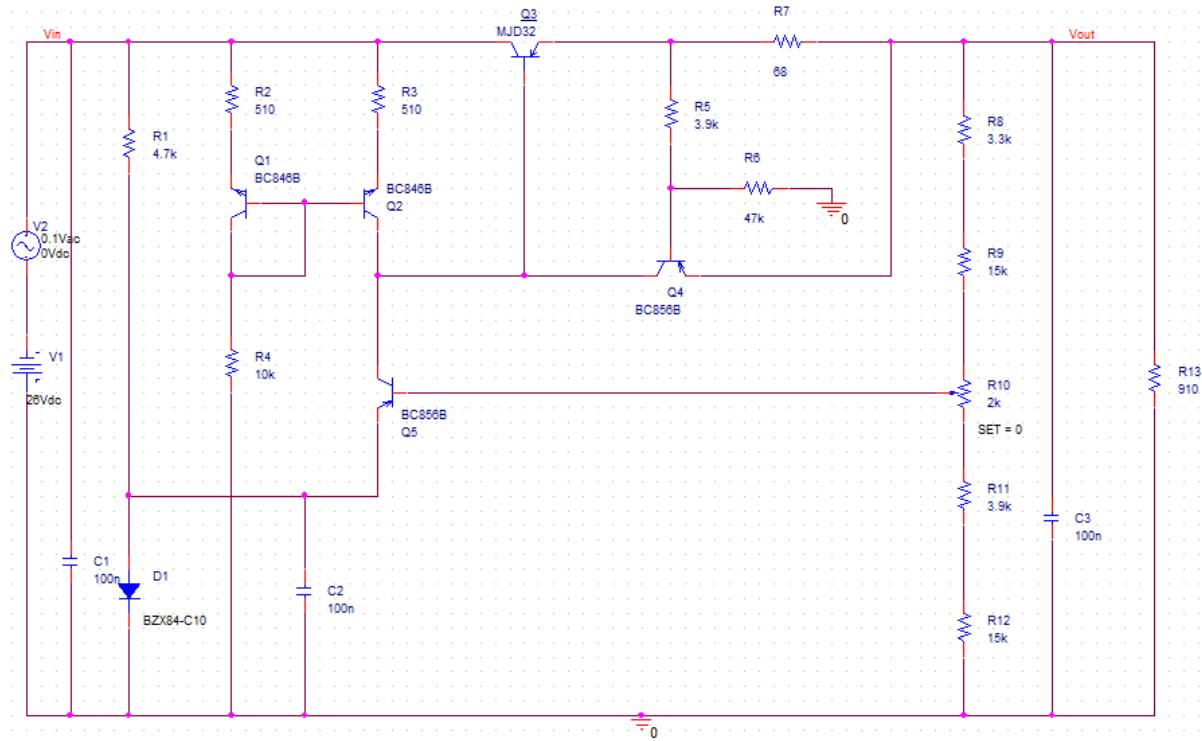


Fig. 4.10

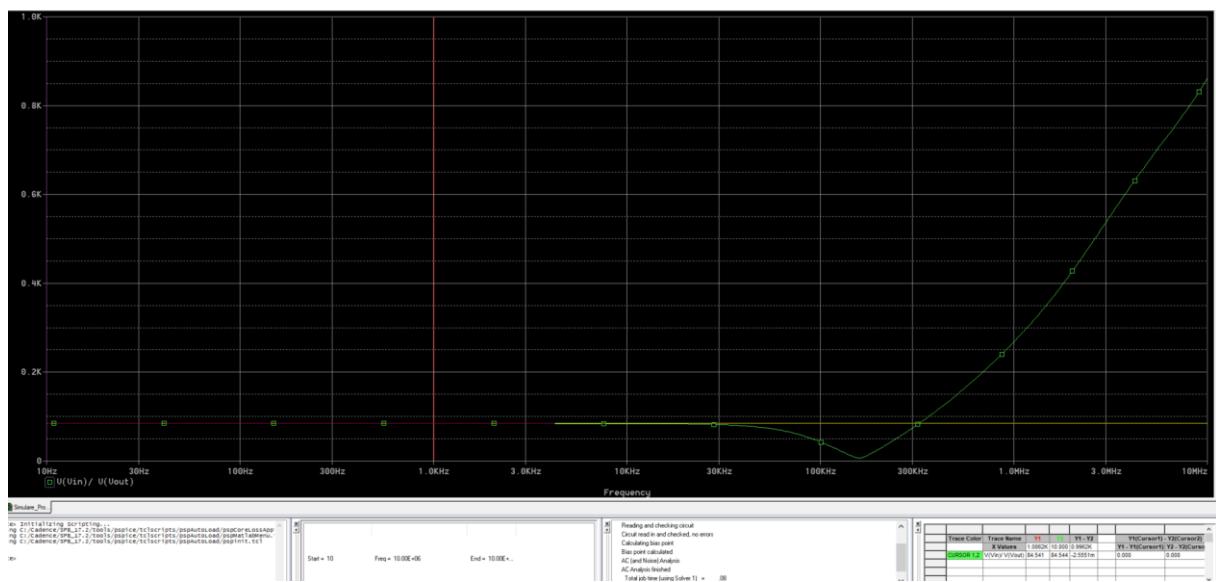
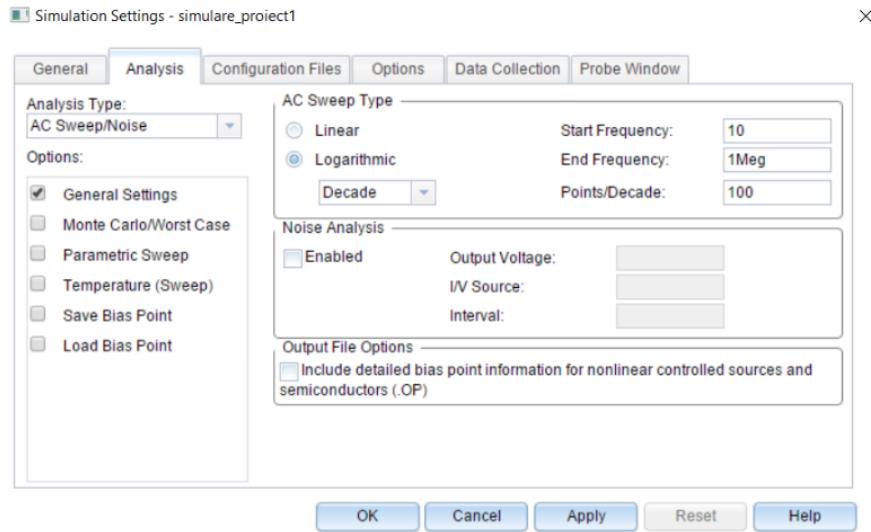


Fig. 4.11



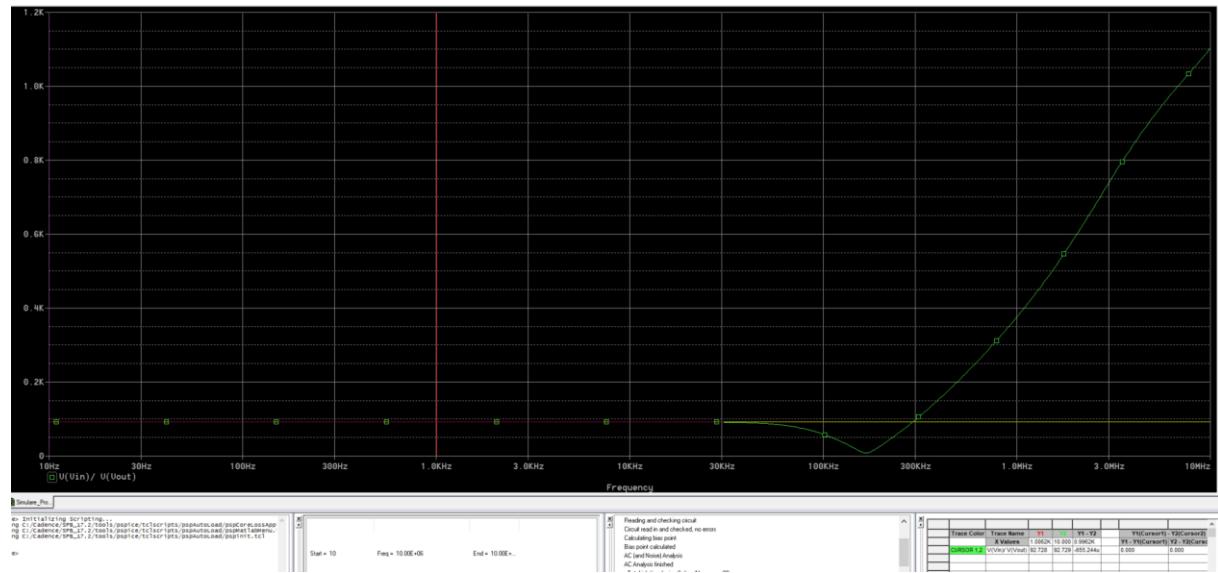
**Fig. 4.12**

For  $V_{in} = 26 \text{ V}$  and  $V_{out} = 22 \text{ V}$  (SET = 0) (Fig. 4.11)

According to the graph, at the frequency of 1KHz, the value of  $S = 84.5 > 53$

I plotted  $V(Vin)/V(Vout)$  to find S.

This simulation is saved as *sim3.dat*



**Fig. 4.13**

For  $V_{in} = 26\text{V}$  and  $V_{out} = 20 \text{ V}$  (SET = 1) (Fig. 4.13)

According to the graph, at the frequency of 1 KHz, the value of  $S = 92.7 > 53$

I plotted  $V(Vin)/V(Vout)$  to find S.

## Overcurrent Protection Circuit Simulation

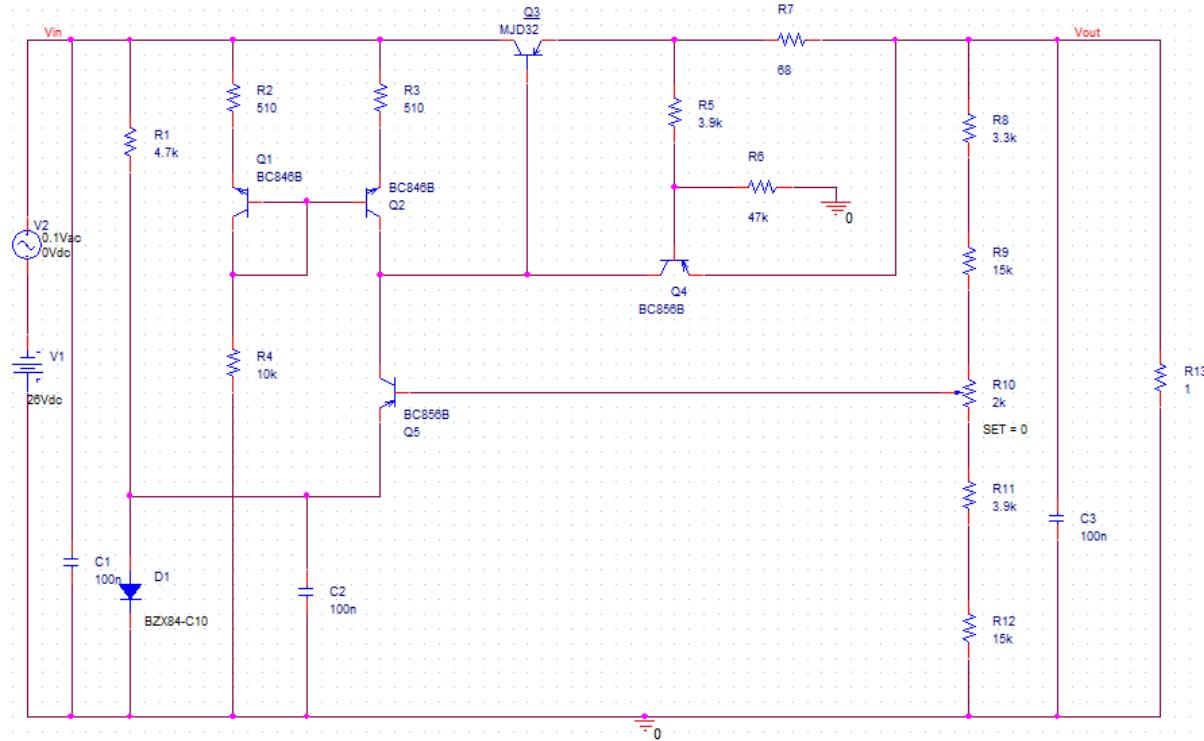


Fig. 4.14

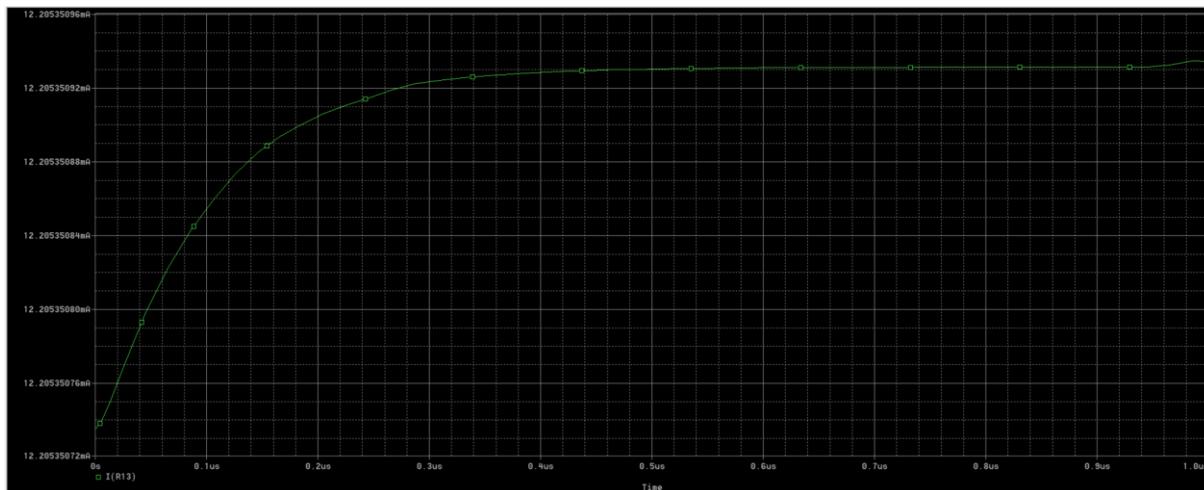
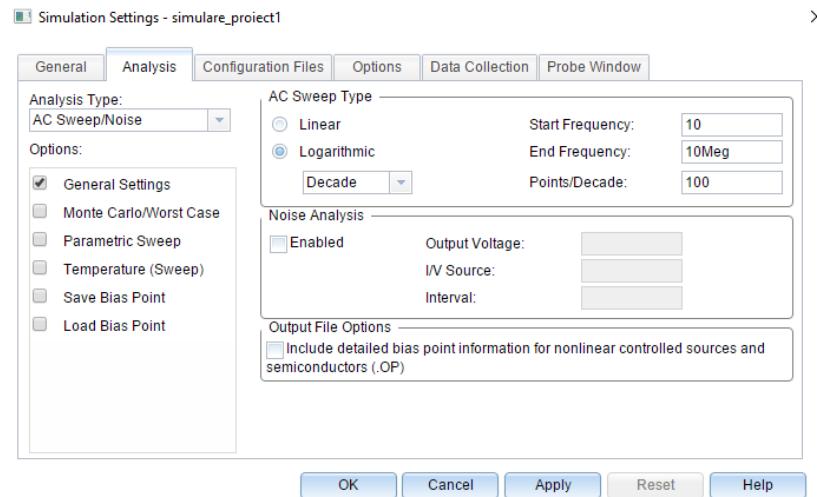


Fig. 4.15

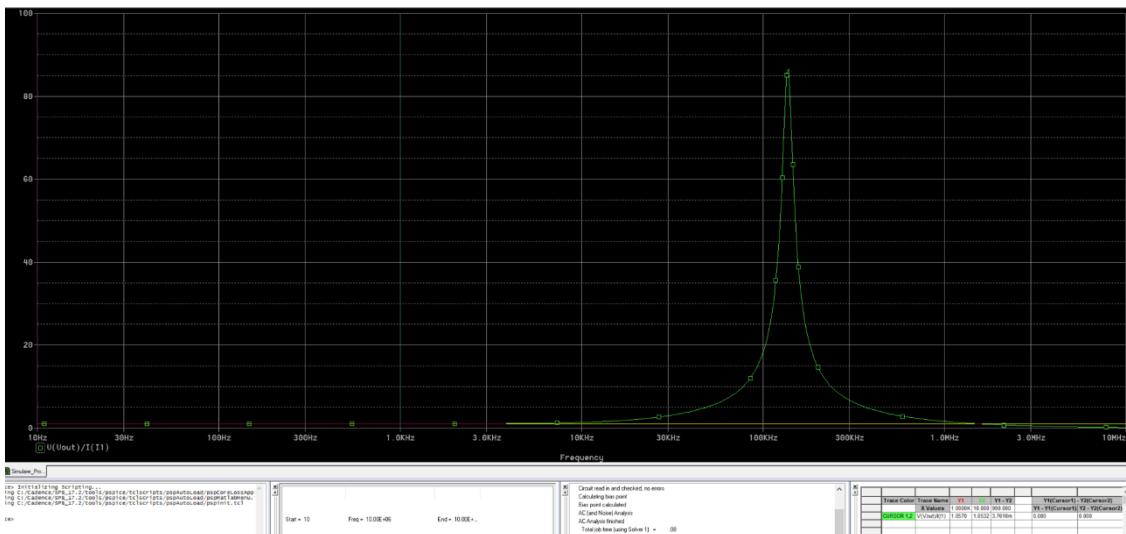
From this graph (Fig. 4.15), we can see that the shortcircuit current ( $I_{R13}$ ) is about 12.2 mA, still significantly less than  $I_{out\_max} = 26\text{mA}$ .

This simulation is saved as **sim4.dat**

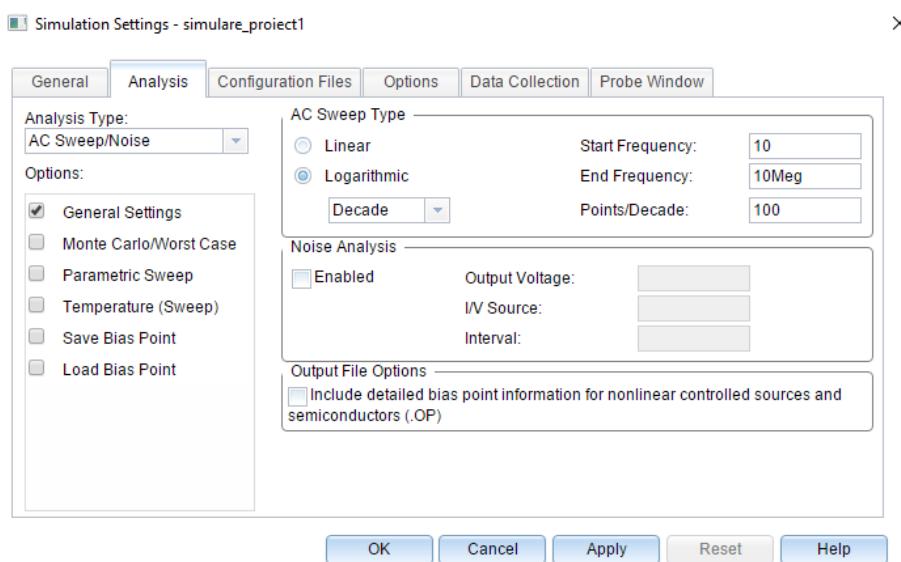


**Fig. 4.16**

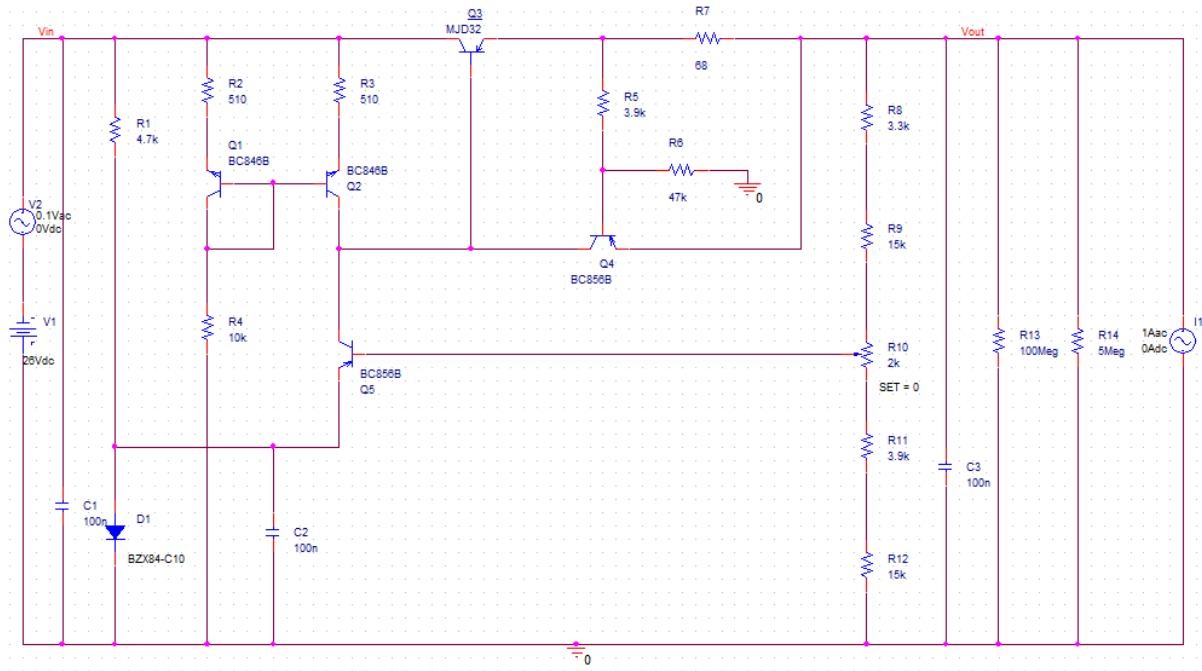
## Ro Simulation



**Fig. 4.17**



**Fig. 4.18**



**Fig. 4.19**

At the frequency of 1KHz,  $\text{Ro} = 1 \text{ Ohm} < 2 \text{ Ohm}$ . (from the graph in Fig. 4.17)

This simulation is saved as *sim5.dat*

## **5. Comments/Conclusions**

I have learnt a lot about voltage regulators while working on this project.

For simplicity, I used a single transistor as error amplifier instead of making a differential amplifier with two transistors.

Because the standard values for resistors are quite limiting, I had to use more resistors than I initially placed in the negative feedback circuit so that I got as close to the theoretical values as possible. This has also helped me obtain more accurate  $V_{out}$  values.

I found some parts of this project a bit challenging, but I consulted the lectures, seminars and laboratories from DE and CEF and I got some more clarifications from there.

## 6. Layout

### PCB schematic

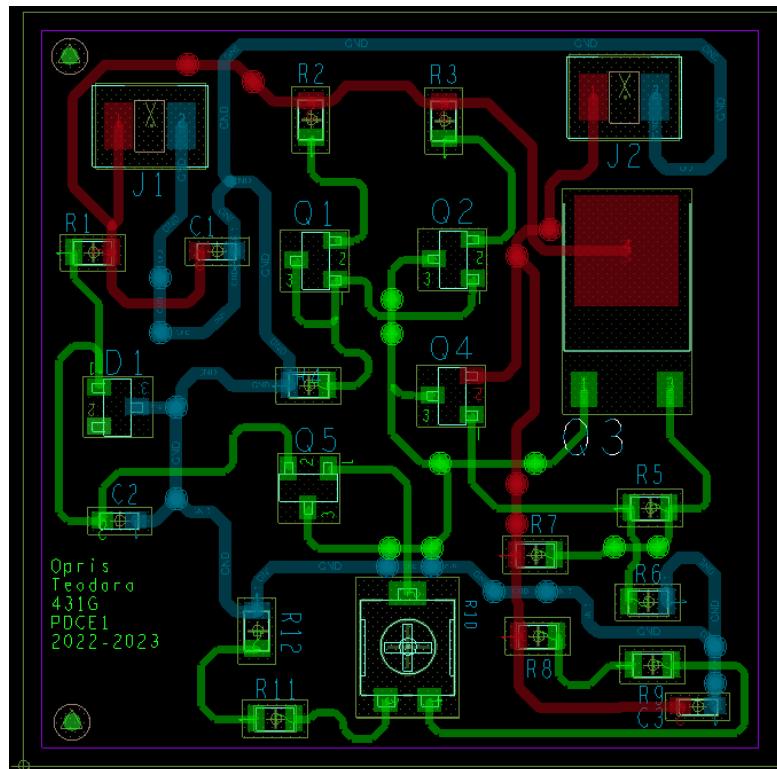


Fig. 6.1

### Board Outline

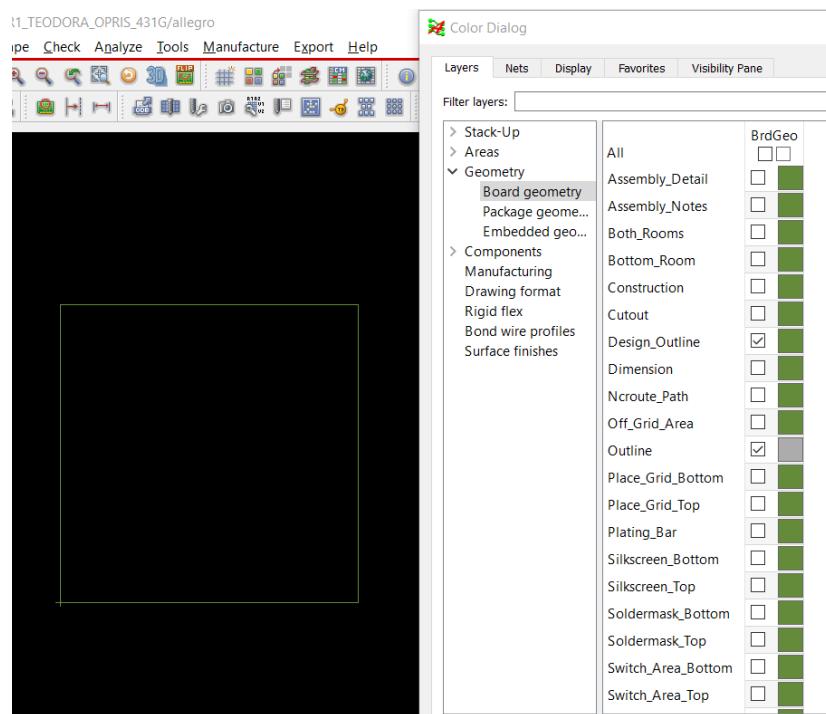
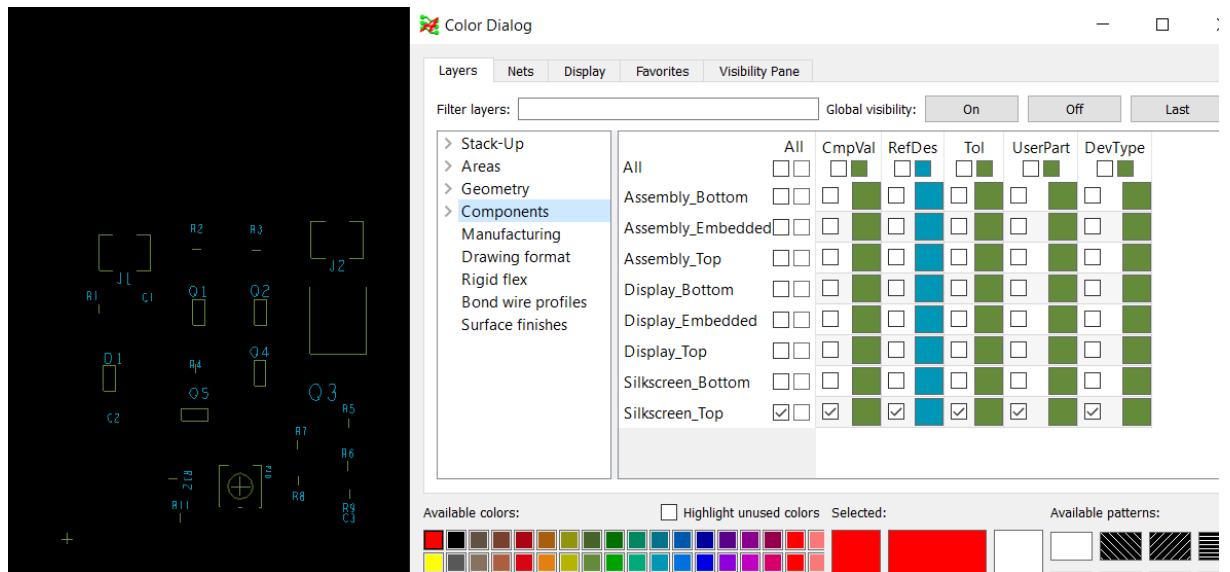
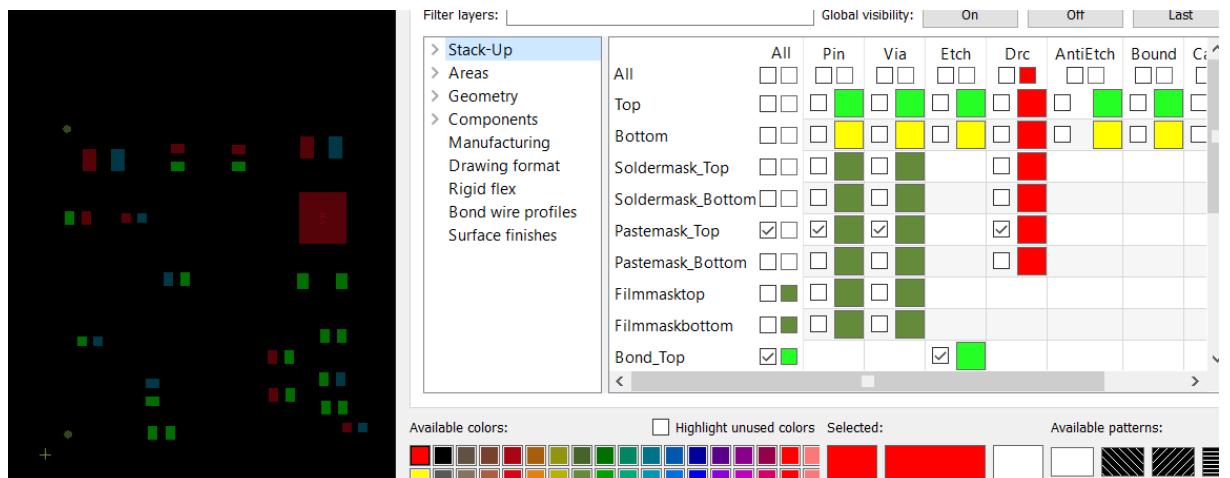


Fig. 6.2

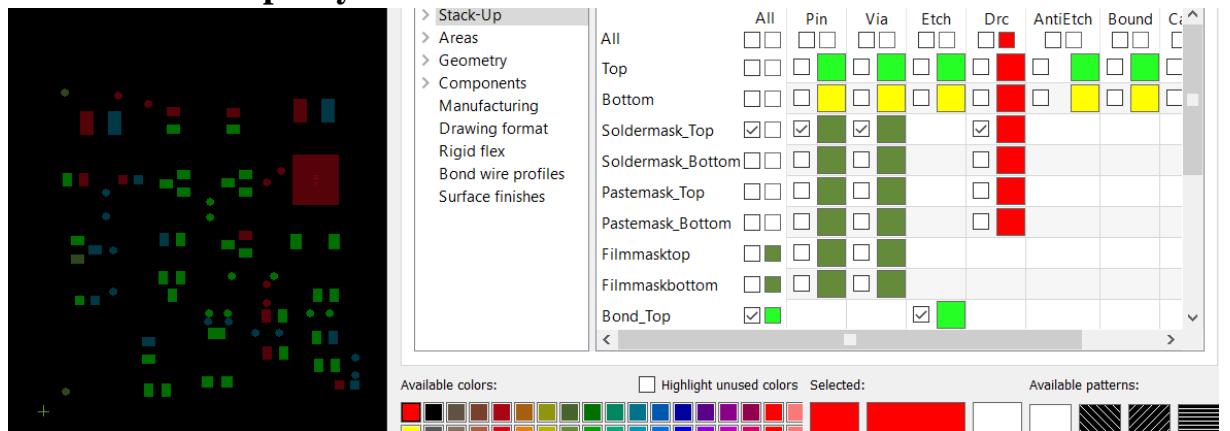
## Silkscreen Top Layer



## Paste Mask Top Layer

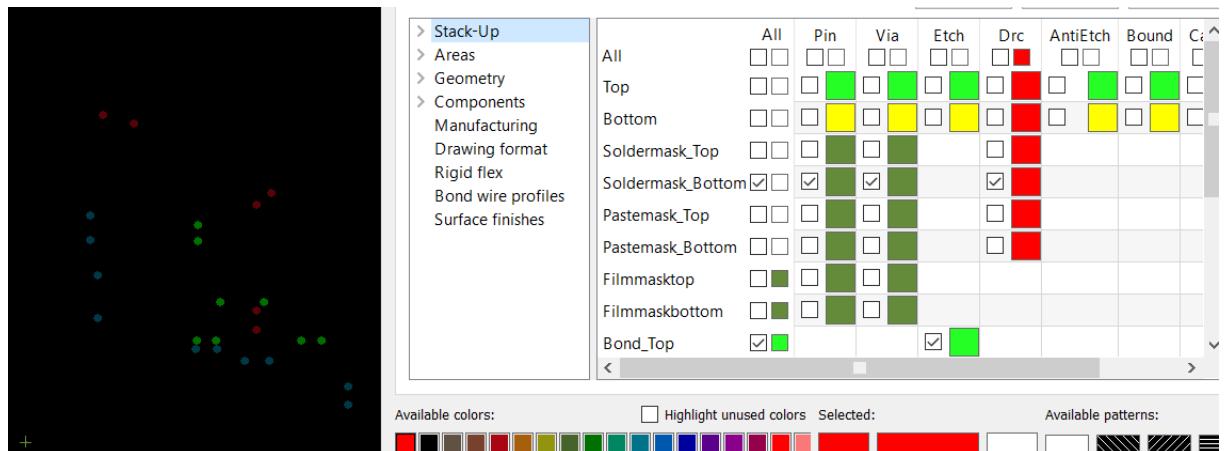


## Solder Mask Top Layer



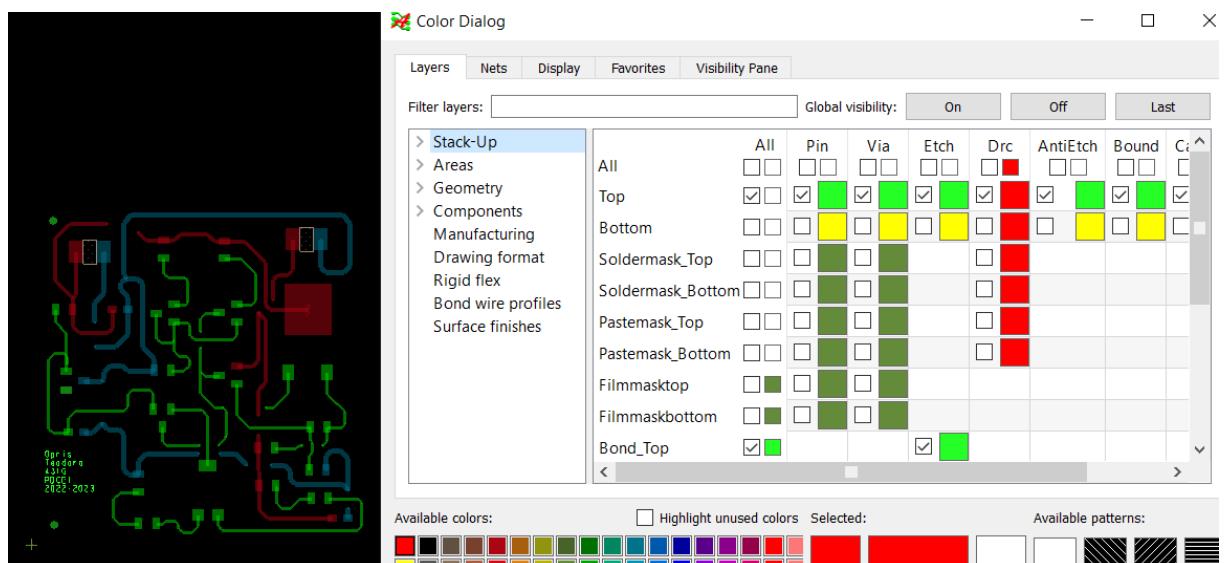
## Solder Mask Bottom Layer

Fig. 6.6



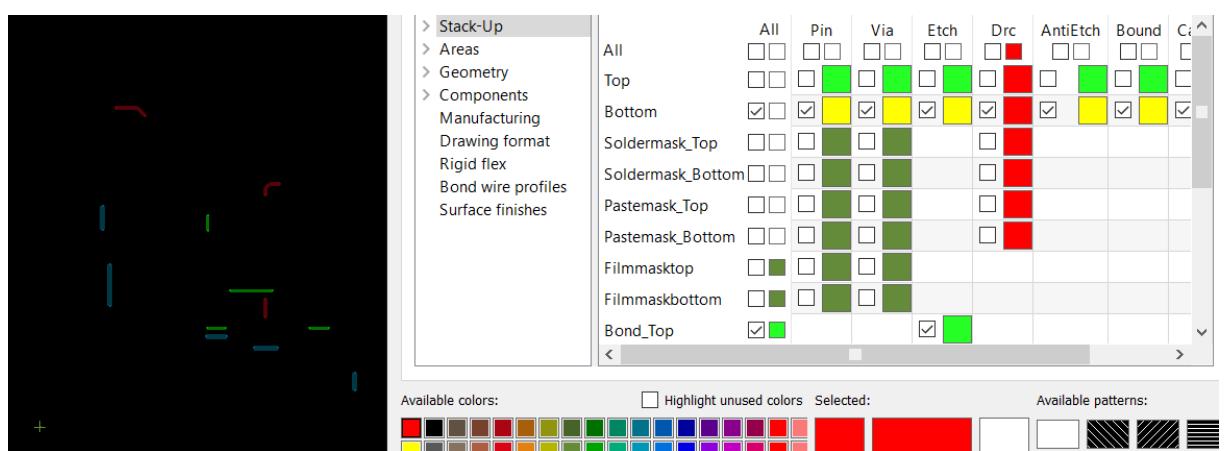
## Copper Layer Top Layer

Fig. 6.7



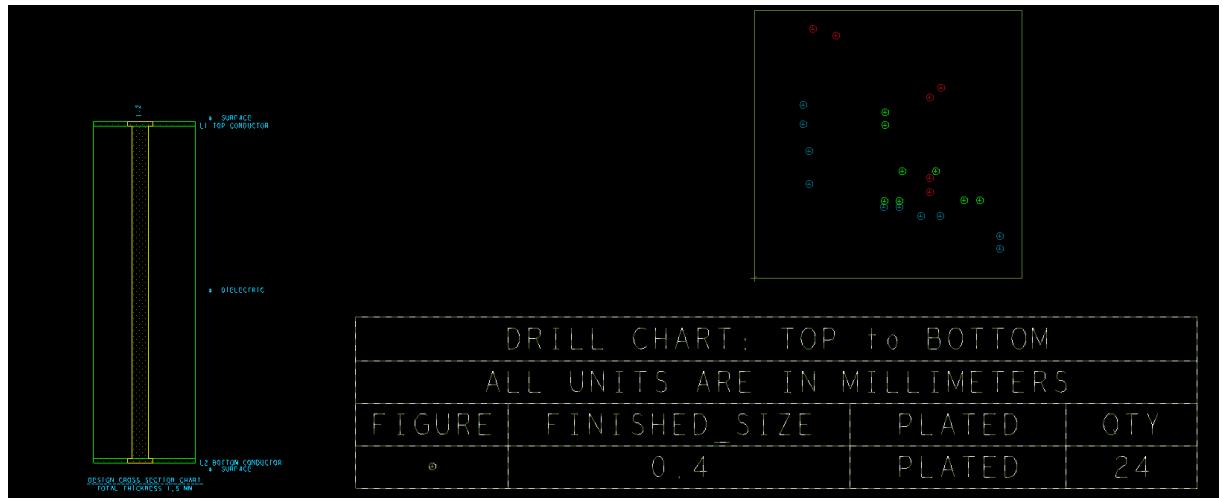
## Copper Layer Bottom Layer

Fig. 6.8



## Mechanical Layer

Fig. 6.9



## 7. Bibliography

- 1) L. Teodorescu, [http://wiki.dcae.pub.ro/images/7/79/Linear\\_regulator.pdf](http://wiki.dcae.pub.ro/images/7/79/Linear_regulator.pdf)
- 2) BZX84-C10 datasheet,  
[https://www.tme.eu/Document/17496f94aed149a6280f8105698167e8/BZX84\\_SER.pdf](https://www.tme.eu/Document/17496f94aed149a6280f8105698167e8/BZX84_SER.pdf)
- 3) BC856B datasheet,  
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- 4) BC846B datasheet,  
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