

UFERN



Projeto Marcapasso

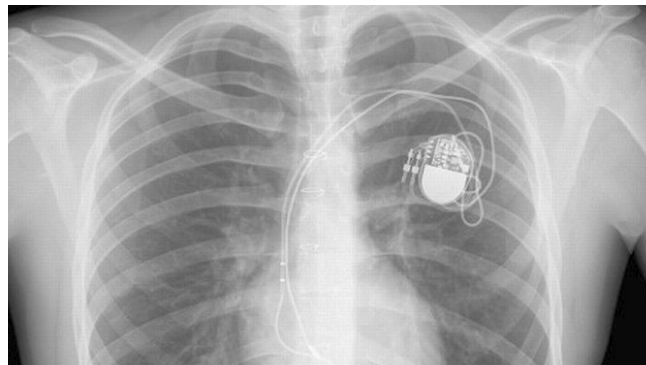
Circuitos Digitais

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DCA

Marcapasso

O marcapasso atrioventricular é um dispositivo implantável que se conecta por eletrodos ao coração, sendo capaz de monitorar o ritmo cardíaco e estimular o mesmo, evitando que os batimentos fiquem abaixo do nível normal.



Processo de Design do Controlador

CAPTURA (FSM)

Criação do FSM que descreve o comportamento do bloco de controle.

ARQUITETURA

Utilizando um registrador de estados se cria uma arquitetura padrão.

CODIFICAR

Utilização de binários para cada estado através de bits (o mínimo possível).

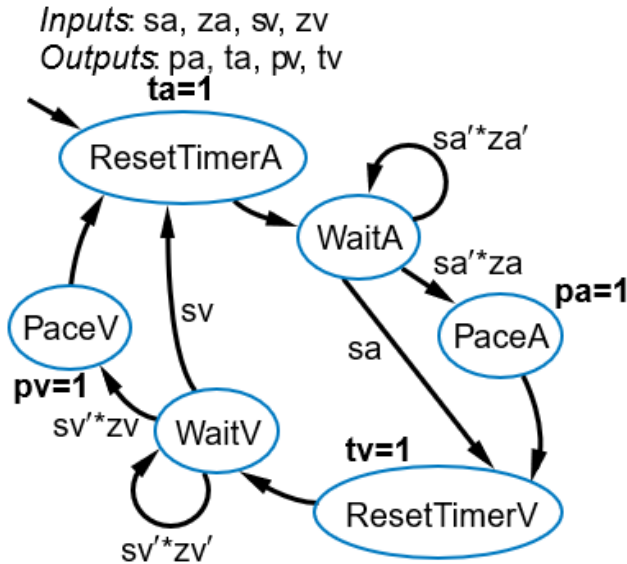
TABELA VERDADE

Criação da tabela verdade para a lógica combinacional.

IMPLEMENTAÇÃO

Elaboração da lógica combinacional e registrador de estados.

Captura



- Máquina de estados finitos (FSM)
- Entradas e Saídas
- Instantes dos Processos

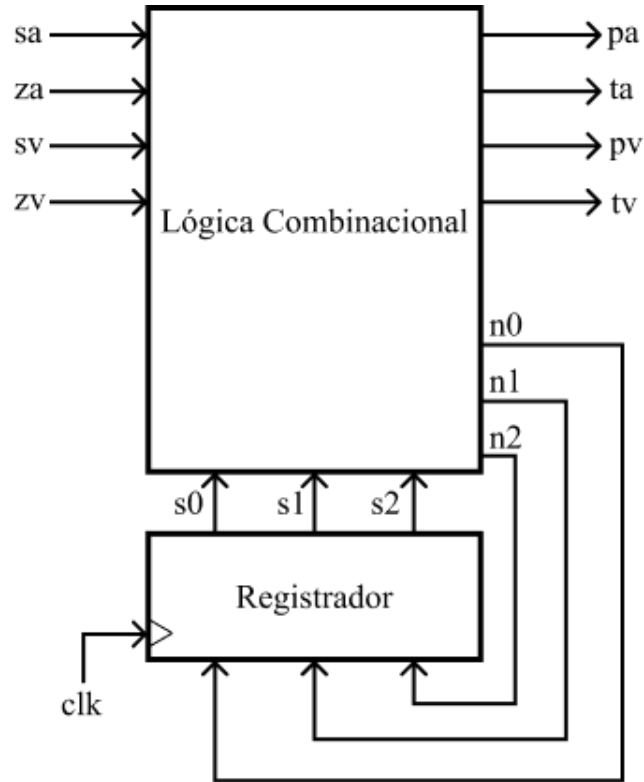
Inputs:

- sa = sensor pulso do átrio
- sv = sensor pulso de ventrículo
- za = timer do átrio
- zv = timer do ventrículo

Outputs:

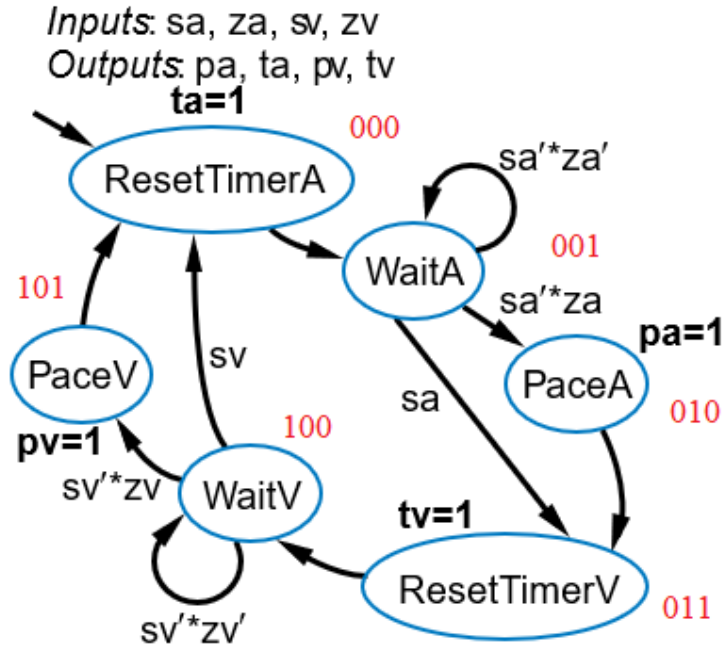
- pa = pulso no átrio
- ta = reset timer do átrio
- pv = pulso no ventrículo
- tv = reset timer do ventrículo

Arquitetura



- Bloco de Controle
- Registrador
- Lógica Combinacional

Codificação



- Processo
- N° de Estados
- N° de Bits
- Estados Codificados

Tabela Verdade (ResetTimerA)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
ResetTimerA	0	0	0	0	0	0	0	0	1	0	0	0	0	1
	0	0	0	1	0	0	0	0	1	0	0	0	0	1
	0	0	1	0	0	0	0	0	1	0	0	0	0	1
	0	0	1	1	0	0	0	0	1	0	0	0	0	1
	0	1	0	0	0	0	0	0	1	0	0	0	0	1
	0	1	0	1	0	0	0	0	1	0	0	0	0	1
	0	1	1	0	0	0	0	0	1	0	0	0	0	1
	0	1	1	1	0	0	0	0	1	0	0	0	0	1
	1	0	0	0	0	0	0	0	1	0	0	0	0	1
	1	0	0	1	0	0	0	0	1	0	0	0	0	1
	1	0	1	0	0	0	0	0	1	0	0	0	0	1
	1	0	1	1	0	0	0	0	1	0	0	0	0	1
	1	1	0	0	0	0	0	0	1	0	0	0	0	1
	1	1	0	1	0	0	0	0	1	0	0	0	0	1
	1	1	1	0	0	0	0	0	1	0	0	0	0	1
	1	1	1	1	0	0	0	0	1	0	0	0	0	1

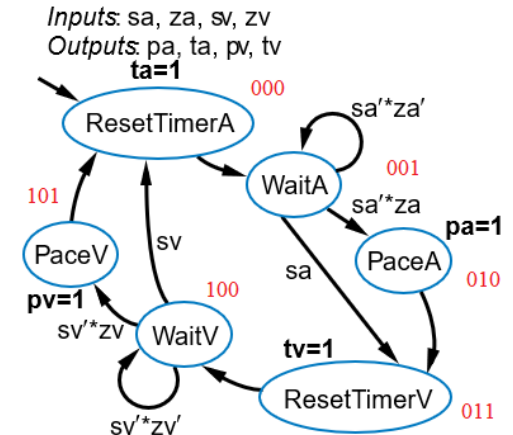


Tabela Verdade (WaitA)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
WaitA	0	0	0	0	0	0	1	0	0	0	0	0	0	1
	0	0	0	1	0	0	1	0	0	0	0	0	0	1
	0	0	1	0	0	0	1	0	0	0	0	0	0	1
	0	0	1	1	0	0	1	0	0	0	0	0	0	1
	0	1	0	0	0	0	1	0	0	0	0	0	1	0
	0	1	0	1	0	0	1	0	0	0	0	0	1	0
	0	1	1	0	0	0	1	0	0	0	0	0	1	0
	0	1	1	1	0	0	1	0	0	0	0	0	1	0
	1	0	0	0	0	0	1	0	0	0	0	0	1	1
	1	0	0	1	0	0	1	0	0	0	0	0	1	1
	1	0	1	0	0	0	1	0	0	0	0	0	1	1
	1	0	1	1	0	0	1	0	0	0	0	0	1	1
	1	1	0	0	0	0	1	0	0	0	0	0	1	1
	1	1	0	1	0	0	1	0	0	0	0	0	1	1
	1	1	1	0	0	0	1	0	0	0	0	0	1	1
	1	1	1	1	0	0	1	0	0	0	0	0	1	1

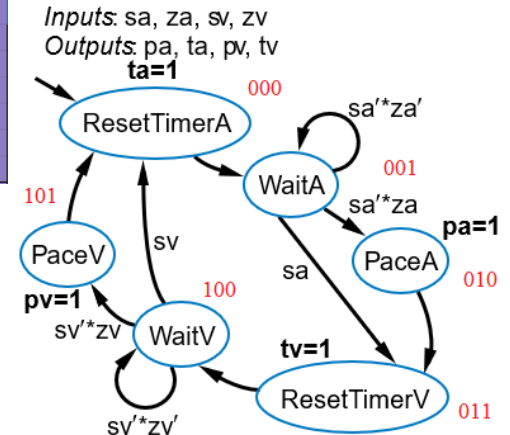


Tabela Verdade (PaceA)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
PaceA	0	0	0	0	0	1	0	1	0	0	0	0	1	1
	0	0	0	1	0	1	0	1	0	0	0	0	1	1
	0	0	1	0	0	1	0	1	0	0	0	0	1	1
	0	0	1	1	0	1	0	1	0	0	0	0	1	1
	0	1	0	0	0	1	0	1	0	0	0	0	1	1
	0	1	0	1	0	1	0	1	0	0	0	0	1	1
	0	1	1	0	0	1	0	1	0	0	0	0	1	1
	0	1	1	1	0	1	0	1	0	0	0	0	1	1
	1	0	0	0	0	1	0	1	0	0	0	0	1	1
	1	0	0	1	0	1	0	1	0	0	0	0	1	1
	1	0	1	0	0	1	0	1	0	0	0	0	1	1
	1	0	1	1	0	1	0	1	0	0	0	0	1	1
	1	1	0	0	0	1	0	1	0	0	0	0	1	1
	1	1	0	1	0	1	0	1	0	0	0	0	1	1
	1	1	1	0	0	1	0	1	0	0	0	0	1	1
	1	1	1	1	0	1	0	1	0	0	0	0	1	1

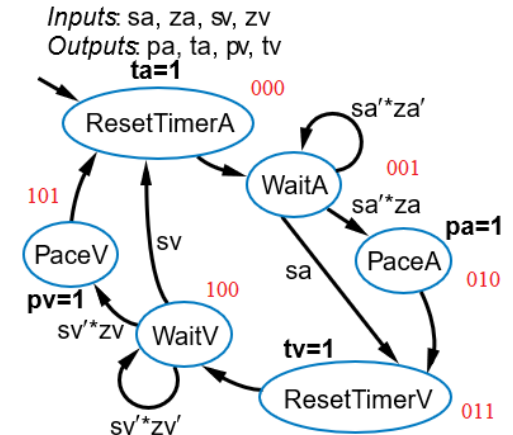


Tabela Verdade (ResetTimerV)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
ResetTimerV	0	0	0	0	0	1	1	0	0	0	1	1	0	0
	0	0	0	1	0	1	1	0	0	0	1	1	0	0
	0	0	1	0	0	1	1	0	0	0	1	1	0	0
	0	0	1	1	0	1	1	0	0	0	1	1	0	0
	0	1	0	0	0	1	1	0	0	0	1	1	0	0
	0	1	0	1	0	1	1	0	0	0	1	1	0	0
	0	1	1	0	0	1	1	0	0	0	1	1	0	0
	0	1	1	1	0	1	1	0	0	0	1	1	0	0
	1	0	0	0	0	1	1	0	0	0	1	1	0	0
	1	0	0	1	0	1	1	0	0	0	1	1	0	0
	1	0	1	1	0	1	1	0	0	0	1	1	0	0
	1	1	0	0	0	1	1	0	0	0	1	1	0	0
	1	1	0	1	0	1	1	0	0	0	1	1	0	0
	1	1	1	0	0	1	1	0	0	0	1	1	0	0
	1	1	1	1	0	1	1	0	0	0	1	1	0	0
	1	1	1	1	0	1	1	0	0	0	1	1	0	0

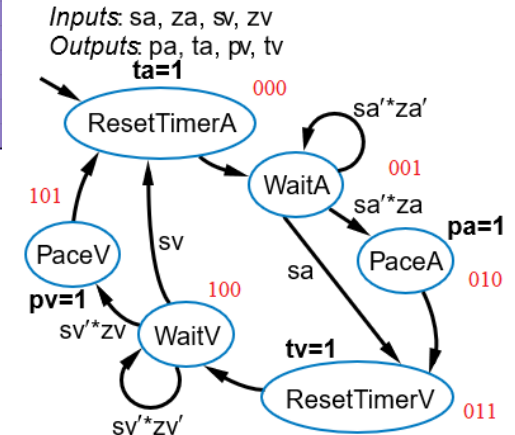


Tabela Verdade (WaitV)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
WaitV	0	0	0	0	1	0	0	0	0	0	0	1	0	0
	0	0	0	1	1	0	0	0	0	0	0	1	0	1
	0	0	1	0	1	0	0	0	0	0	0	0	0	0
	0	0	1	1	1	0	0	0	0	0	0	0	0	0
	0	1	0	0	1	0	0	0	0	0	0	1	0	0
	0	1	0	1	1	0	0	0	0	0	0	1	0	1
	0	1	1	0	1	0	0	0	0	0	0	0	0	0
	0	1	1	1	1	0	0	0	0	0	0	0	0	0
	1	0	0	0	1	0	0	0	0	0	0	1	0	0
	1	0	0	1	1	0	0	0	0	0	0	1	0	1
	1	0	1	0	1	0	0	0	0	0	0	0	0	0
	1	0	1	1	1	0	0	0	0	0	0	0	0	0
	1	1	0	0	1	0	0	0	0	0	0	1	0	0
	1	1	0	1	1	0	0	0	0	0	0	1	0	1
	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	0	0	0	0	0	0	0	0

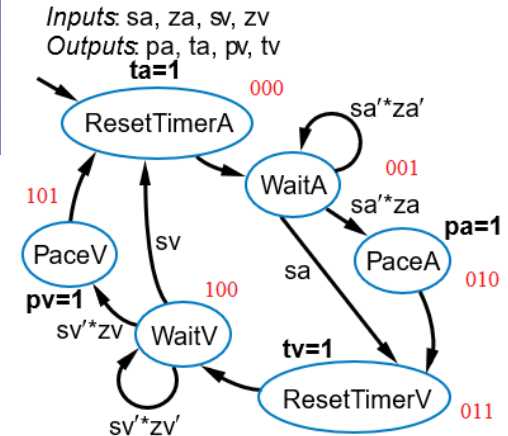


Tabela Verdade (PaceV)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
PaceV	0	0	0	0	1	0	1	0	0	1	0	0	0	0
	0	0	0	1	1	0	1	0	0	1	0	0	0	0
	0	0	1	0	1	0	1	0	0	1	0	0	0	0
	0	0	1	1	1	0	1	0	0	1	0	0	0	0
	0	1	0	0	1	0	1	0	0	1	0	0	0	0
	0	1	0	1	1	0	1	0	0	1	0	0	0	0
	0	1	1	0	1	0	1	0	0	1	0	0	0	0
	0	1	1	1	1	0	1	0	0	1	0	0	0	0
	1	0	0	0	1	0	1	0	0	1	0	0	0	0
	1	0	0	1	1	0	1	0	0	1	0	0	0	0
	1	0	1	0	1	0	1	0	0	1	0	0	0	0
	1	0	1	1	1	0	1	0	0	1	0	0	0	0
	1	1	0	0	1	0	1	0	0	1	0	0	0	0
	1	1	0	1	1	0	1	0	0	1	0	0	0	0
	1	1	1	0	1	0	1	0	0	1	0	0	0	0
	1	1	1	1	1	0	1	0	0	1	0	0	0	0

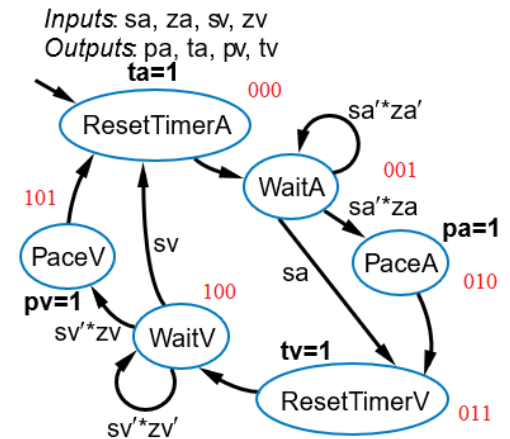
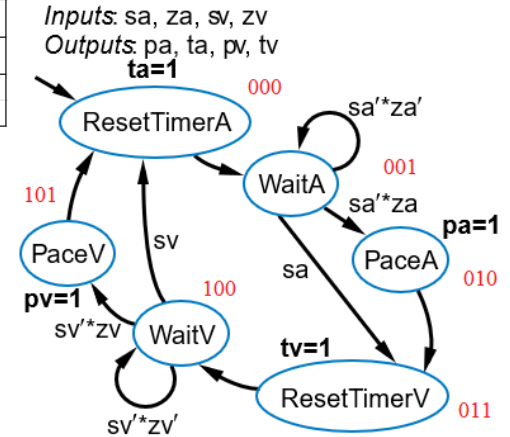


Tabela Verdade Simplificada (estados)

	INPUTS							OUTPUTS						
	sa	za	sv	zv	s2	s1	s0	pa	ta	pv	tv	n0	n1	n2
ResetTimerA	x	x	x	x	0	0	0	0	1	0	0	0	0	1
WaitA	0	0	x	x	0	0	1	0	0	0	0	0	0	1
	0	1	x	x	0	0	1	0	0	0	0	0	1	0
	1	x	x	x	0	0	1	0	0	0	0	0	1	1
PaceA	x	x	x	x	0	1	0	1	0	0	0	0	1	1
ResetTimerV	x	x	x	x	0	1	1	0	0	0	1	1	0	0
WaitV	x	x	0	0	1	0	0	0	0	0	0	1	0	0
	x	x	0	1	1	0	0	0	0	0	0	1	0	1
	x	x	1	x	1	0	0	0	0	0	0	0	0	0
PaceV	x	x	x	x	1	0	1	0	0	1	0	0	0	0
---					1	1	0							
					1	1	1							



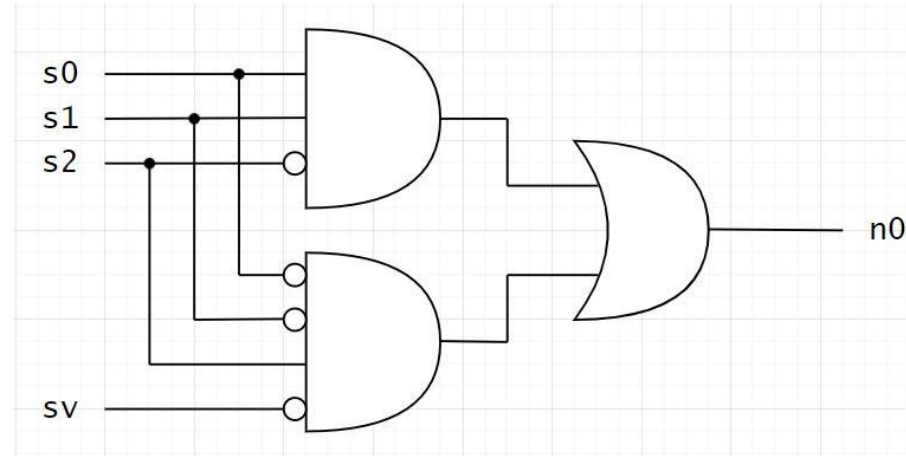
Lógica Combinacional - Exemplo n0

- Como as saídas dependem das entradas?
- Equações montadas
- Simplificação

$$n0 = (s2' \cdot s1 \cdot s0) + (sv' \cdot zv' \cdot s2 \cdot s1' \cdot s0') + (sv' \cdot zv \cdot s2 \cdot s1' \cdot s0')$$

$$n0 = s2' \cdot s1 \cdot s0 + sv' \cdot s2 \cdot s1' \cdot s0' \cdot (zv' + zv)$$

$$n0 = s2' \cdot s1 \cdot s0 + sv' \cdot s2 \cdot s1' \cdot s0'$$



Lógica Combinacional + Registrador de Estados

$$n0 = s2' \cdot s1 \cdot s0 + sv' \cdot s2 \cdot s1' \cdot s0'$$

$$n1 = s2' \cdot (s1' \cdot s0 \cdot (sa + za) + s1 \cdot s0')$$

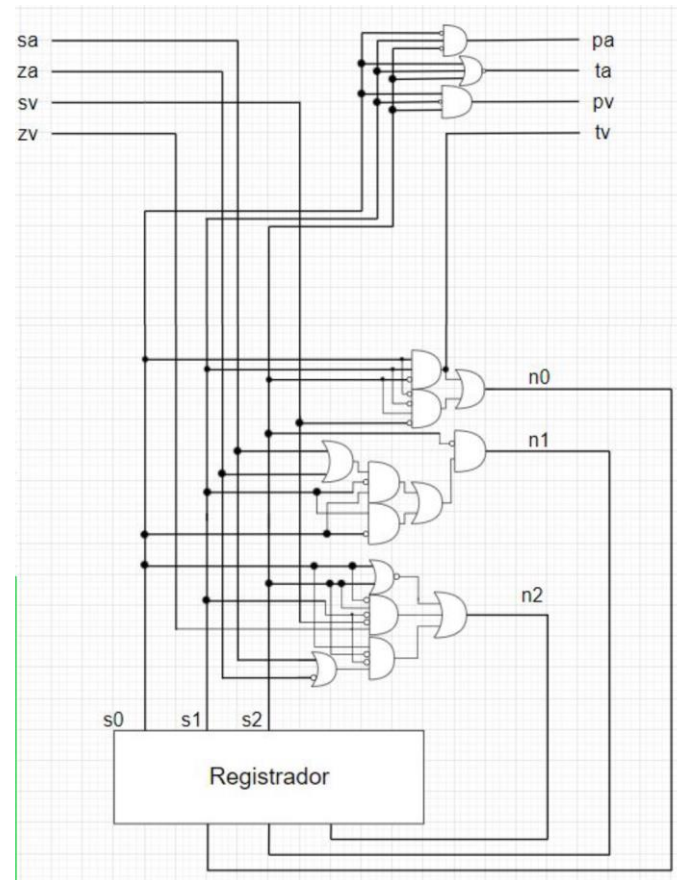
$$n2 = s0' \cdot s2' + s0' \cdot sv' \cdot zv \cdot s2 \cdot s1' + s2' \cdot s1' \cdot s0 \cdot (sa + za')$$

$$pa = s2' \cdot s1 \cdot s0'$$

$$ta = s2' \cdot s1' \cdot s0'$$

$$pv = s2 \cdot s1' \cdot s0$$

$$tv = s2' \cdot s1 \cdot s0$$



**OBIGADO PELA
ATENÇÃO!**