



Tephilla Prince <183061002@iitdh.ac.in>

[Research] BMC+LTL+SMT Tool

Tephilla Prince <183061002@iitdh.ac.in>

Thu, Apr 7, 2022 at 3:42 PM

To: Ramchandra Phawade <prb@iitdh.ac.in>, Sheerazuddin S <sheeraz@nitc.ac.in>

Dear Sir

Please find the forwarded email from Prof.Yann Thierry-Mieg,LIP6 (highlighted).

Based on searching online and Prof.Yann's reply, it seems like there are no BMC tools that have preceded ours.

Thanks
Tephilla

----- Forwarded message -----

From: Yann Thierry-Mieg <yann.thierry-mieg@lip6.fr>

Date: Thu, Apr 7, 2022 at 3:21 PM

To: Tephilla Prince <183061002@iitdh.ac.in>

Hi,

>tools to perform bounded model checking for petri nets using linear temporal logic, queried using SMT/SAT.

I'm not sure what you mean,

* LTL tools yes,

* BMC tools usually are for reachability properties rather than LTL, I guess one could try to encode using BMC the problem of reachability inside the product with an automaton, but I don't know of a tool that attempts that

* queried with SAT/SMT is usually the case when talking about BMC, that is what most ppl have in mind.

Currently ITS-tools does use a layer of SMT when solving LTL, we try to prove simpler assertions we call "knowledge" and combine them to simplify or even prove the property. But I would not call that BMC.

Best regards

ytm

=====

= Yann Thierry-Mieg
 = Maître de conférences, HDR
 = Labo. d'Informatique de Paris 6 (LIP6)
 = Equipe MoVe: Modelling and Verification
 = Sorbonne Université
 = 4 Place Jussieu
 = 25/26 Bureau 210
 = tel: +33-(0)1-44-27-71-04

=====

Le 2022-04-07 07:48, Tephilla Prince a écrit :

> Dear Prof.Yann

>

> I am a student researcher from IIITDh, India.

> We had interacted earlier regarding ITS-Tools.

>

> I would like to know, if you are aware of any tools to perform bounded model checking for petri nets using linear temporal logic, queried using SMT/SAT.

>
> Thank you very much for your time.
>
> Regards
> Tephilla