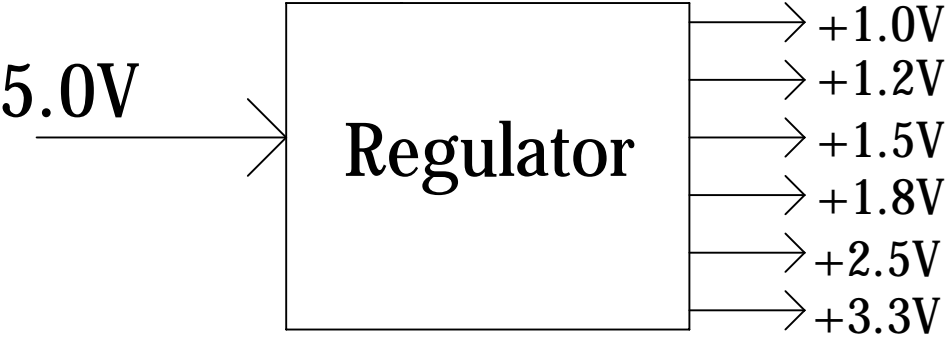
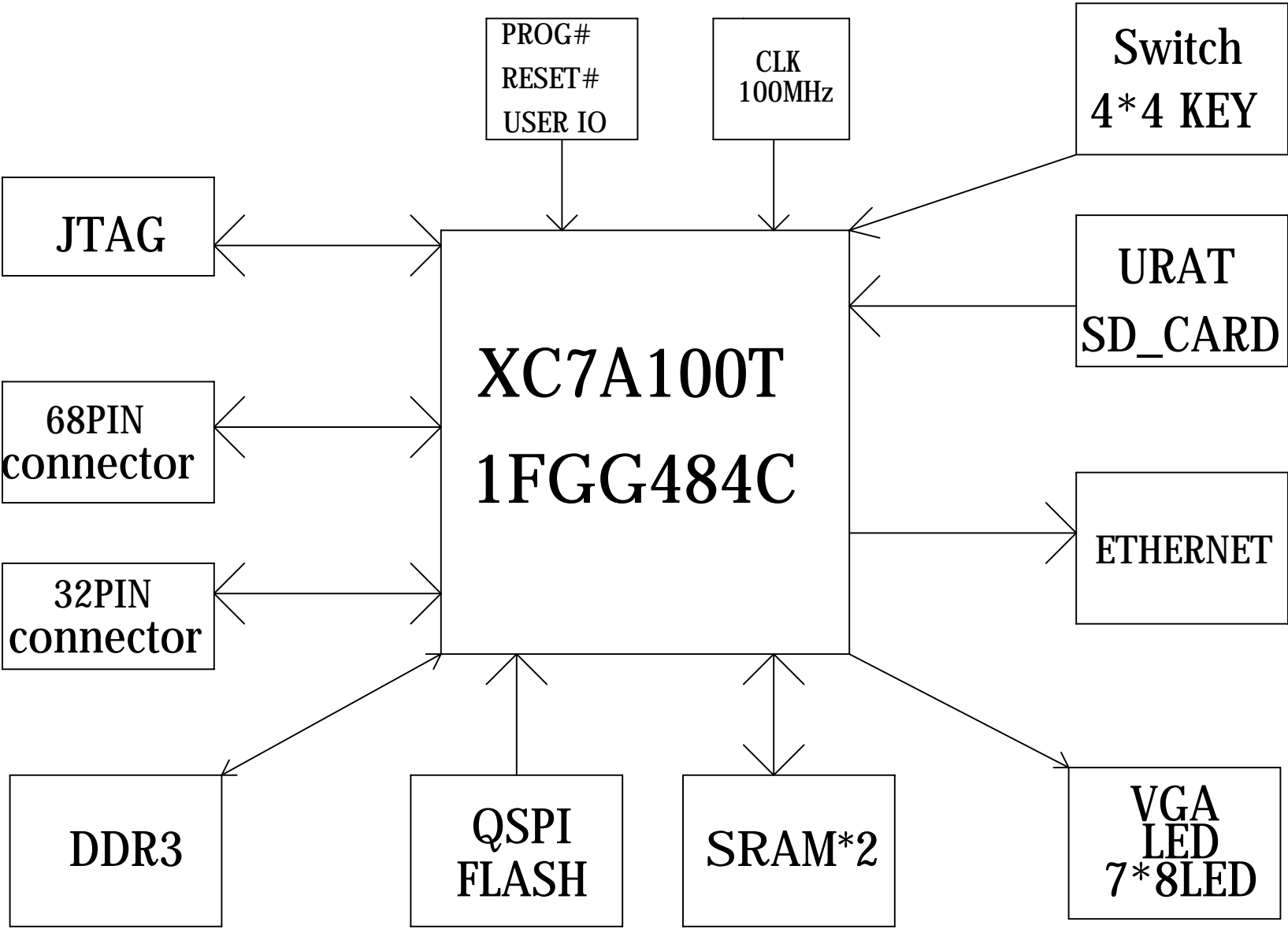


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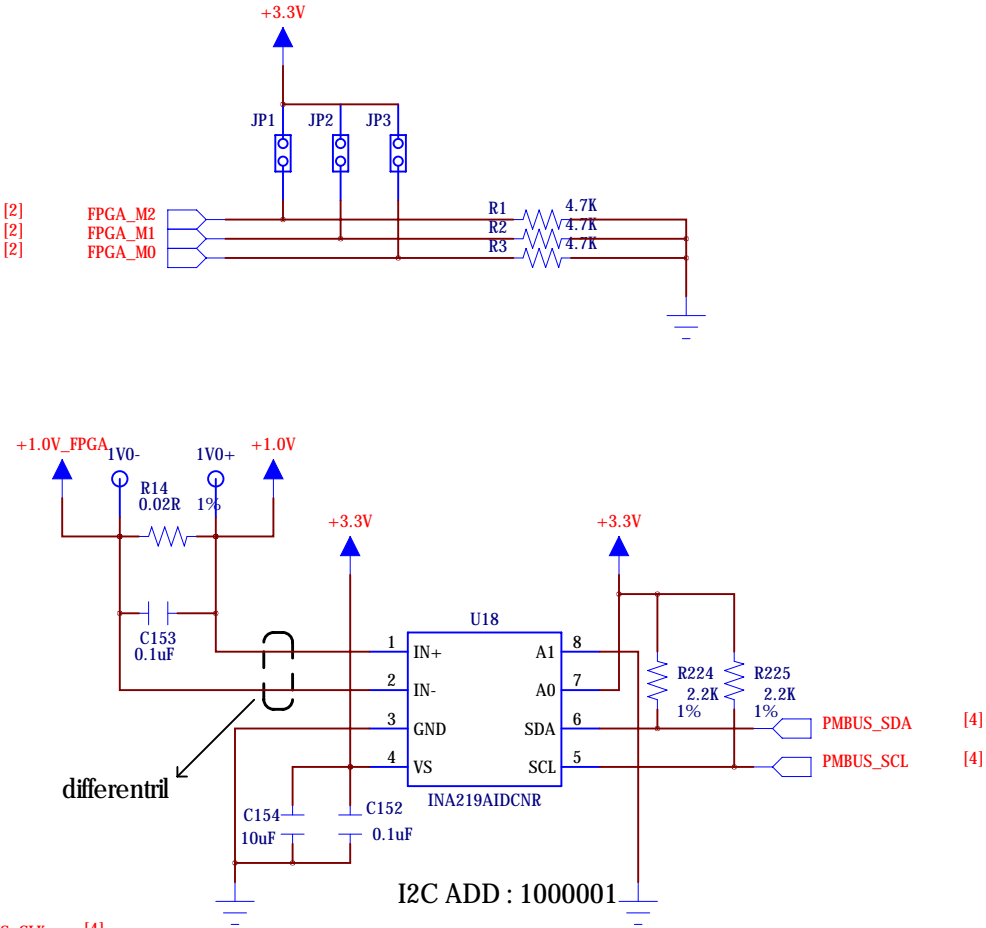
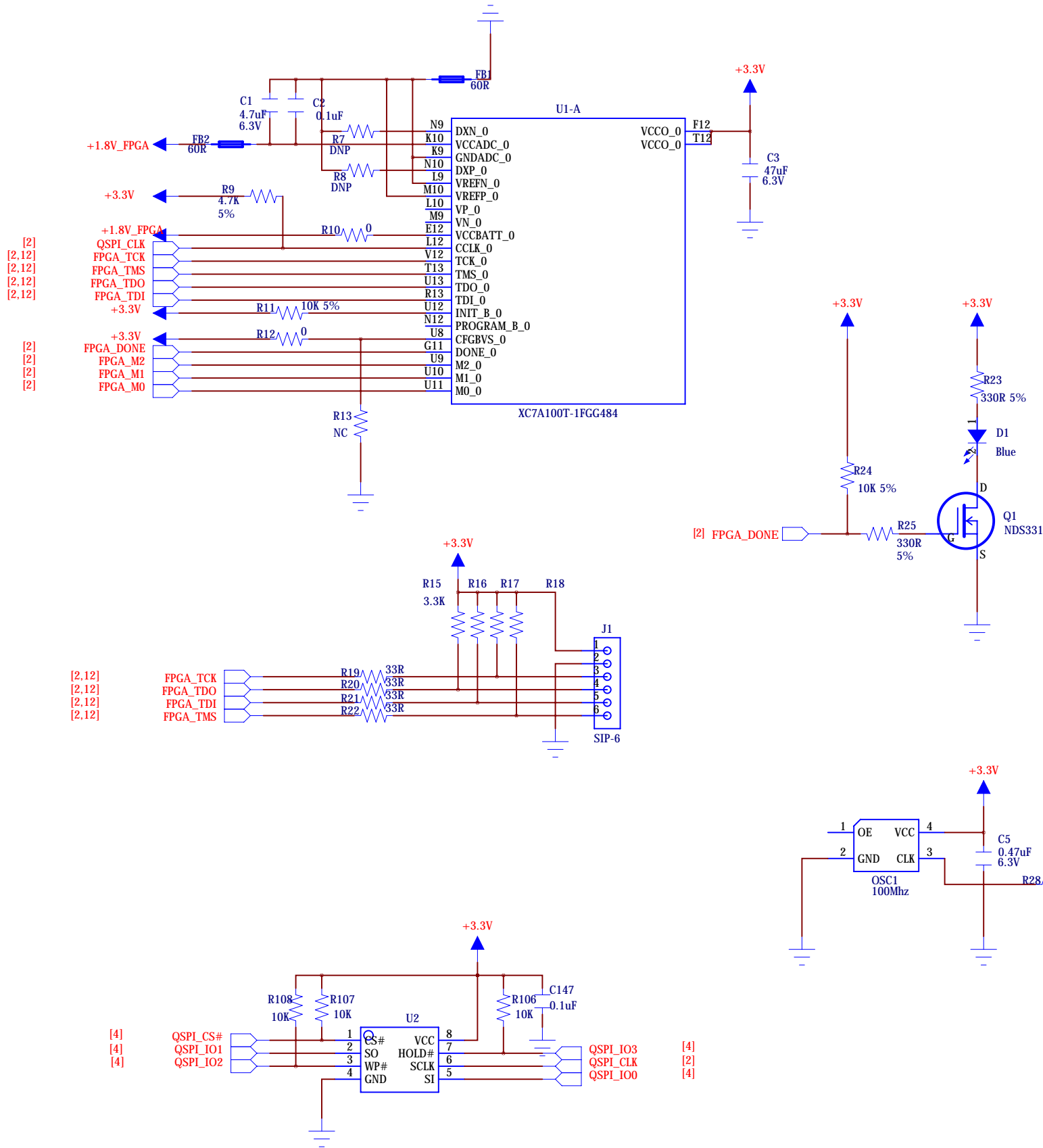
TITLE: 					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:1 OF 14
RELEASED:		E- ELEMENTS			

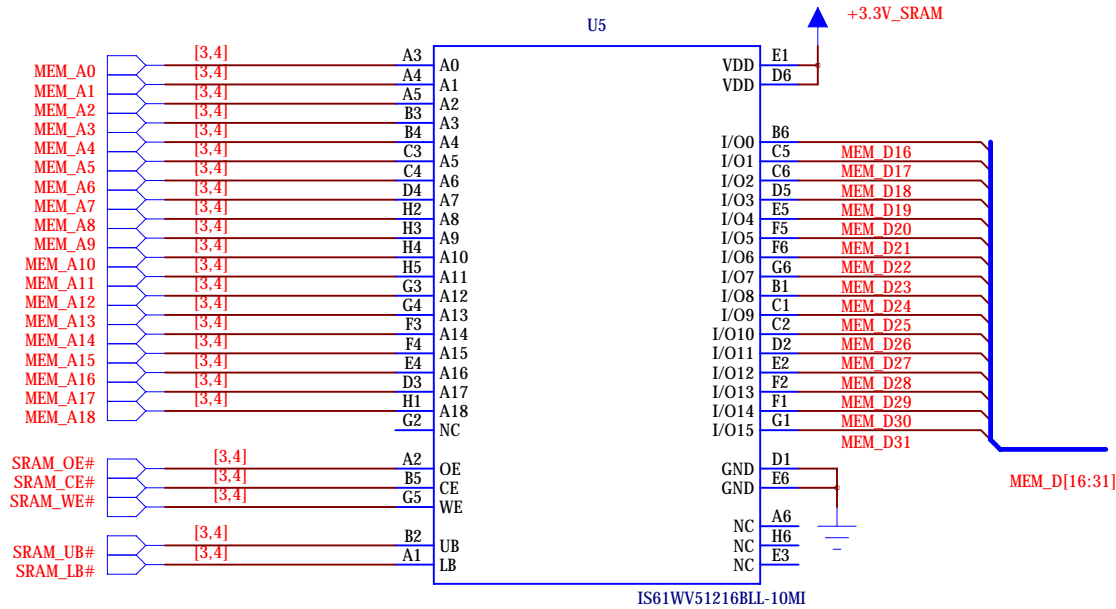
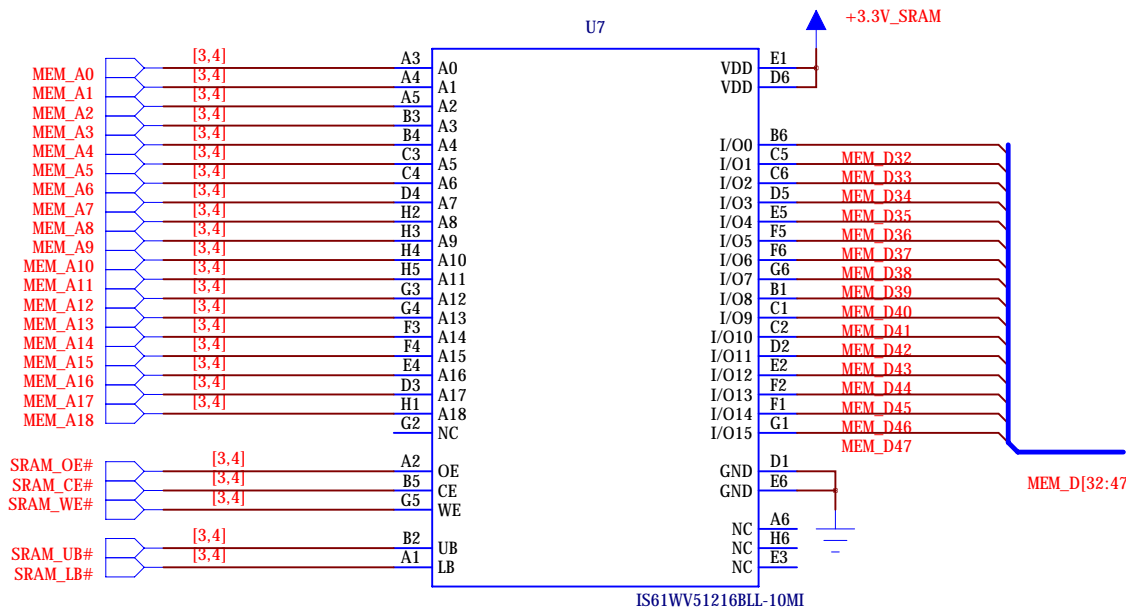
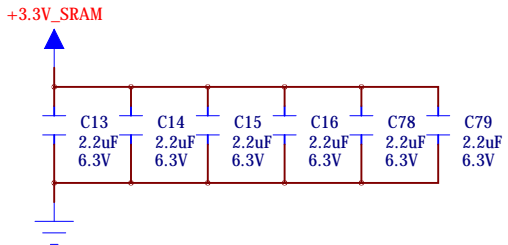
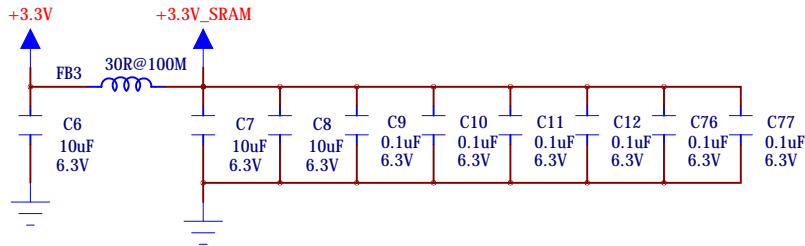
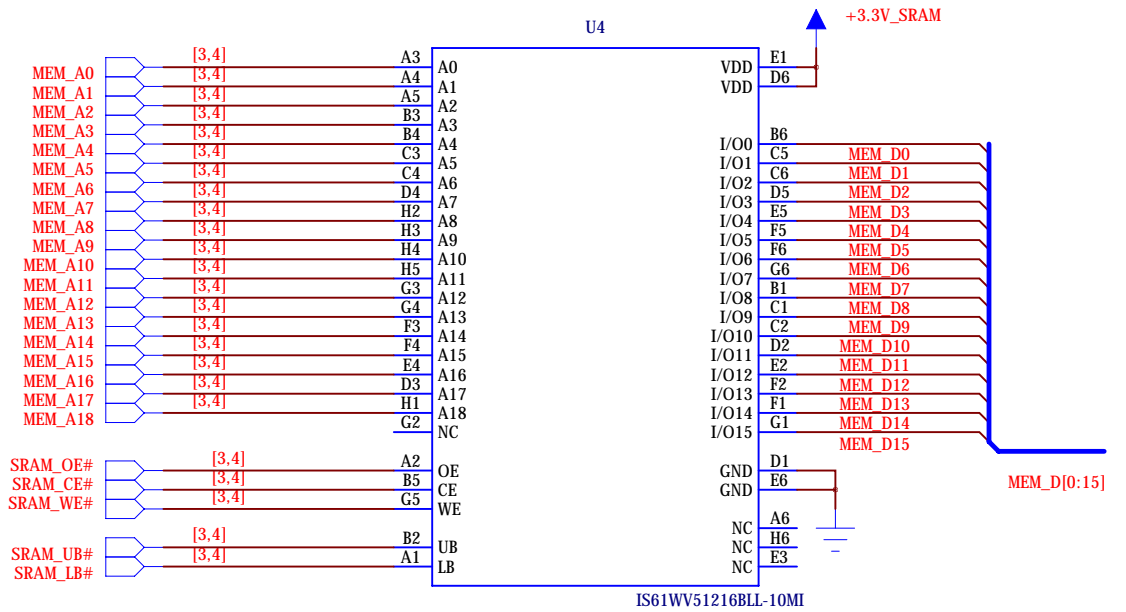
Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 <sup>(1)</sup>	Input
Slave Serial <sup>(2)</sup>	111	x1	Input



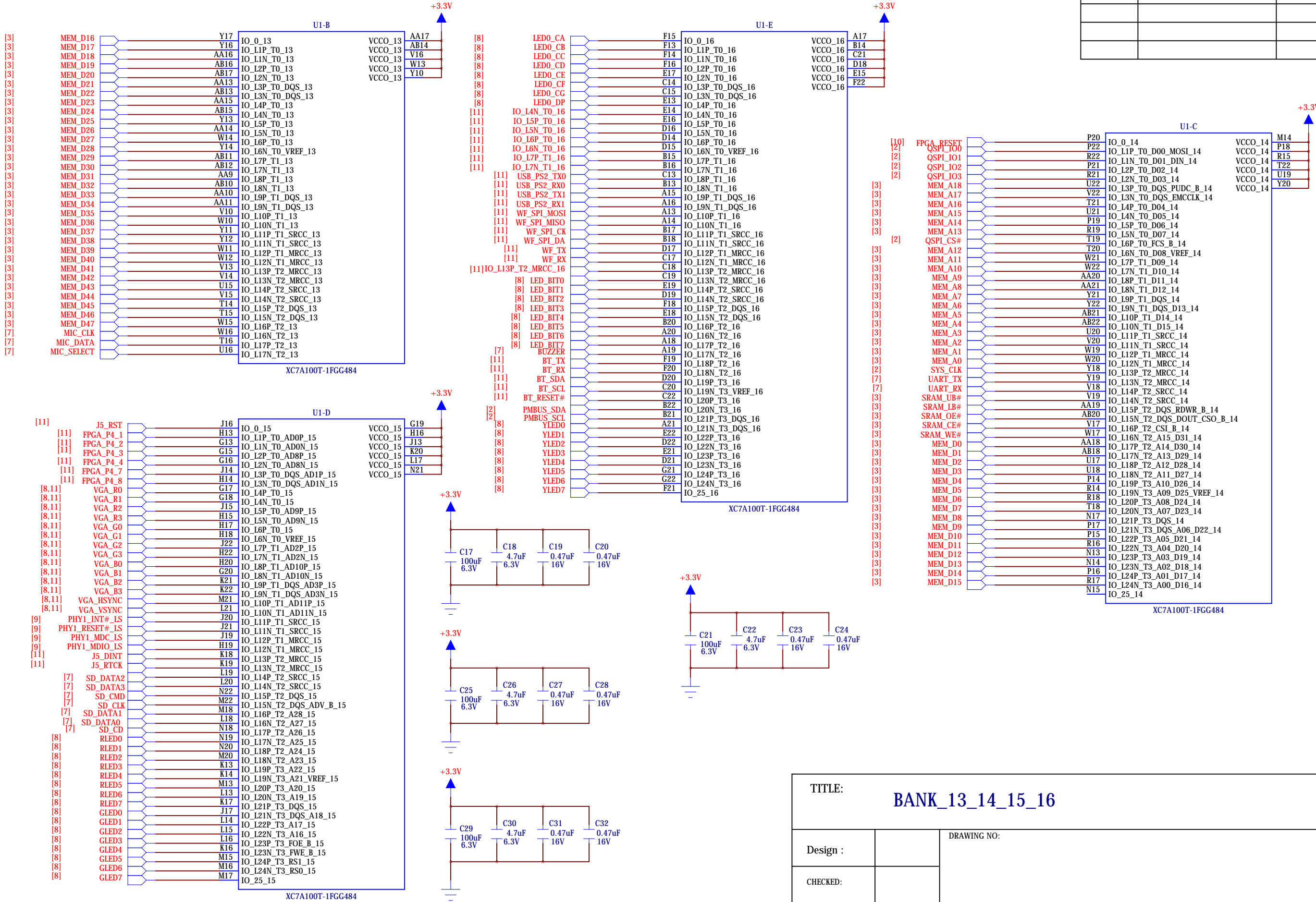
TITLE: <b>SYSTEM</b>					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: <b>A3</b>	SCALE:	SHEET:2 OF 14
RELEASED:		E- ELEMENTS			

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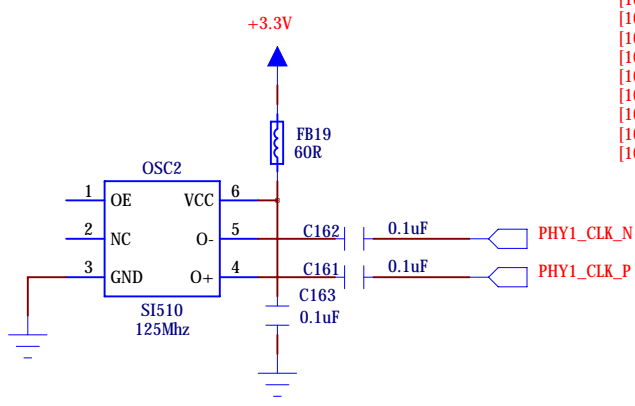
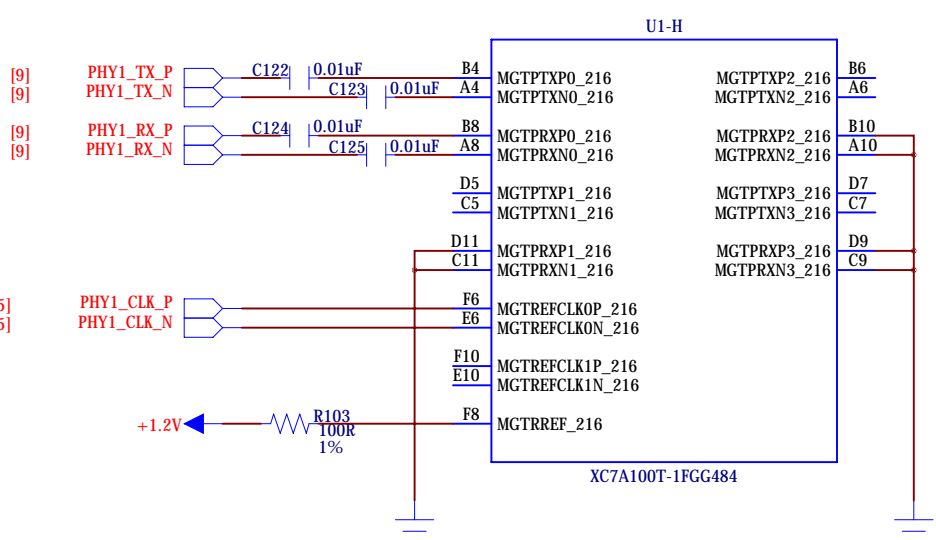
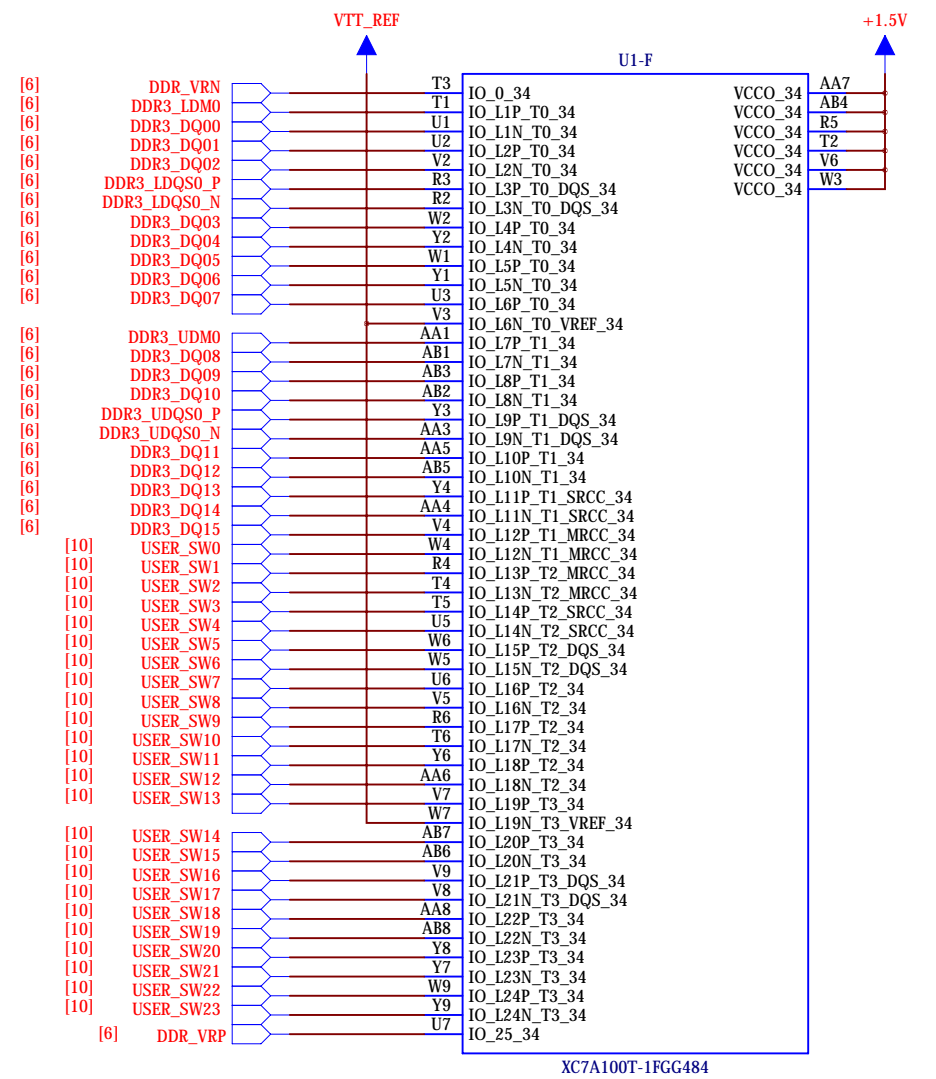
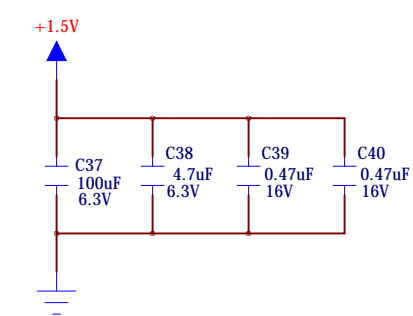
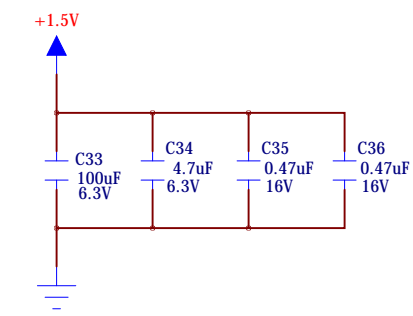
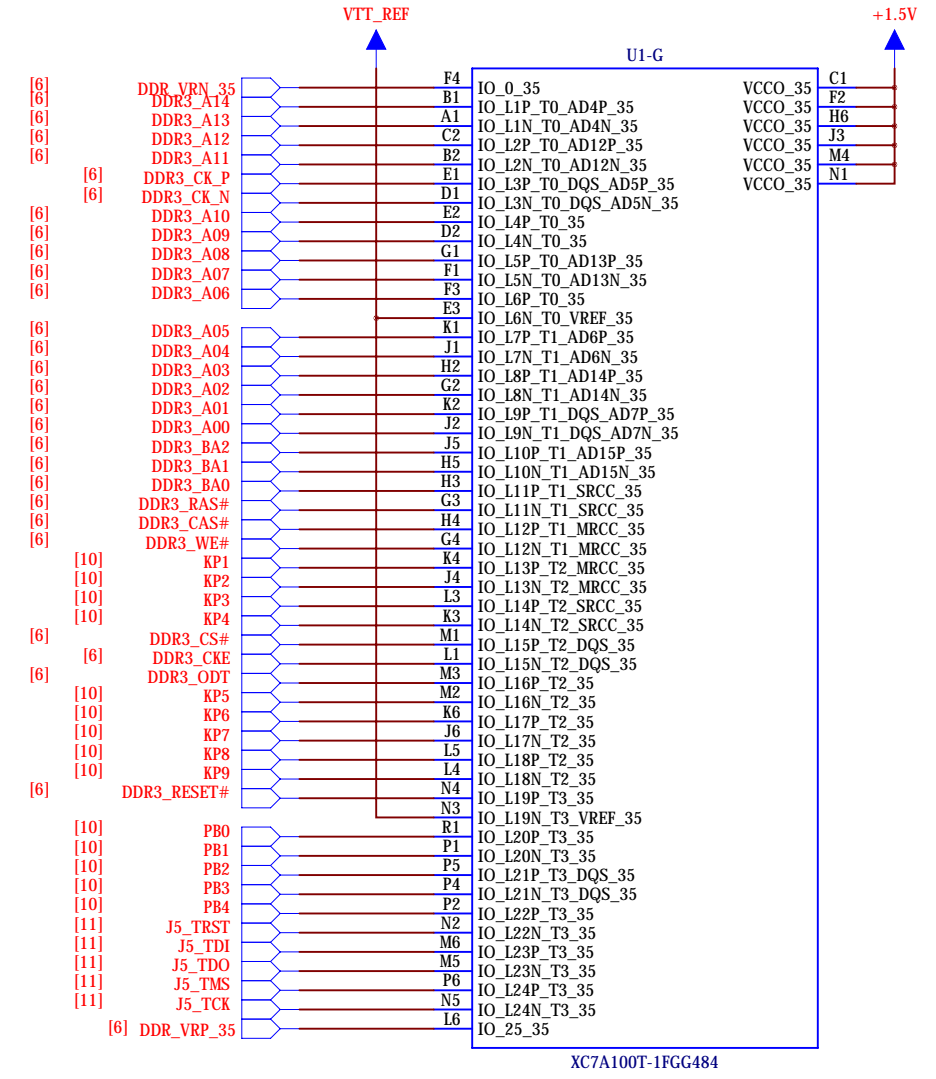
TITLE: SRAM					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:3 OF 14
RELEASED:		E- ELEMENTS			

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TITLE: BANK_13_14_15_16				
Design :		DRAWING NO:		
CHECKED:				
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:
RELEASED:		E-ELEMENTS		
		SHEET:4 OF 14		

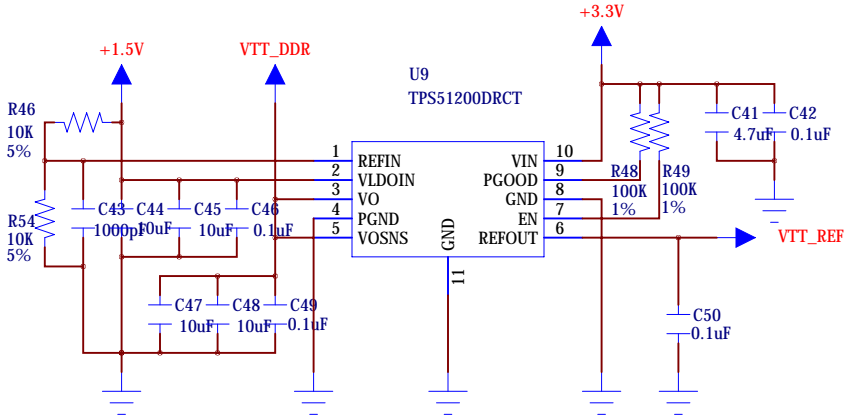
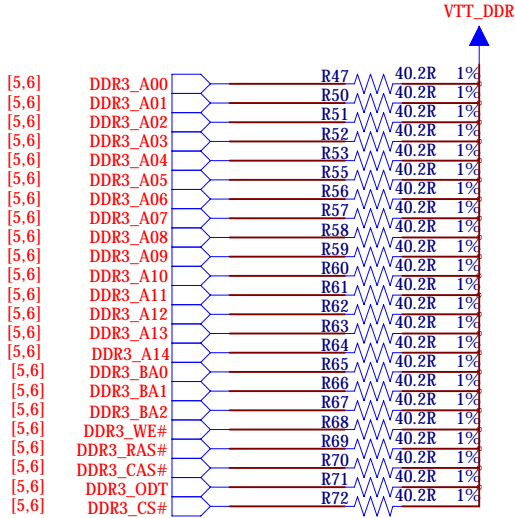
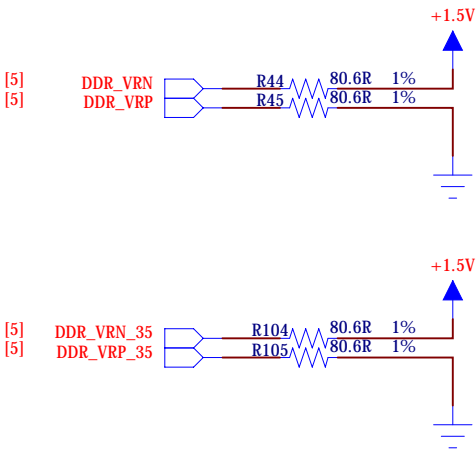
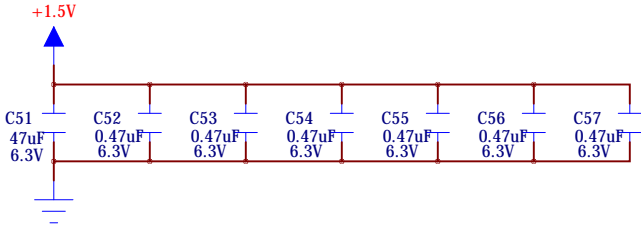
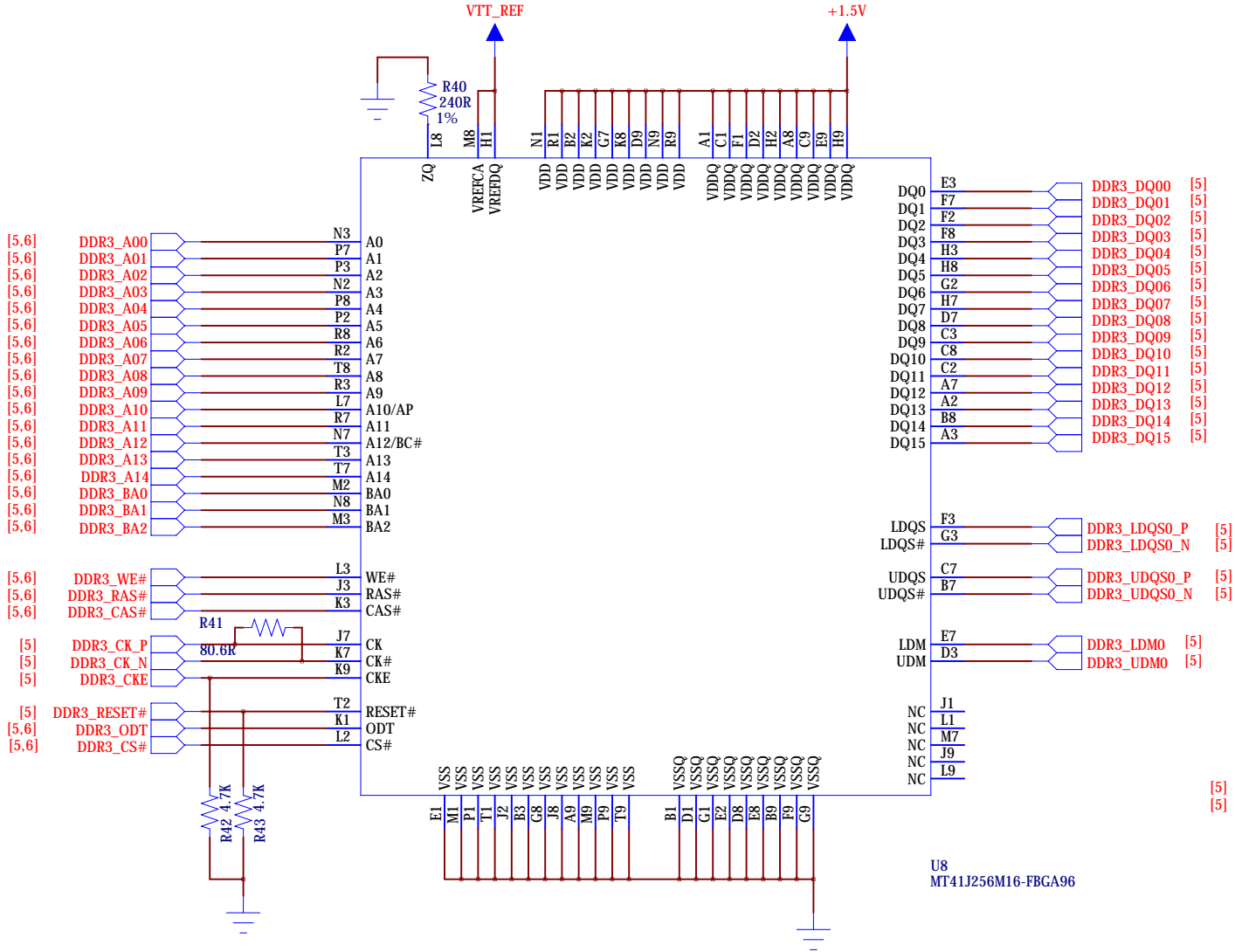
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



TITLE: BANK_34_35_216					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:5 OF 14
RELEASED:		E- ELEMENTS			

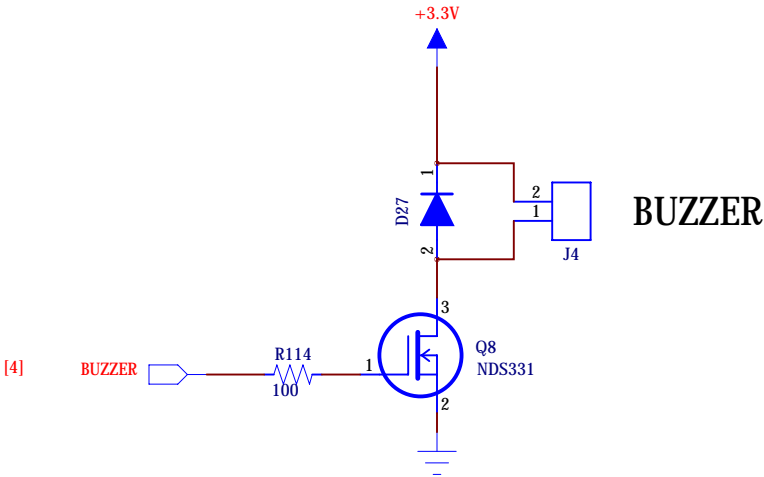
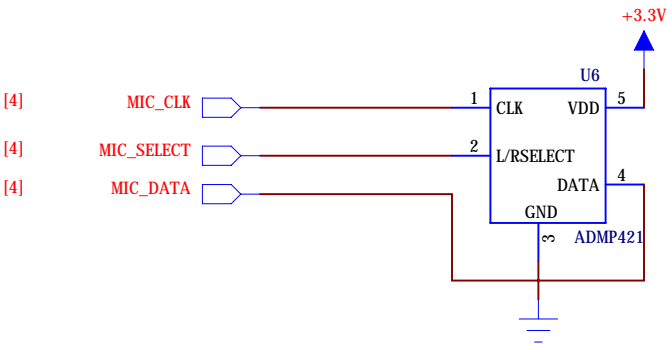
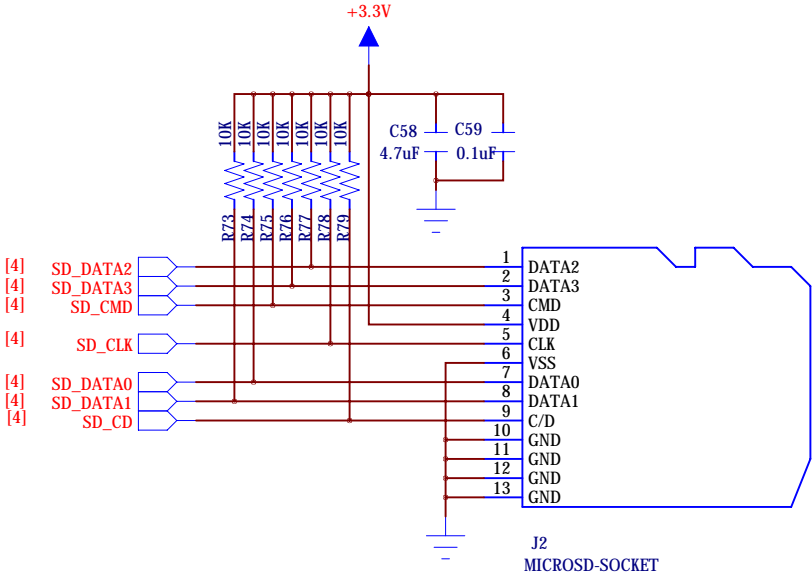
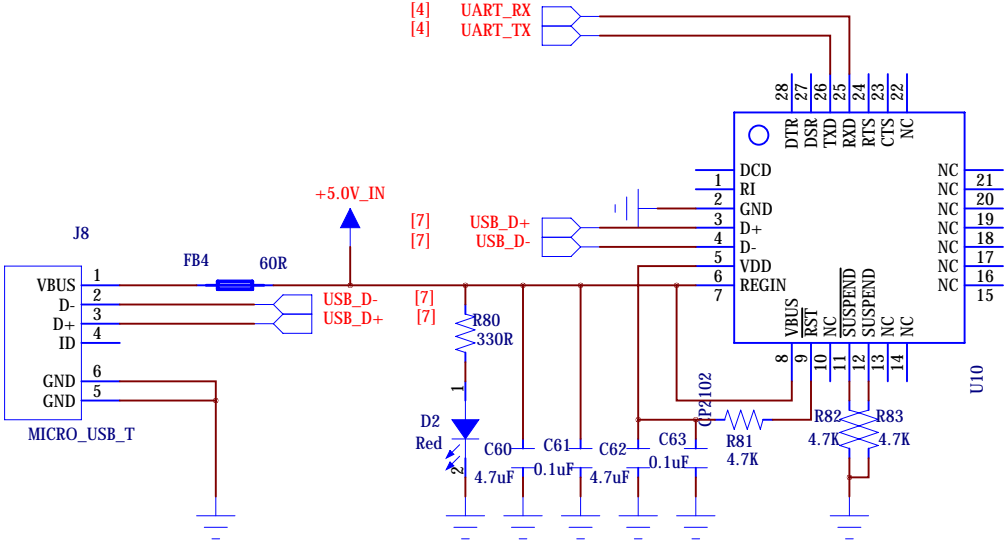


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



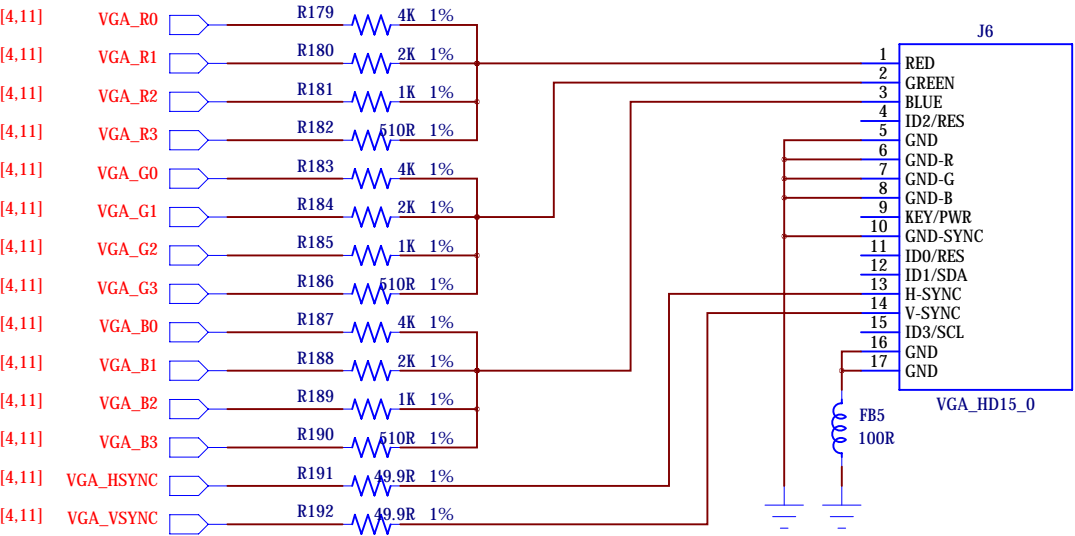
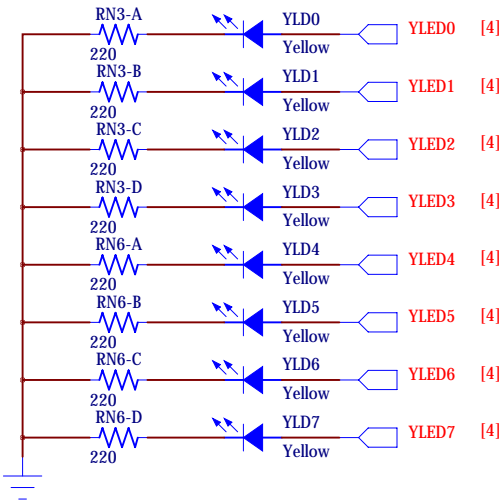
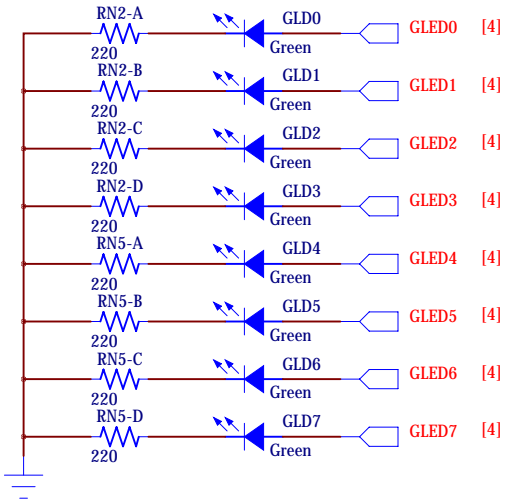
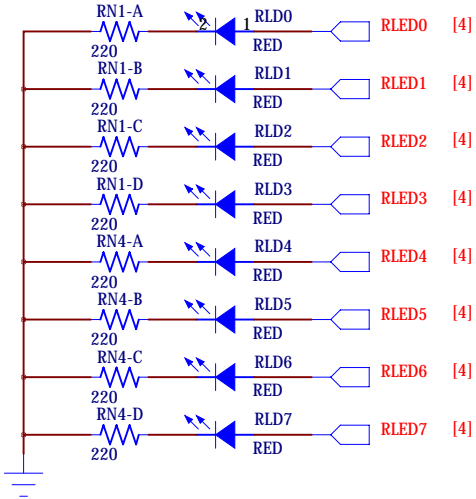
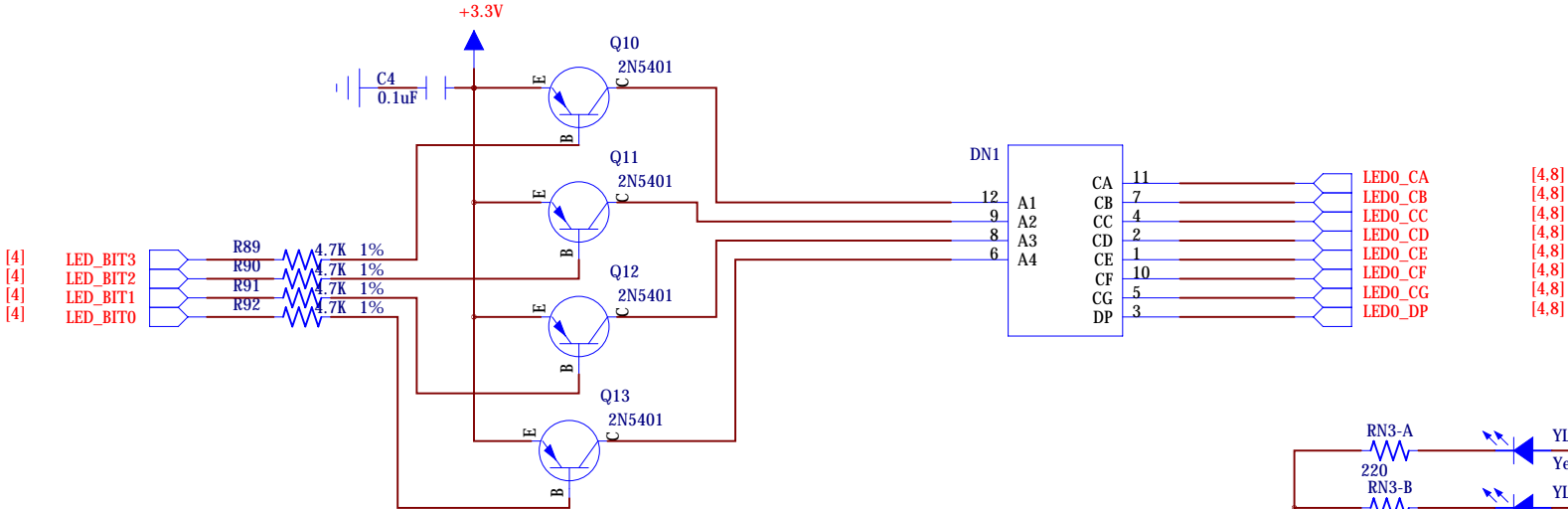
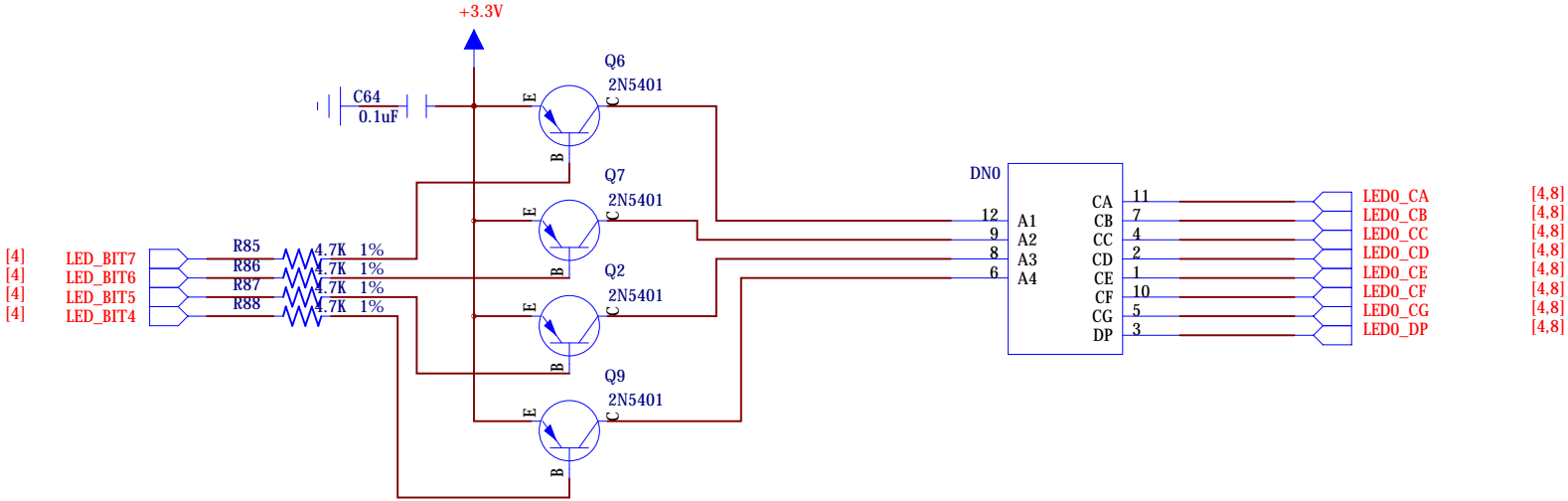
TITLE: DDR					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:6 OF 14
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LTR	ECO NO:	APPROVED:	DATE:



TITLE: URAT_SD					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:7 OF 14
RELEASED:		E- ELEMENTS			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

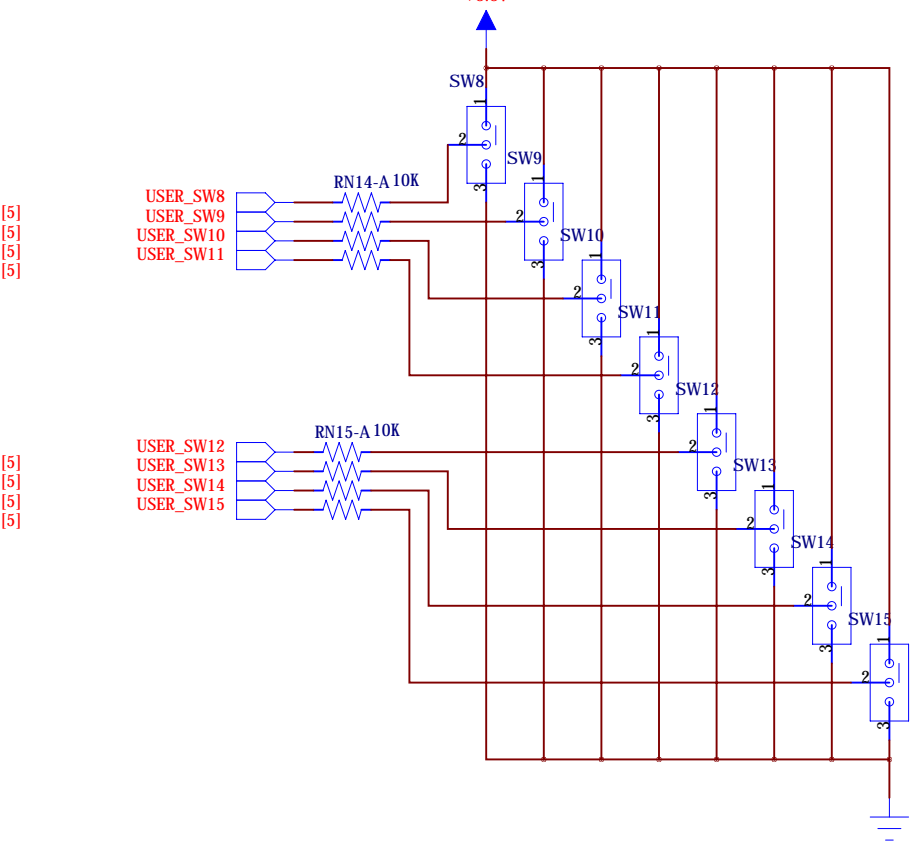
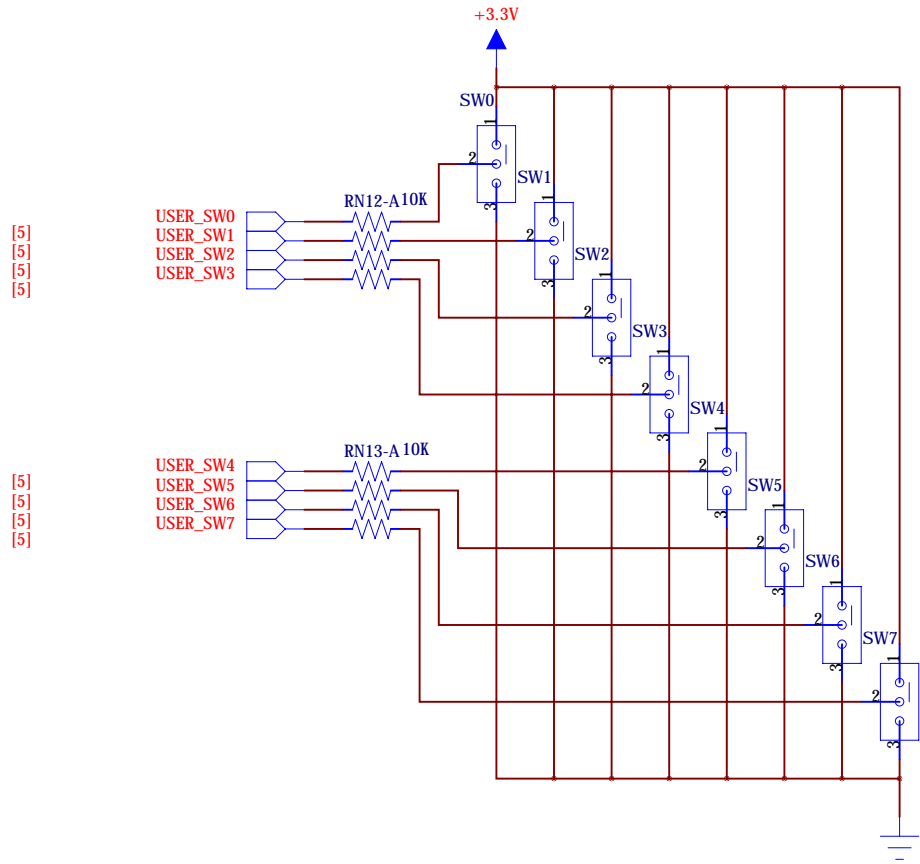


TITLE: <div>DISPLAY</div>					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: <div>A3</div>	SCALE:	SHEET:8 OF 14
RELEASED:		E- ELEMENTS			

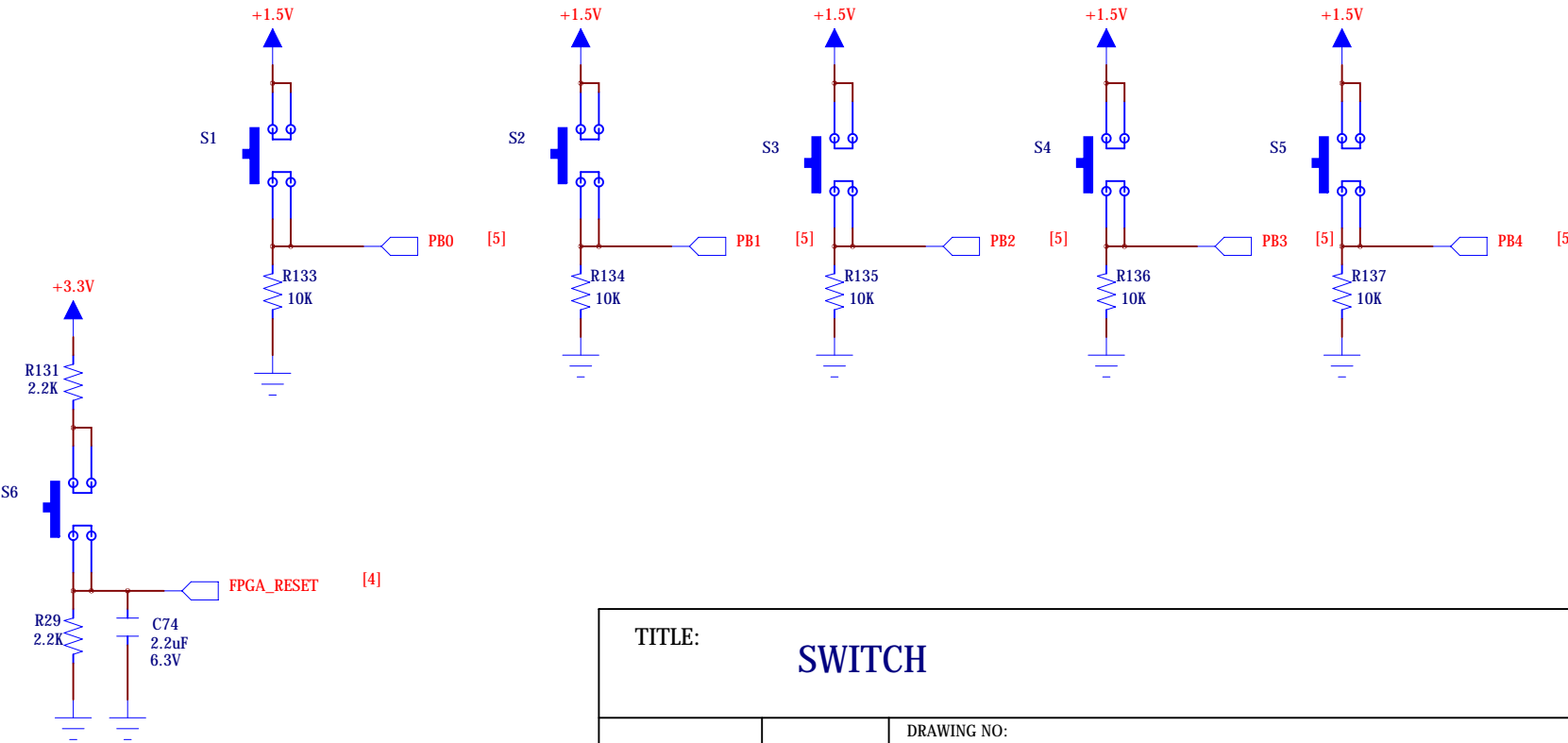
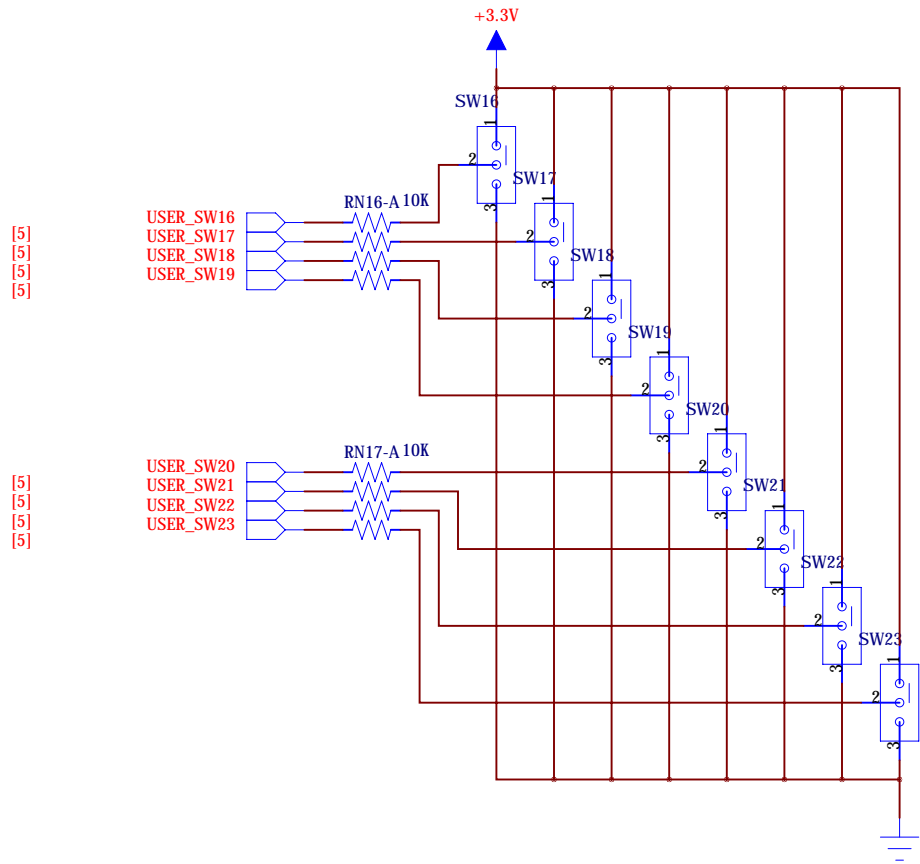
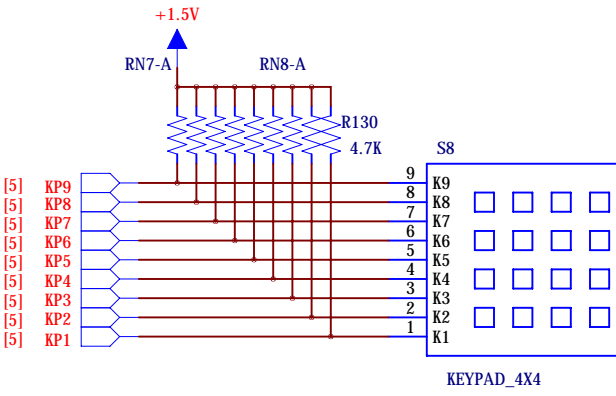




REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

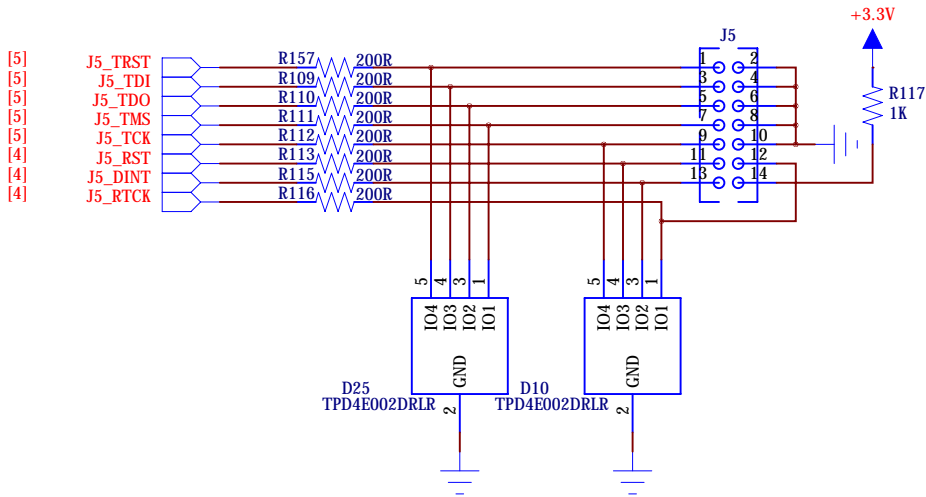
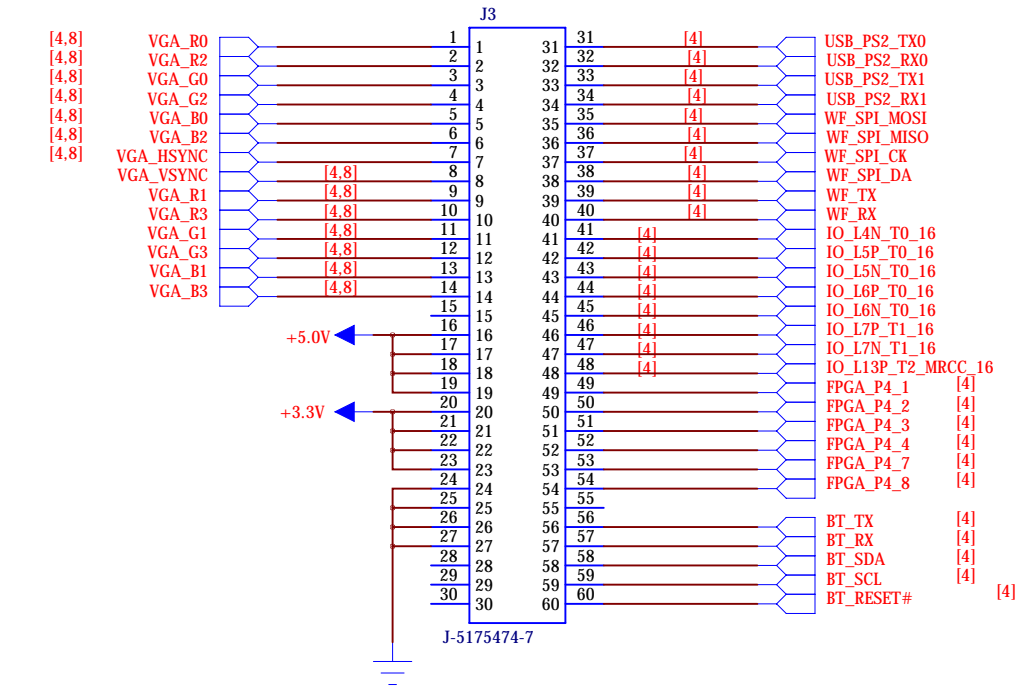


4\*4 keypad



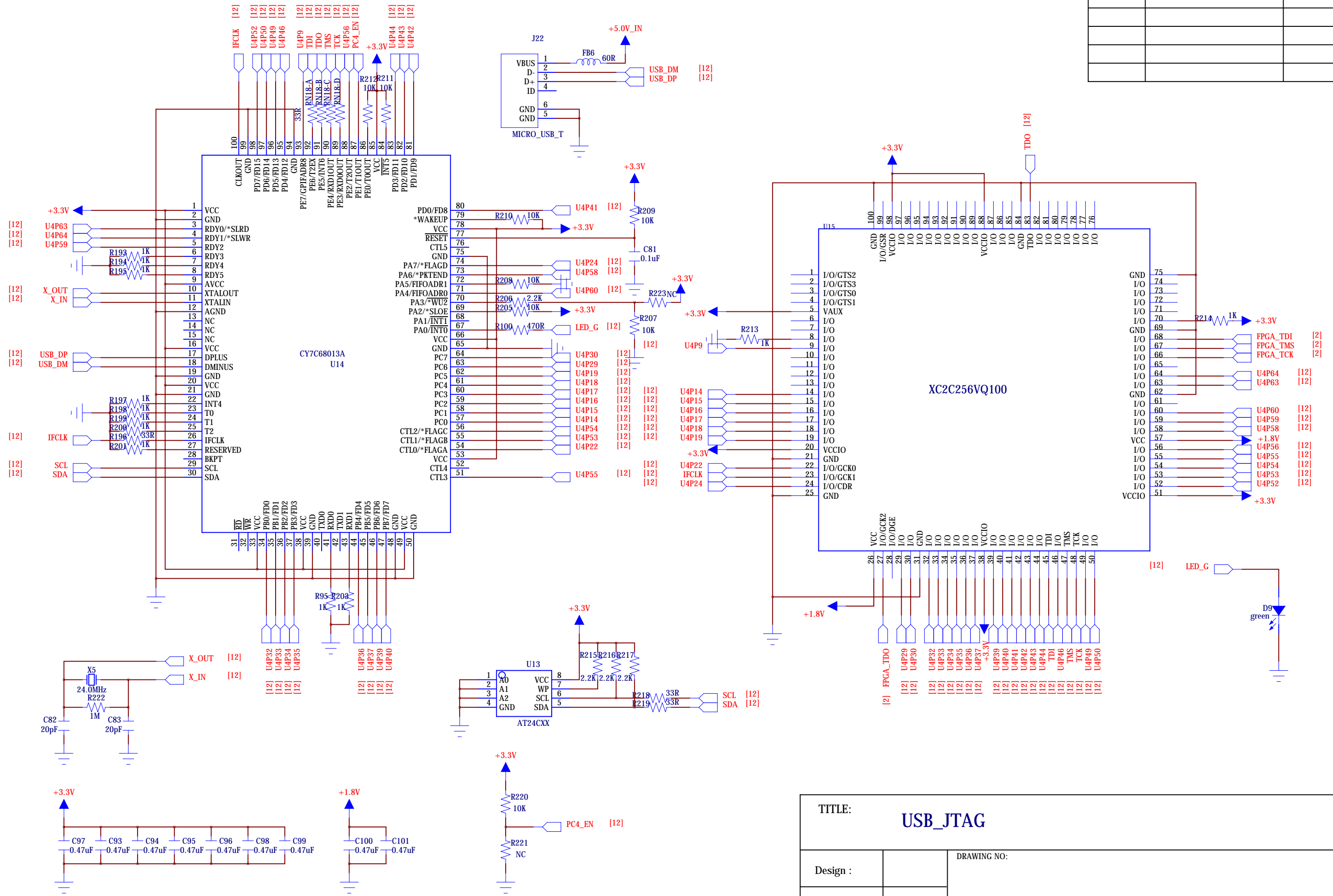
TITLE: SWITCH					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:10 OF 14
RELEASED:		E- ELEMENTS			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



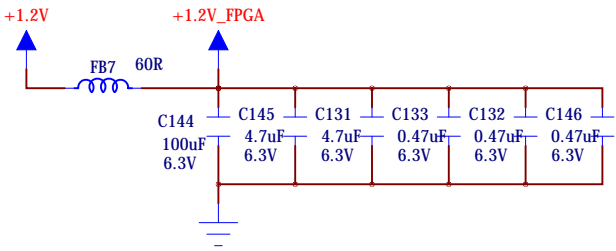
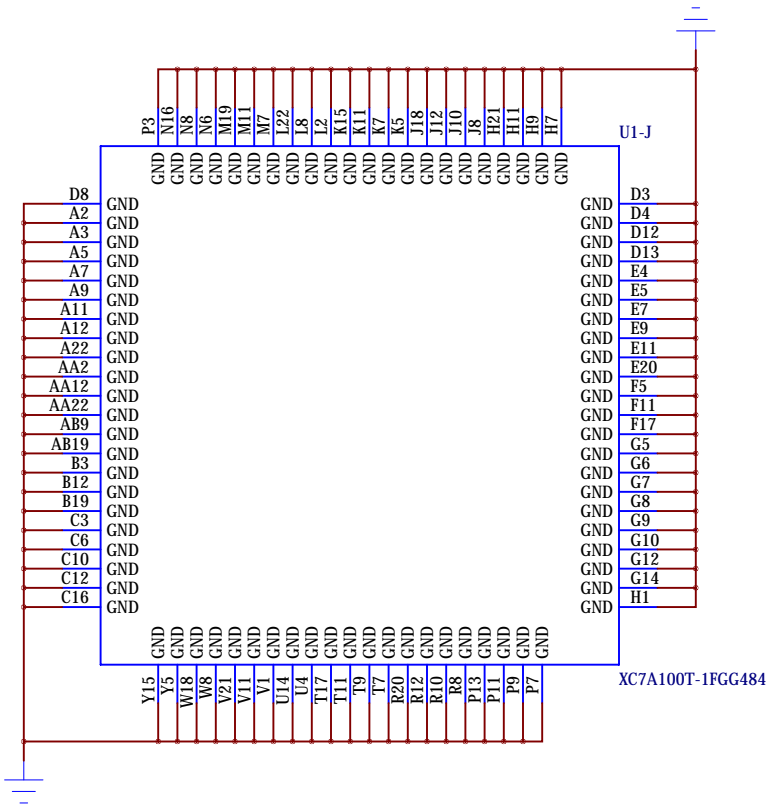
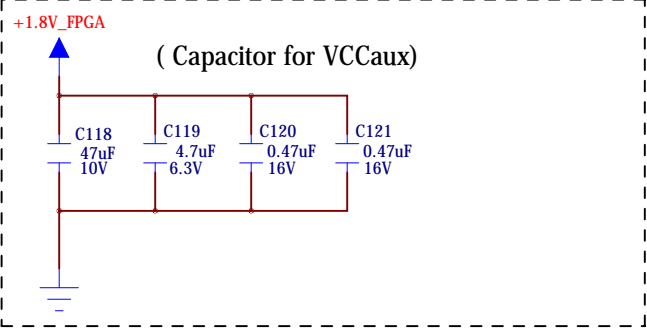
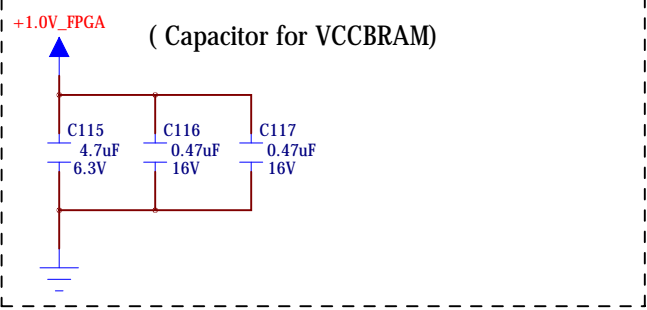
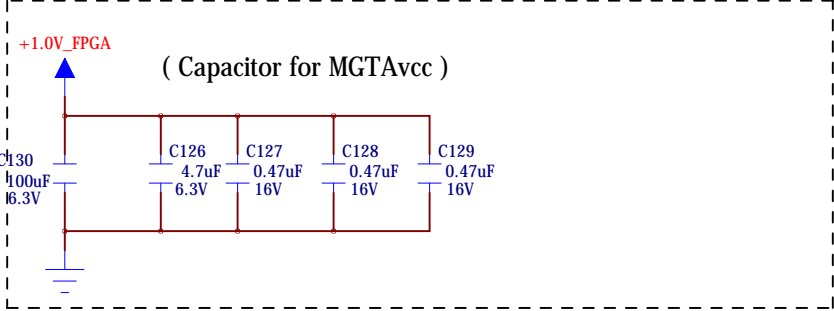
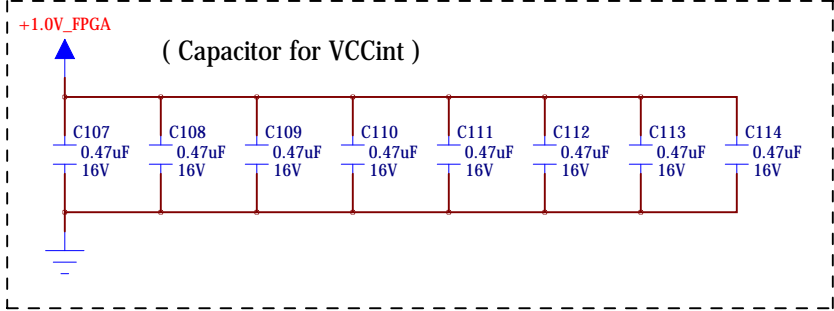
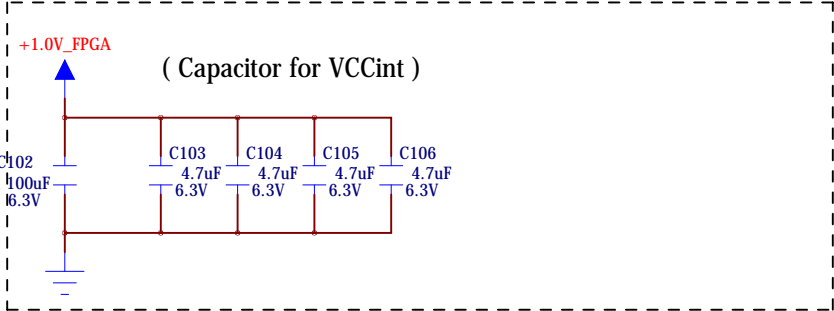
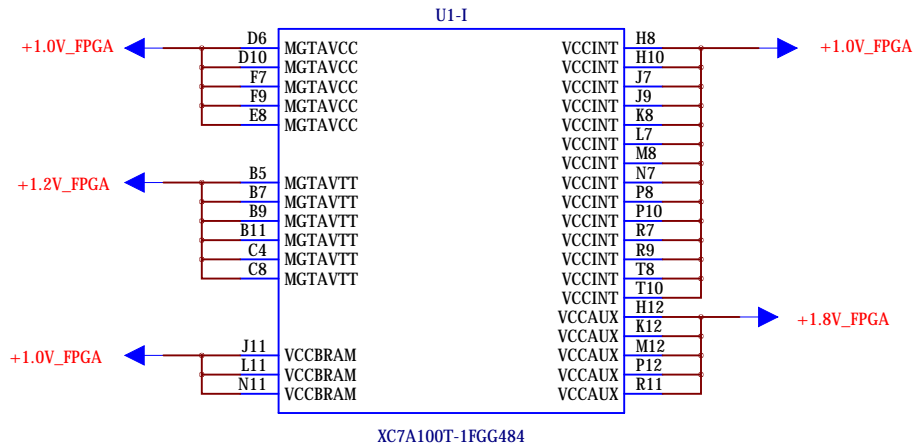
TITLE: CON_M					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET:11 OF 14
RELEASED:		E- ELEMENTS			

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TITLE: USB_JTAG					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: A3	SCALE:	SHEET: 12 OF 14
RELEASED:		E- ELEMENTS			

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TITLE: <b>FPGA_POWER</b>					
Design :		DRAWING NO:			
CHECKED:					
STANDARDIZED:		VERSION:	SIZE: <b>A3</b>	SCALE:	SHEET:13 OF 14
RELEASED:		<b>E-ELEMENTS</b>			

