FIFO buffer operates as follows:

Write Operation:

- When writeEn is asserted (set to 1) and the FIFO is not full (full is 0), the data present on writeData is written into the memory array in one clock cycle at the location indicated by wrPtr.
- The write pointer (wrPtr) is then incremented by one in the next clock cycle to point to the next write location.
- If the write pointer reaches the end of the memory array, it wraps around to the beginning, maintaining the circular nature of the FIFO.

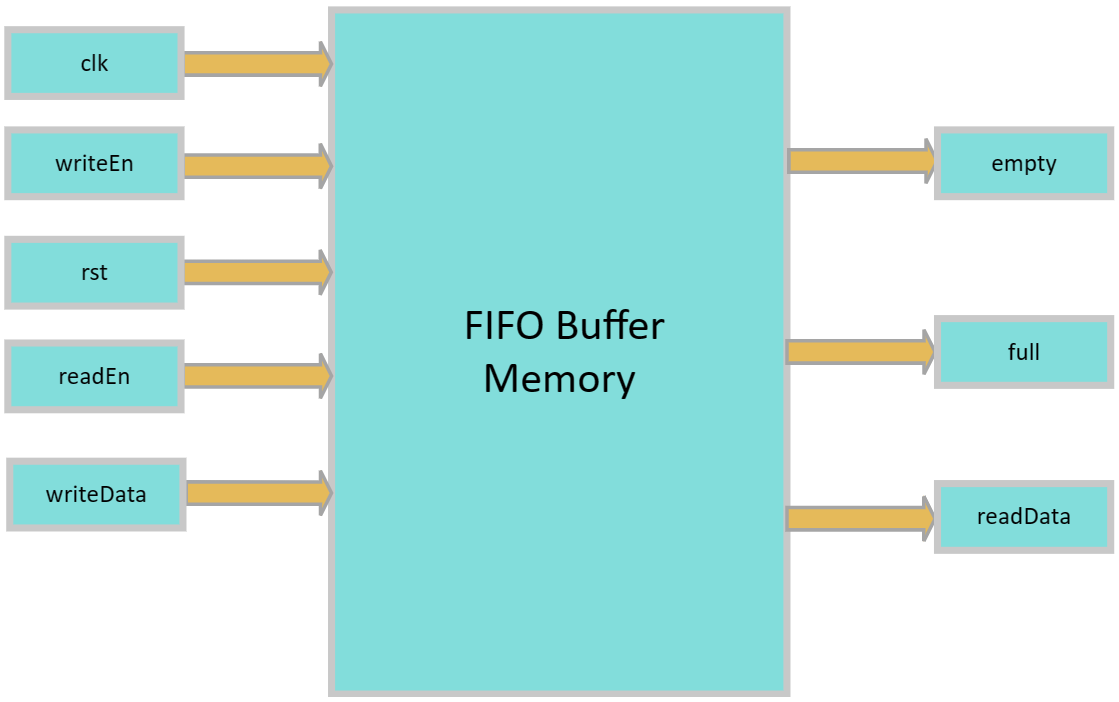
Read Operation:

- When readEn is asserted (set to 1) and the FIFO is not empty (empty is 0), the data at the location indicated by rdPtr is read out and presented on readData in a combinational way using continuous assignment.
- The read pointer (rdPtr) is then incremented by one in the next clock cycle to point to the next read location.
- Similar to the write pointer, if the read pointer reaches the end of the memory array, it wraps around to the beginning.

Full and Empty Flags:

- Empty Flag (empty): This is one when no write operation was performed and when the same amount of write and read operations was performed.
- Full Flag (full): If the difference between the write and read operations is equal to the size of the memory then the full flag is active.

Block Diagram:



Input Definitions

- clk: Clock signal.
- rst: Reset signal.
- writeEn: Write enable signal.
- writeData: Data input for writing.
- readEn: Read enable signal.

Output Definitions.

- readData: Data output for reading.
- full: Full flag indicating if the FIFO is full.
- empty: Empty flag indicating if the FIFO is empty.

Internal Components:

- Memory Array: Stores the data elements.
- Write Pointer: Points to the current write location.
- Read Pointer: Points to the current read location.
- Full Flag: Indicates when the FIFO is full.
- Empty Flag: Indicates when the FIFO is empty.