FIFO buffer operates as follows:

Initialization:

- The read and write pointers (rdcnt and wrcnt) are initialized to 0.
- The count is initialized to 0, indicating the buffer is empty initially.

Writing Data:

- When wr (write enable) is high and the buffer is not full (count < 8), data from datain is written into the FIFO at the current wrcnt position. The write pointer (wrcnt) is then incremented.

Reading Data:

- When rd (read enable) is high and the buffer is not empty (count > 0), data from the FIFO at the current rdcnt position is read into dataout. The read pointer (rdcnt) is then incremented.

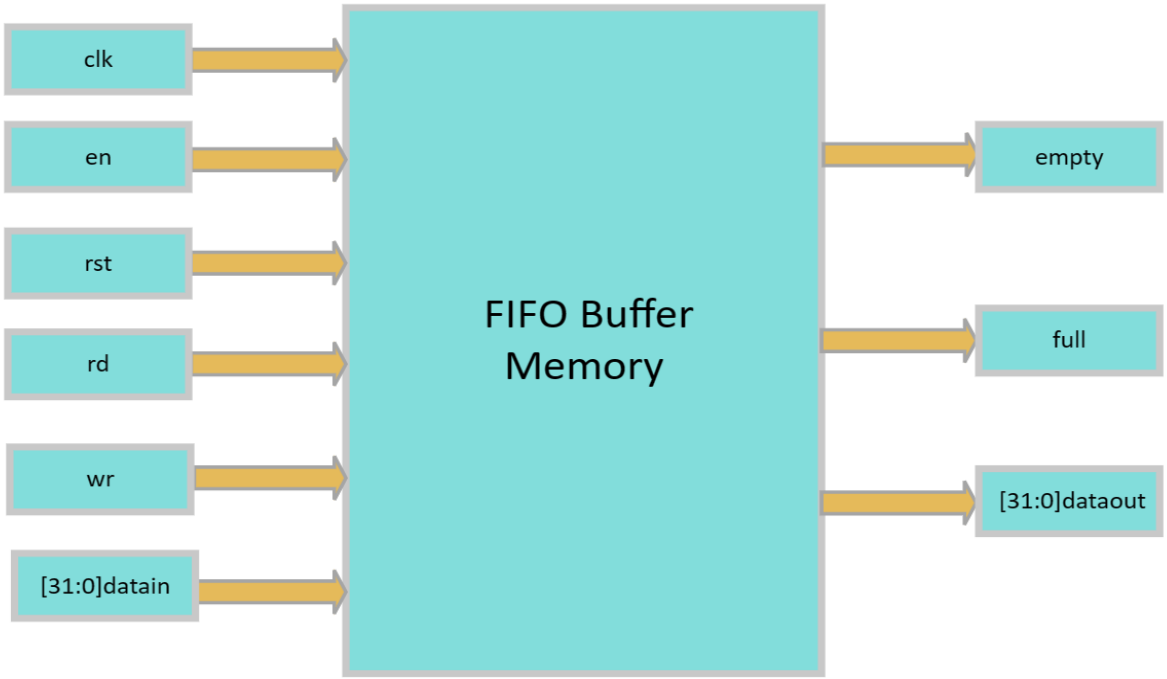
Pointer Wrapping:

- Both pointers (rdcnt and wrcnt) wrap around to 0 when they reach the end of the FIFO array (position 7).

Count Adjustment:

- The count is adjusted based on the positions of the read and write pointers to reflect the current number of elements in the FIFO.

Block Diagram:



Input and Output Definitions

- clk: Clock signal
- en: Enable signal
- rst: Reset signal
- rd: Read enable signal
- wr: Write enable signal
- datain: 32-bit data input
- dataout: 32-bit data output (registered output)
- empty: Indicates if the FIFO is empty
- full: Indicates if the FIFO is full

Internal Registers and Variables

- count: 3-bit counter to keep track of the number of elements in the FIFO
- fifo: Array to store 8 elements of 32-bit data (FIFO buffer)
- rdcnt: 3-bit read pointer
- wrcnt: 3-bit write pointer

Output Assignments

- empty is 1 if count is 0, indicating the FIFO is empty.
- full is 1 if count is 8, indicating the FIFO is full.