128K x 8 SRAM
WITH DUAL CHIP ENABLE

AVAILABLE AS MILITARY SPECIFICATIONS
- SMD 5962-89598
- MIL-STD-883

FEATURES
- High Speed: 12, 15, 20, 25, 35, 45, 55 and 70 ns
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power CMOS process
- Single +5V (+10%) Power Supply
- Easy memory expansion with CE1\, CE2, and OE\ options.
- All inputs and outputs are TTL compatible

OPTIONS

MARKING

- **Timing**

12ns access	-12 (contact factory)
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

- **Package(s)•**

Ceramic DIP (400 mil)	C	No. 111
Ceramic DIP (600 mil)	CW	No. 112
Ceramic LCC	EC	No. 207
Ceramic LCC	ECA	No. 208
Ceramic Flatpack	F	No. 303
Ceramic SOJ	DCJ	No. 501
Ceramic SOJ	SOJ	No. 507

- 2V data retention/low power   L

*Electrical characteristics identical to those provided for the 45ns access devices.

For more products and information please visit our web site at
www.austinsemiconductor.com

PIN ASSIGNMENT
(Top View)
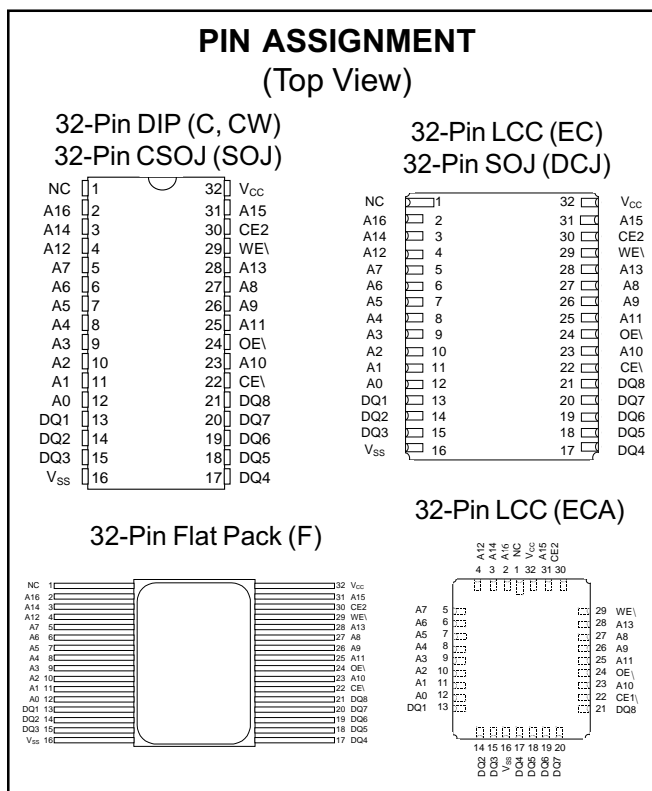
GENERAL DESCRIPTION

The MT5C1008 SRAM employs high-speed, low power CMOS designs using a four-transistor memory cell, and are fabricated using double-layer metal, double-layer polysilicon technology.
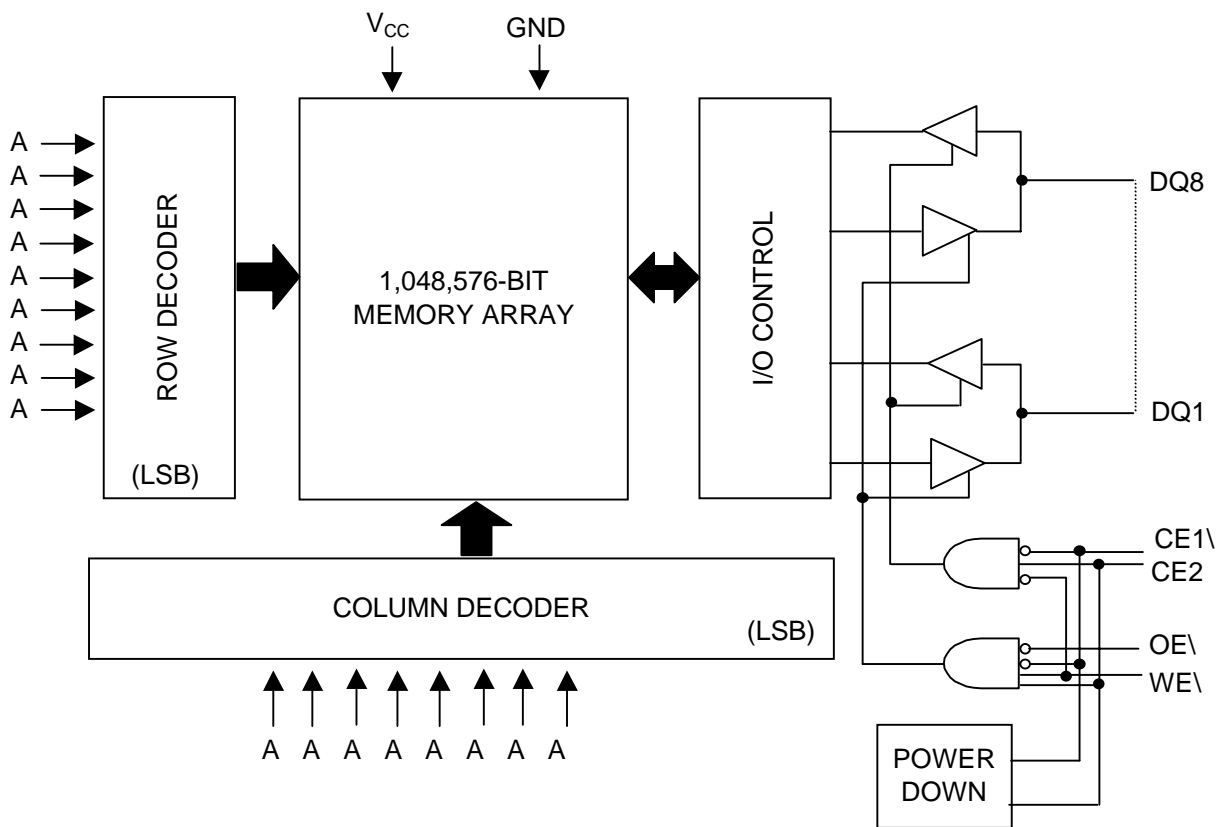
For design flexibility in high-speed memory applications, this device offers dual chip enables (CE1\, CE2) and output enable (OE\). These control pins can place the outputs in High-Z for additional flexibility in system design. All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

Writing to these devices is accomplished when write enable (WE\) and CE1\ inputs are both LOW and CE2 is HIGH. Reading is accomplished when WE\ and CE2 remain HIGH and CE1\ and OE\ go LOW. The devices offer a reduced power standby mode when disabled, allowing system designs to achieve low standby power requirements.

The "L" version offers a 2V data retention mode, reducing current consumption to 1mA maximum.

FUNCTIONAL BLOCK DIAGRAM

V$_{CC}$ GND

ROW DECODER

A
A
A
A
A
A
A
A
A

(LSB)

1,048,576-BIT
MEMORY ARRAY

I/O CONTROL

DQ8

DQ1

COLUMN DECODER

(LSB)

A A A A A A A A

CE1\
CE2

OE\
WE\

POWER
DOWN

NOTE: The two least significant row address bits (A8 and A6) are encoded using gray code.

TRUTH TABLE

MODE	OE\	CE1\	CE2	WE\	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range (Vcc)................................-.5V to +6.0V
Storage Temperature ....-65°C to +150°C
Short Circuit Output Current (per I/O)…........................20mA
Voltage on any Pin Relative to Vss................-.5V to Vcc+1 V
Max Junction Temperature**.......................................+150°C
Power Dissipation ....1 W

*Stresses at or greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods will affect reliability. Refer to page 17 of this datasheet for a technical note on this subject.
** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C $\leq T_C \leq$ 125°C & -45°C to +85°C; V_{CC} = 5.0V $\pm$10%)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	IL_I	-10	10	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq V_{CC}$	IL_O	-10	10	µA	
Output High Voltage	I_{OH}=-4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL}=8.0mA	V_{OL}		0.4	V	1

PARAMETER	CONDITIONS	SYM	MAX						UNITS	NOTES
			-12	-15	-20	-25	-35	-45		
Power Supply Current: Operating	$CE\backslash \leq V_{IL}$; $OE\backslash$, $WE\backslash$, and $CE2 \geq V_{IH}$ V_{CC} = MAX, f = MAX = 1/t_{RC} (MIN) Output Open *L version only	I_{CCSP}	250	180	150	140	135	125	mA	3
		I_{CCLP} *	250	180	140	130	125	115	mA	
Power Supply Current: Standby	$CE\backslash=V_{IH}$, $CE2=V_{IL}$; Other Inputs at $\leq V_{IL}$, $\geq V_{IH}$, V_{CC} = MAX f = 0 Hz	I_{SBT}	25	25	25	25	25	25	mA	
	$CE\backslash \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \leq V_{SS}$ -0.2V $V_{IH} \geq V_{CC}$ -0.2V; F = 0 Hz	I_{SBC}	10	10	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance (A0-A16)	T_A = 25°C, f = 1MHz V_{CC} = 5V	C_I	12	pF	4
Output Capacitance		C_O	14	pF	4
Input Capacitance (CE\, WE\, OE\)		C_I	20	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C $\leq$ T$_C$ $\leq$ 125°C & -40°C to +85°C; V$_{CC}$ = 5.0V $\pm$10%)

DESCRIPTION	SYMBOL	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	-45 MIN	-45 MAX	UNITS	NOTES
READ CYCLE															
READ cycle time	t$_{RC}$	12		15		20		25		35		45		ns	
Address access time	t$_{AA}$		12		15		20		25		35		45	ns	
Chip Enable access time	t$_{ACE}$		12		15		20		25		35		45	ns	
Output hold from address change	t$_{OH}$	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t$_{LZCE}$	3		3		3		3		3		3		ns	4, 6, 7
Chip disable to output in High-Z	t$_{HZCE}$		7		7		8		10		15		20	ns	4, 6, 7
Output Enable access time	t$_{AOE}$		7		7		7		10		15		20	ns	4, 6, 7
Output Enable to output in Low-Z	t$_{LZOE}$	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t$_{HZOE}$		7		7		8		10		15		20	ns	4, 6, 7
WRITE CYCLE															
WRITE cycle time	t$_{WC}$	12		15		20		25		35		45		ns	
Chip Enable to end of write	t$_{CW}$	11		12		15		20		25		35		ns	
Address valid to end of write	t$_{AW}$	11		12		15		20		25		35		ns	
Address setup time	t$_{AS}$	0		0		0		0		0		0		ns	
Address hold from end of write	t$_{AH}$	0		0		0		0		0		5		ns	
WRITE pulse width	t$_{WP}$	11		12		15		20		25		35		ns	
Data setup time	t$_{DS}$	8		8		10		15		20		20		ns	
Data hold time	t$_{DH}$	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t$_{LZWE}$	5		5		5		5		5		5		ns	4, 6, 7
Write Enable to output in High-Z	t$_{HZWE}$		7		7		9		10		15		20	ns	4, 6, 7

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AC TEST CONDITIONS

Input pulse levels .... Vss to 3.0V
Input rise and fall times 5ns
Input timing reference levels 1.5V
Output reference levels 1.5V
Output load .... See Figures 1 and 2
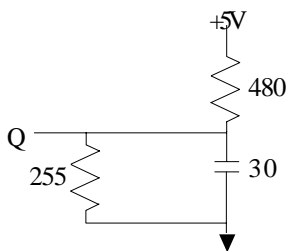
Fig. 1 Output Load
Equivalent
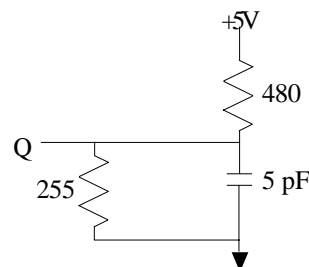
Fig. 2 Output Load
Equivalent

NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \dfrac{1}{t_{RC}\,(MIN)}$ Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{LZCE}, t_{LZWE}, t_{LZOE}, t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.

7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} and t_{HZOE} is less than t_{LZOE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. CE2 timing is the same as CE1\ timing. The waveform is inverted.
13. Chip enable (CE1\, CE2) and write enable (WE\) can initiate and terminate a WRITE cycle.

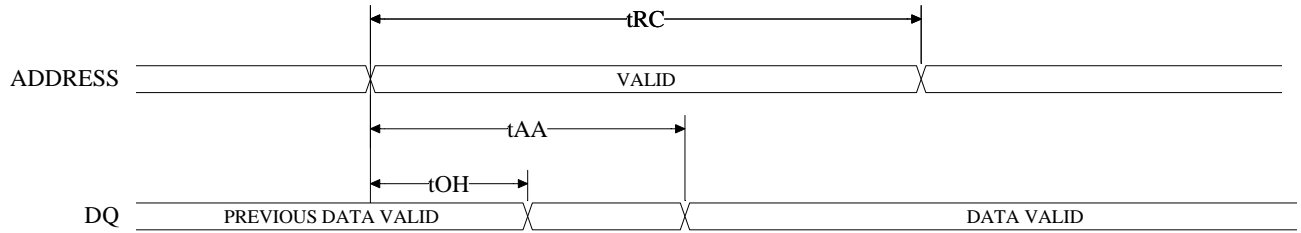## DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2	---	V	
Data Retention Current	CE\ ≥ (V_{CC} - 0.2V) V_{IN} ≥ (V_{CC} - 0.2V) or ≤ 0.2V, f=0	V_{CC} = 2V	I_{CCDR}		1.0	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	---	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM

DON'T CARE

UNDEFINED
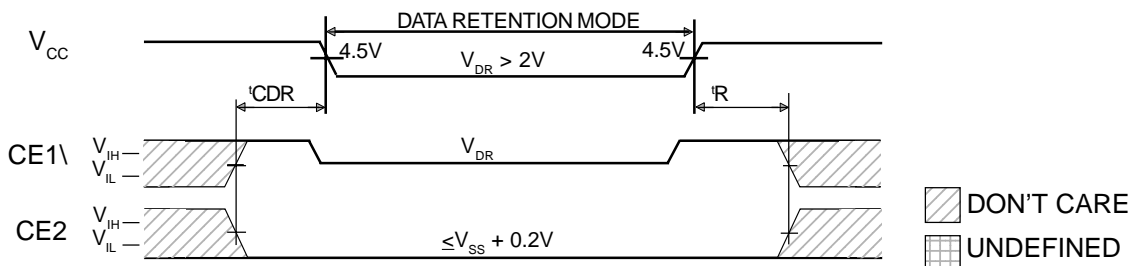
READ CYCLE NO. 1 [8, 9]

READ CYCLE NO. 2 [7, 8, 10, 12]
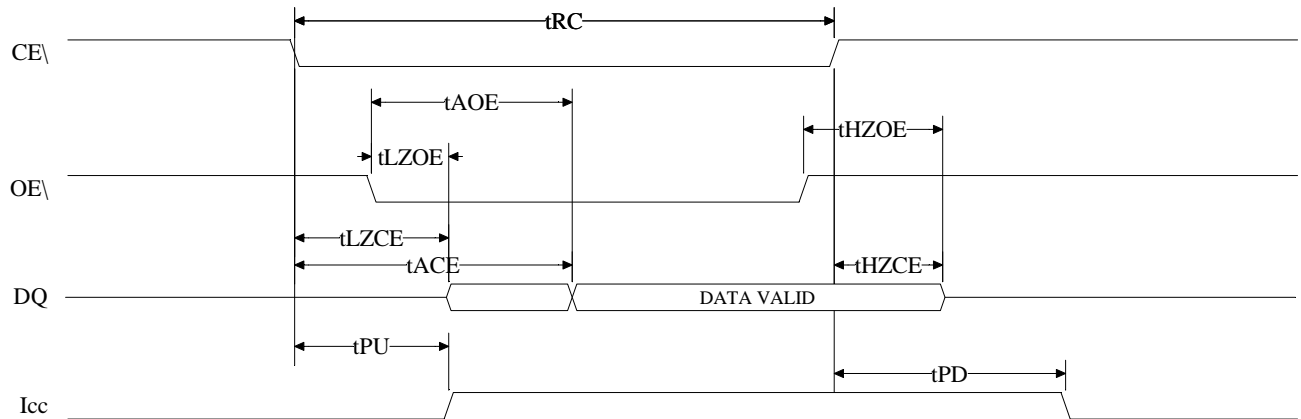
WRITE CYCLE NO. 1 [12, 13]
(Chip Enabled Controlled)
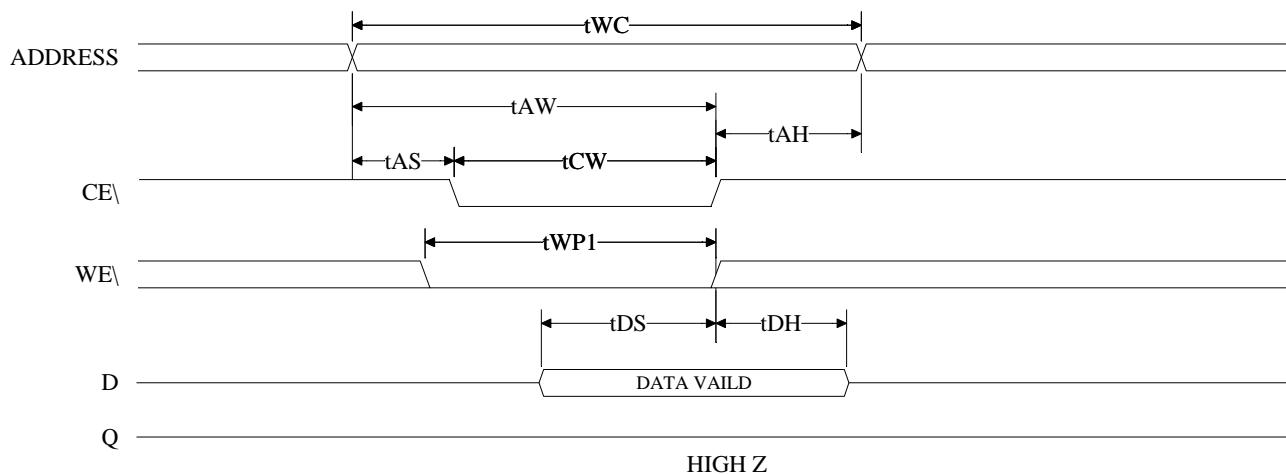
WRITE CYCLE NO. 2 [7, 12, 13]
(Write Enabled Controlled)
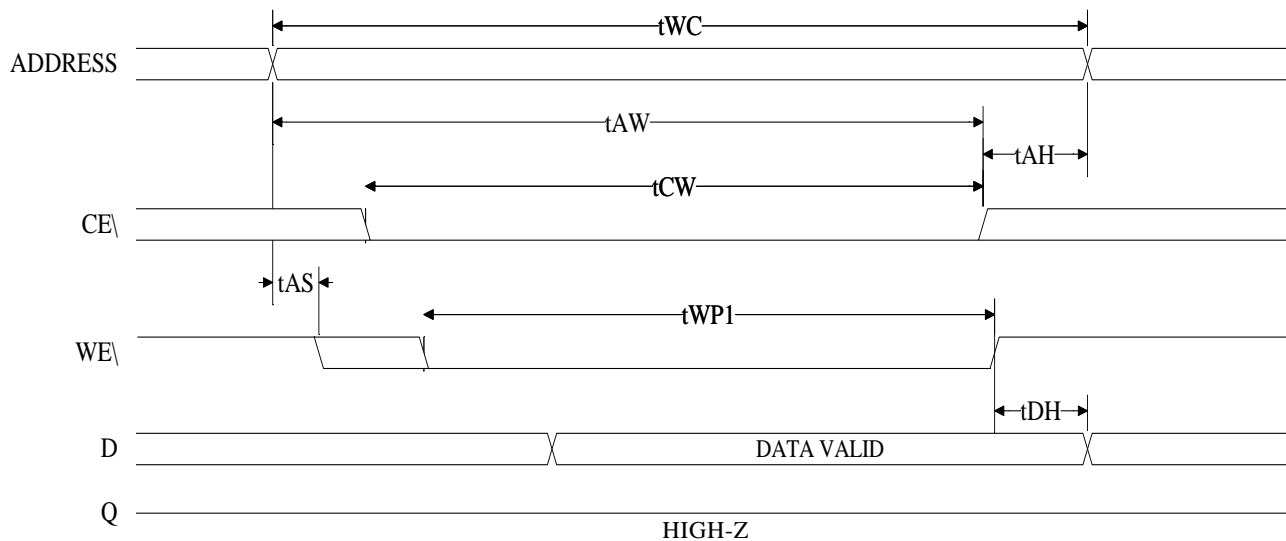
NOTE: Output enable (OE\) is inactive (HIGH).

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MECHANICAL DEFINITIONS*

ASI Case #111 (Package Designator C)
SMD 5962-89598, Case Outline Z
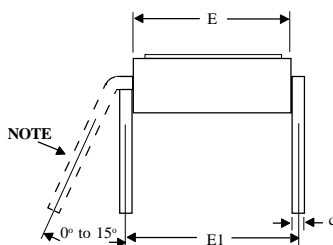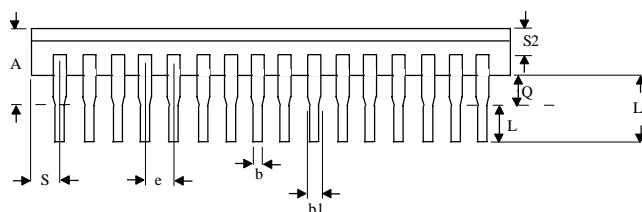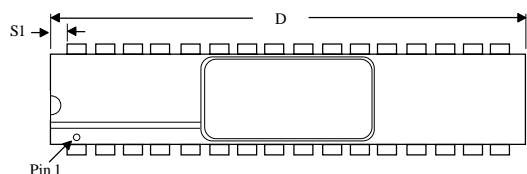
	SMD SPECIFICATIONS	
SYMBOL	**MIN**	**MAX**
A	---	0.232
b	0.014	0.023
b1	0.038	0.065
c	0.008	0.015
D	---	1.700
E	0.350	0.405
E1	0.390	0.420
e	0.100 BSC	
L	0.125	0.200
L1	0.150	---
Q	0.015	0.060
S	---	0.100
S1	0.005	---
S2	0.005	---
NOTE:	Either configuration in detail A is allowed on SMD.	

All measurements are in inches.

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MECHANICAL DEFINITIONS*

ASI Case #112 (Package Designator CW)
SMD 5962-89598, Case Outline X

SYMBOL	SMD SPECIFICATIONS	
	MIN	**MAX**
A	0.089	0.111
b	0.016	0.020
b1	0.045	0.055
b2	0.009	0.011
D	1.585	1.615
E	0.585	0.605
E1	0.595	0.610
e	0.090	0.110
L	0.040	0.060
L1	0.125	0.175

All measurements are in inches.

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MECHANICAL DEFINITIONS*

**ASI Case #207 (Package Designator EC)
SMD 5962-89598, Case Outline U**

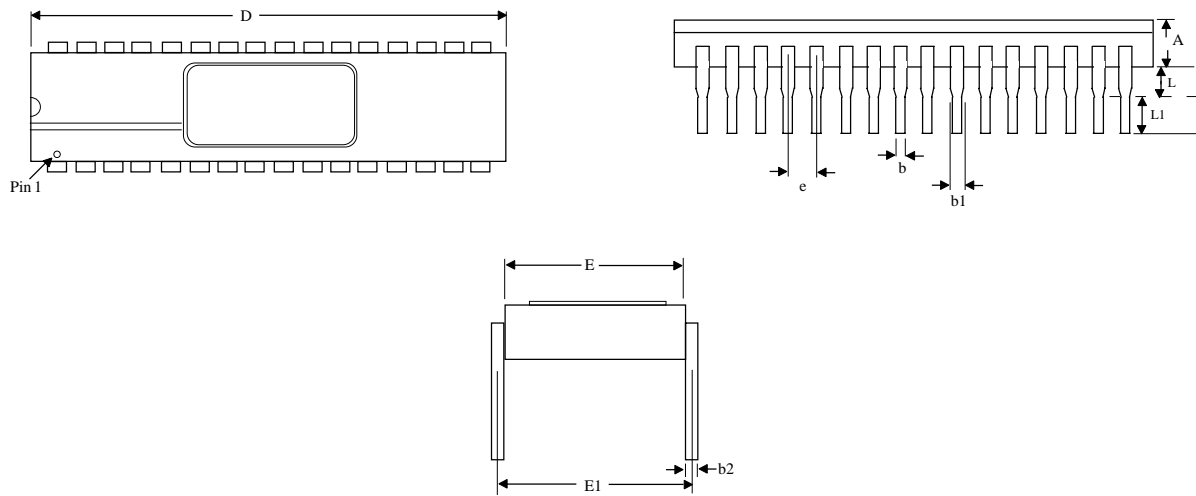| SYMBOL	SMD SPECIFICATIONS	
	MIN	**MAX**
A	0.080	0.100
b	0.022	0.028
b1	0.006	0.022
b2	0.040	---
D	0.800	0.840
E	0.392	0.408
e	0.050 BSC	
h	0.012 REF	
L	0.070	0.080
L1	0.090	0.110
L2	0.003	0.015

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #208 (Package Designator ECA)
SMD 5962-89598, Case Outline M

Detail A
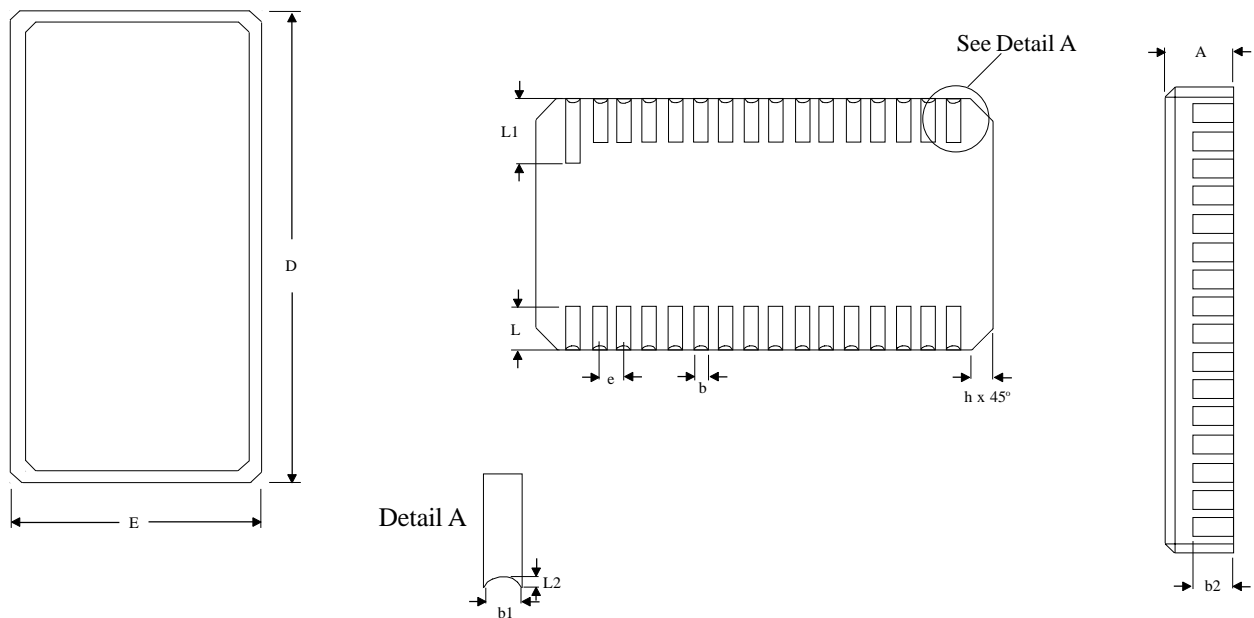
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
b	0.022	0.028
b1	0.004	0.014
b2	0.040	---
D	0.442	0.458
D1	0.300 BSC	
E	0.540	0.560
E1	0.400 BSC	
e	0.050 BSC	
L	0.045	0.055
L1	0.075	0.095

All measurements are in inches.

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MECHANICAL DEFINITIONS*

ASI Case #303 (Package Designator F)
SMD 5962-89598, Case Outline T

Top View

Bottom View

SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.097	0.125
b	0.015	0.019
c	0.003	0.009
D	---	0.830
E	0.400	0.420
E1	---	0.450
E2	0.180	---
E3	0.030	---
e	0.050 BSC	
L	0.250	0.370
Q	0.026	0.045
S	---	0.045
S1	0.000	---

All measurements are in inches.

MECHANICAL DEFINITIONS*

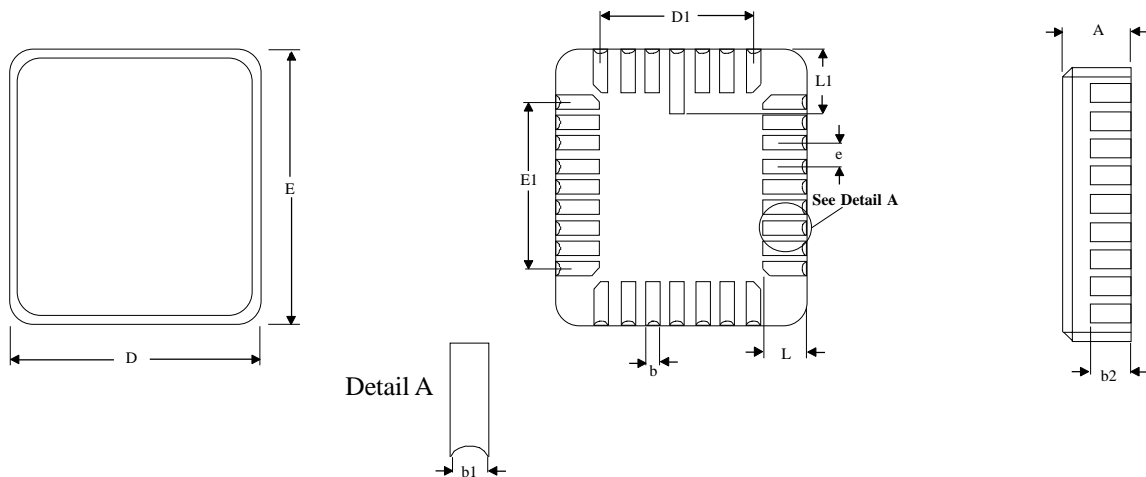**ASI Case #501 (Package Designator DCJ)**
SMD 5962-89598, Case Outline 7

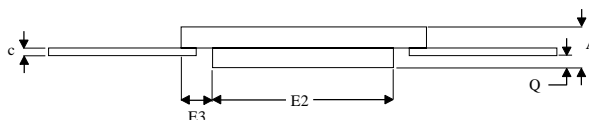| SYMBOL	SMD SPECIFICATIONS	
	MIN	**MAX**
A	0.132	0.144
A2	0.026	0.036
B1	0.030	0.040
b	0.015	0.019
D	0.812	0.828
D1	0.740	0.760
E	0.405	0.415
E1	0.435	0.445
E2	0.360	0.380
e	0.050 BSC	

All measurements are in inches.

MECHANICAL DEFINITIONS*

**ASI Case #507 (Package Designator SOJ)
SMD 5962-89598, Case Outline Y**

Detail A
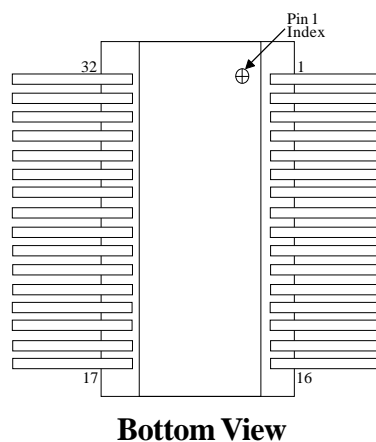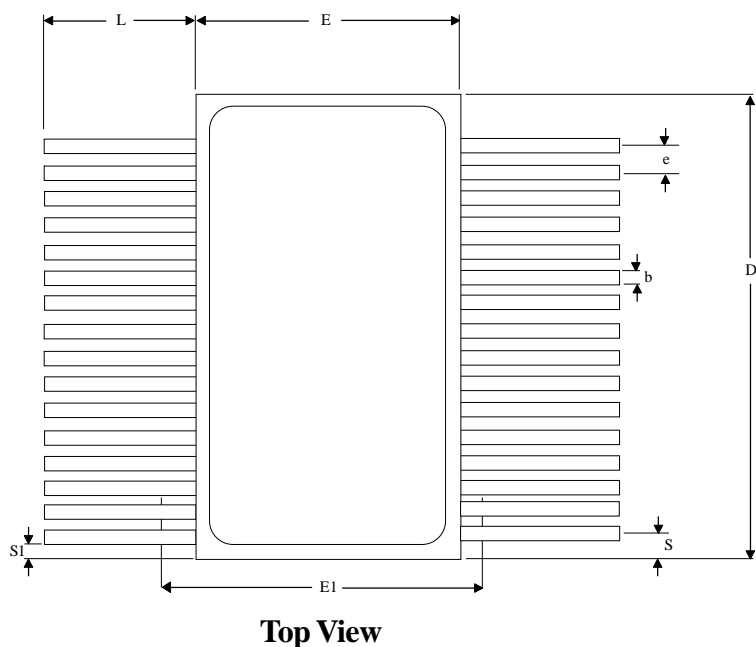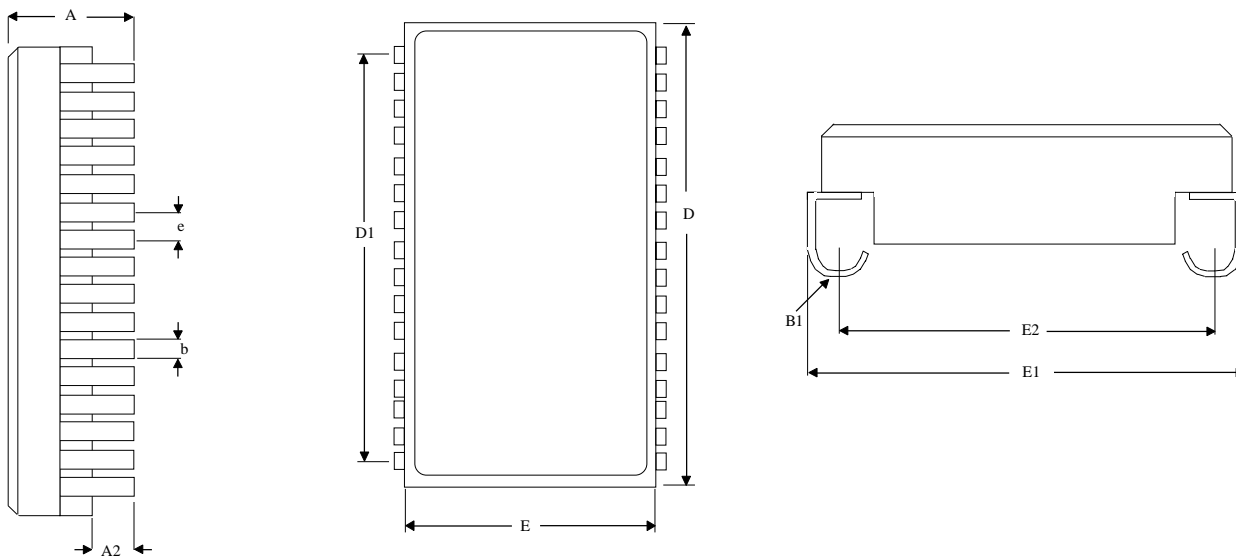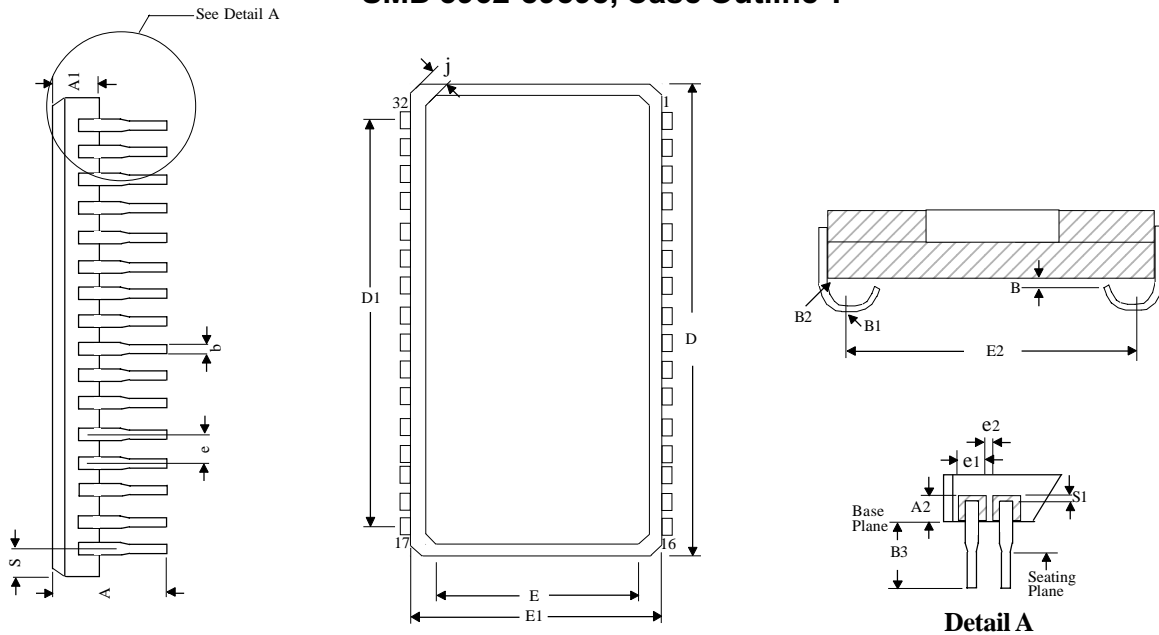
	SMD SPECIFICATIONS	
SYMBOL	MIN	MAX
A	0.120	0.165
A1	0.088	0.120
A2	0.070 REF	
B	0.010 REF	
B1	0.030R TYP	
B2	0.020 REF	
B3	0.025	0.045
b	0.015	0.019
D	0.816	0.838
D1	0.750 REF	
E	0.419	0.431
E1	0.430	0.445
E2	0.360	0.380
e	0.050 BSC	
e1	0.038 TYP	
e2	0.005	---
j	0.005 TYP	
S	0.030	0.040
S1	0.020 TYP	

All measurements are in inches.

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ORDERING INFORMATION

EXAMPLE: MT5C1008CW-45/883C

Device Number	Package Type	Speed ns	Options**	Process
MT5C1008	C	-12	L	/*
MT5C1008	CW	-12	L	/*
MT5C1008	C	-15	L	/*
MT5C1008	CW	-15	L	/*
MT5C1008	C	-20	L	/*
MT5C1008	CW	-20	L	/*
MT5C1008	C	-25	L	/*
MT5C1008	CW	-25	L	/*
MT5C1008	C	-35	L	/*
MT5C1008	CW	-35	L	/*
MT5C1008	C	-45	L	/*
MT5C1008	CW	-45	L	/*
MT5C1008	C	-55	L	/*
MT5C1008	CW	-55	L	/*
MT5C1008	C	-70	L	/*
MT5C1008	CW	-70	L	/*

EXAMPLE: MT5C1008ECA-25L/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1008	EC	-12	L	/*
MT5C1008	ECA	-12	L	/*
MT5C1008	EC	-15	L	/*
MT5C1008	ECA	-15	L	/*
MT5C1008	EC	-20	L	/*
MT5C1008	ECA	-20	L	/*
MT5C1008	EC	-25	L	/*
MT5C1008	ECA	-25	L	/*
MT5C1008	EC	-35	L	/*
MT5C1008	ECA	-35	L	/*
MT5C1008	EC	-45	L	/*
MT5C1008	ECA	-45	L	/*
MT5C1008	EC	-55	L	/*
MT5C1008	ECA	-55	L	/*
MT5C1008	EC	-70	L	/*
MT5C1008	ECA	-70	L	/*

EXAMPLE: MT5C1008F-25L/883C

Device Number	Package Type	Speed ns	Options**	Process
MT5C1008	F	-12	L	/*
MT5C1008	F	-15	L	/*
MT5C1008	F	-20	L	/*
MT5C1008	F	-25	L	/*
MT5C1008	F	-35	L	/*
MT5C1008	F	-45	L	/*
MT5C1008	F	-55	L	/*
MT5C1008	F	-70	L	/*

EXAMPLE: MT5C1008DCJ-35/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1008	DCJ	-12	L	/*
MT5C1008	SOJ	-12	L	/*
MT5C1008	DCJ	-15	L	/*
MT5C1008	SOJ	-15	L	/*
MT5C1008	DCJ	-20	L	/*
MT5C1008	SOJ	-20	L	/*
MT5C1008	DCJ	-25	L	/*
MT5C1008	SOJ	-25	L	/*
MT5C1008	DCJ	-35	L	/*
MT5C1008	SOJ	-35	L	/*
MT5C1008	DCJ	-45	L	/*
MT5C1008	SOJ	-45	L	/*
MT5C1008	DCJ	-55	L	/*
MT5C1008	SOJ	-55	L	/*
MT5C1008	DCJ	-70	L	/*
MT5C1008	SOJ	-70	L	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range   -40°C to +85°C
XT = Extended Temperature Range   -55°C to +125°C
883C = Full Military Processing   -55°C to +125°C

** OPTIONS

L = 2V Data Retention/Low Power

ASI

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ASI TO DSCC PART NUMBER
CROSS REFERENCE

ASI Package Designator C & CW

ASI Part #	SMD Part #
MT5C1008C-20/883C	5962-8959838MZA
MT5C1008C-20L/883C	5962-8959821MZA
MT5C1008C-25/883C	5962-8959837MZA
MT5C1008C-25L/883C	5962-8959820MZA
MT5C1008C-35/883C	5962-8959836MZA
MT5C1008C-35L/883C	5962-8959819MZA
MT5C1008C-45/883C	5962-8959835MZA
MT5C1008C-45L/883C	5962-8959818MZA
MT5C1008C-55/883C	5962-8959834MZA
MT5C1008C-55L/883C	5962-8959817MZA
MT5C1008C-70/883C	5962-8959833MZA
MT5C1008C-70L/883C	5962-8959816MZA
MT5C1008CW-20/883C	5962-8959838MXA
MT5C1008CW-20L/883C	5962-8959821MXA
MT5C1008CW-25/883C	5962-8959837MXA
MT5C1008CW-25L/883C	5962-8959820MXA
MT5C1008CW-35/883C	5962-8959836MXA
MT5C1008CW-35L/883C	5962-8959819MXA
MT5C1008CW-45/883C	5962-8959835MXA
MT5C1008CW-45L/883C	5962-8959818MXA
MT5C1008CW-55/883C	5962-8959834MXA
MT5C1008CW-55L/883C	5962-8959817MXA
MT5C1008CW-70/883C	5962-8959833MXA
MT5C1008CW-70L/883C	5962-8959816MXA

ASI Package Designator EC & ECA

ASI Part #	SMD Part #
MT5C1008EC-20/883C	5962-8959838MUA
MT5C1008EC-20L/883C	5962-8959821MUA
MT5C1008EC-25/883C	5962-8959837MUA
MT5C1008EC-25L/883C	5962-8959820MUA
MT5C1008EC-35/883C	5962-8959836MUA
MT5C1008EC-35L/883C	5962-8959819MUA
MT5C1008EC-45/883C	5962-8959835MUA
MT5C1008EC-45L/883C	5962-8959818MUA
MT5C1008EC-55/883C	5962-8959834MUA
MT5C1008EC-55L/883C	5962-8959817MUA
MT5C1008EC-70/883C	5962-8959833MUA
MT5C1008EC-70L/883C	5962-8959816MUA
MT5C1008ECA-20/883C	5962-8959838MMA
MT5C1008ECA-20L/883C	5962-8959821MMA
MT5C1008ECA-25/883C	5962-8959837MMA
MT5C1008ECA-25L/883C	5962-8959820MMA
MT5C1008ECA-35/883C	5962-8959836MMA
MT5C1008ECA-35L/883C	5962-8959819MMA
MT5C1008ECA-45/883C	5962-8959835MMA
MT5C1008ECA-45L/883C	5962-8959818MMA
MT5C1008ECA-55/883C	5962-8959834MMA
MT5C1008ECA-55L/883C	5962-8959817MMA
MT5C1008ECA-70/883C	5962-8959833MMA
MT5C1008ECA-70L/883C	5962-8959816MMA

ASI Package Designator F

ASI Part #	SMD Part #
MT5C1008F-20/883C	5962-8959838MTA
MT5C1008F-20L/883C	5962-8959821MTA
MT5C1008F-25/883C	5962-8959837MTA
MT5C1008F-25L/883C	5962-8959820MTA
MT5C1008F-35/883C	5962-8959836MTA
MT5C1008F-35L/883C	5962-8959819MTA
MT5C1008F-45/883C	5962-8959835MTA
MT5C1008F-45L/883C	5962-8959818MTA
MT5C1008F-55/883C	5962-8959834MTA
MT5C1008F-55L/883C	5962-8959817MTA
MT5C1008F-70/883C	5962-8959833MTA
MT5C1008F-70L/883C	5962-8959816MTA

ASI Package Designator DCJ & SOJ

ASI Part #	SMD Part #
MT5C1008DCJ-20/883C	5962-8959838M7A
MT5C1008DCJ-20L/883C	5962-8959821M7A
MT5C1008DCJ-25/883C	5962-8959837M7A
MT5C1008DCJ-25L/883C	5962-8959820M7A
MT5C1008DCJ-35/883C	5962-8959836M7A
MT5C1008DCJ-35L/883C	5962-8959819M7A
MT5C1008DCJ-45/883C	5962-8959835M7A
MT5C1008DCJ-45L/883C	5962-8959818M7A
MT5C1008DCJ-55/883C	5962-8959834M7A
MT5C1008DCJ-55L/883C	5962-8959817M7A
MT5C1008DCJ-70/883C	5962-8959833M7A
MT5C1008DCJ-70L/883C	5962-8959816M7A
MT5C1008SOJ-20/883C	5962-8959838MYA
MT5C1008SOJ-20L/883C	5962-8959821MYA
MT5C1008SOJ-25/883C	5962-8959837MYA
MT5C1008SOJ-25L/883C	5962-8959820MYA
MT5C1008SOJ-35/883C	5962-8959836MYA
MT5C1008SOJ-35L/883C	5962-8959819MYA
MT5C1008SOJ-45/883C	5962-8959835MYA
MT5C1008SOJ-45L/883C	5962-8959818MYA
MT5C1008SOJ-55/883C	5962-8959834MYA
MT5C1008SOJ-55L/883C	5962-8959817MYA
MT5C1008SOJ-70/883C	5962-8959833MYA
MT5C1008SOJ-70L/883C	5962-8959816MYA

* ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.

DATE: 2/6/01

Technical Note:
128Kx8 SRAM – Maximum Recommended Supply Voltage and Ambient Temperature

Compliance:

This product fully meets and is tested in compliance with SMD# 5962-89598 and tested in accordance with JESD78.

Specific Product Affected:

Die Manufacturer: Alliance Semiconductor Corporation
Die Name: AS2008SA
Device Types: MT5C1008 , MT5C1009
Speed Grades: All
Package Designators: All
Identifying Date Code Marking: Change implemented on product starting with date code 0100.

Characteristic Identified:

Austin Semiconductor, Inc. has received notification from this die vendor, Alliance Semiconductor Corp., that operation at high Vcc's of 6 volts and beyond may result in a latch-up condition. This can cause permanent damage to the device.

Recommendation:

During use in system applications and during manufacturing processes, including Burn-In and Test, the devices should not be subjected to Vcc Supply Voltages higher than 5.5Volts at 125°C.

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Austin Semiconductor, Inc. reserves the right to change products or specifications without notice.