# ASDN laboratory_01

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LaTeX

**Subject:** studierea practică şi cercetarea procesului de sinteză a circuitelor logice combinaţionale.

**Conditions:**

- 1. Se verifică corectitudinea funcţionării circuitelor integrate ale standului de laborator.
  2. Se asamblează şi se reglează circuitul logic combinaţional, care realizează două funcţii din tema pentru acasă în setul de elemente ŞI-NU (la indicaţia profesorului).
  3. Pentru circuitele asamblate se determină costul şi timpul de reţinere.
- 1. Din biblioteca de elemente Simulation Gates.clf se selectează elementele NAND cu numărul corespunzător de intrări. Din biblioteca Simulation IO.clf se selectează dispozitivele de intrare-ieşire Binary Probe şi Hex Keyboard.
  2. Se asamblează circuitul logic combinaţional în Fereastra de lucru şi se verifică corectitudinea lui. Se studiază diagrama de timp. Un exemplu al circuitului asamblat este prezentat în fig. 2.1.
  3. Pentru circuitele asamblate se determină costul şi timpul de reţinere.

# 1 First function

$$y_1 = \Sigma(0, 1, 2, 4, 5, 8, 9, 12, 14)$$

## 1.1 Karnaugh map

| $x_3x_4$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 1 | 0 |

| $x_3x_4$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 1 | 0 |

## 1.2 Disjunctiv minimal form

$$F_{DM} = (x_1 \cdot x_2 \cdot \overline{x_4}) + (\overline{x_2} \cdot \overline{x_3}) + (\overline{x_1} \cdot \overline{x_3}) + (\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_4})$$
$$= \overline{\overline{(x_1 \cdot x_2 \cdot \overline{x_4})} \cdot \overline{(\overline{x_2} \cdot \overline{x_3})} \cdot \overline{(\overline{x_1} \cdot \overline{x_3})} \cdot \overline{(\overline{x_1} \cdot \overline{x_2} \cdot \overline{x_4})}}$$

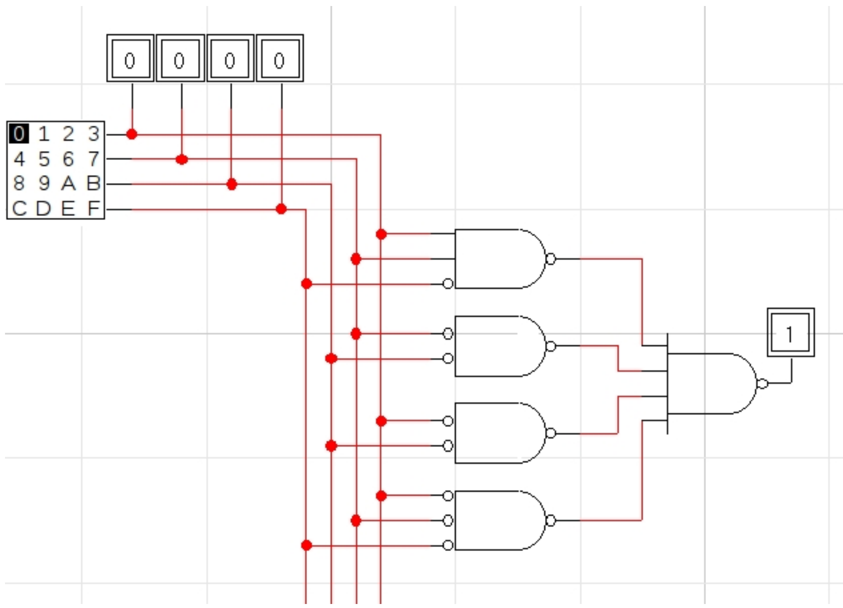


Figure 1: Circuit $y_1$, $F_{DM}$.

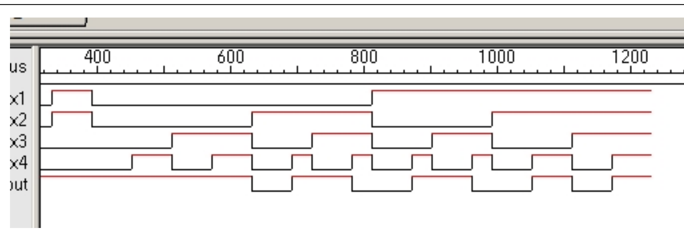


Figure 2: Circuit $y_1$, $F_{DM}$ Timer.

C = 14Q
$T_d = 2r$

## 1.3 Conjunctive minimal form

$$F_{CM} = (x_1 + \overline{x_2} + \overline{x_3}) \cdot (\overline{x_1} + \overline{x_2} + \overline{x_4}) \cdot (\overline{x_1} + x_2 + \overline{x_3}) \cdot (\overline{x_3} + \overline{x_4})$$
$$= \overline{\overline{(x_1 + \overline{x_2} + \overline{x_3})} + \overline{(\overline{x_1} + \overline{x_2} + \overline{x_4})} + \overline{(\overline{x_1} + x_2 + \overline{x_3})} + \overline{(\overline{x_3} + \overline{x_4})}}$$

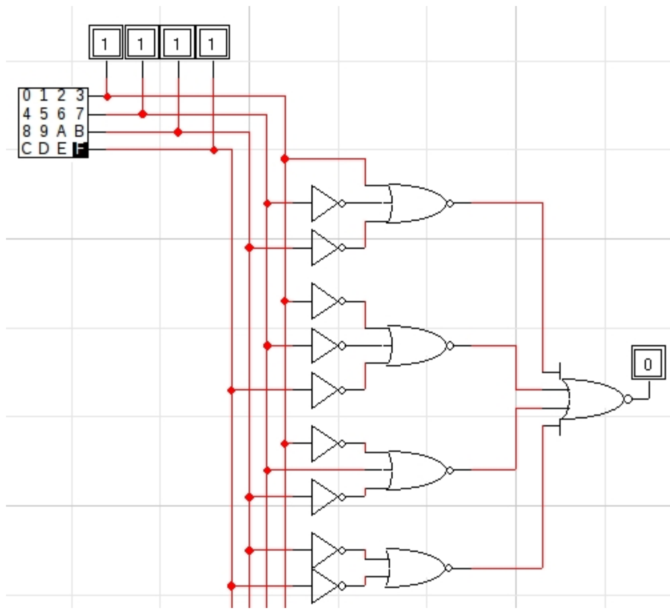

Figure 3: Circuit $y_1$, $F_{CM}$.

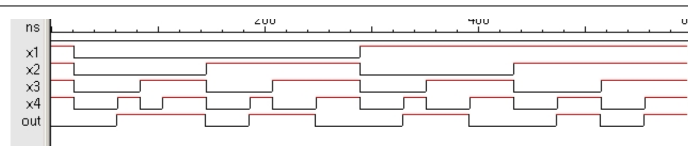

Figure 4: Circuit $y_1$, $F_{CM}$ Timer.

C = 24Q

$T_d = 3r$

# 2 Second function

$$y_1 = \Sigma(1, 2, 3, 5, 6, 8, 10, 11, 12)$$

## 2.1 Karnaugh map

| $x_3x_4$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 1 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 1 | 0 | 1 |

| $x_3x_4$ \ $x_1x_2$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 1 | 1 |
| 01 | 1 | 1 | 0 | 0 |
| 11 | 1 | 0 | 0 | 1 |
| 10 | 1 | 1 | 0 | 1 |

## 2.2 Disjunctiv minimal form

$$F_{DM} = x_1 \cdot \overline{x_3} \cdot \overline{x_4} + \overline{x_1} \cdot \overline{x_3} \cdot x_4 + \overline{x_1} \cdot x_3 \cdot \overline{x_4} + \overline{x_2} \cdot x_3$$
$$= \overline{\overline{(x_1 \cdot \overline{x_3} \cdot \overline{x_4})} \cdot \overline{(\overline{x_1} \cdot \overline{x_3} \cdot x_4)} \cdot \overline{(\overline{x_1} \cdot x_3 \cdot \overline{x_4})} \cdot \overline{(\overline{x_2} \cdot x_3)}}$$

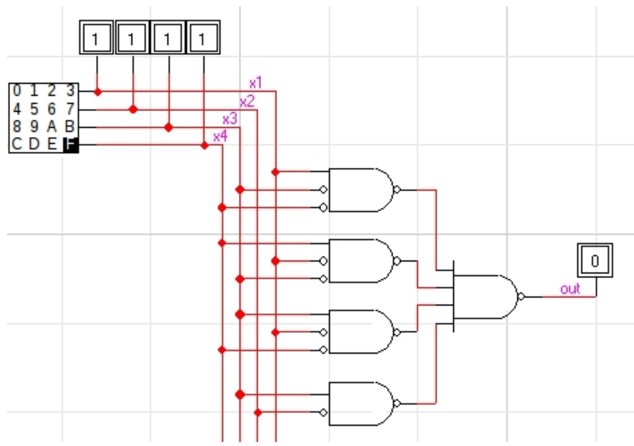


Figure 5: Circuit $y_2$, $F_{DM}$.

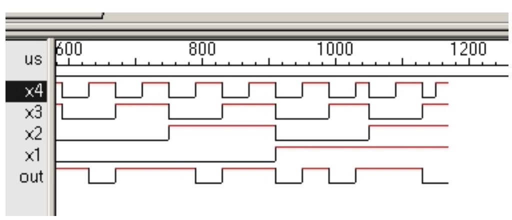


Figure 6: Circuit $y_2$, $F_{DM}$ Timer.

$$\text{C} = 15\text{Q}$$
$$T_d = 2r$$

## 2.3 Conjunctiv minimal form

$$F_{CM} = (x_1 + x_3 + x_4) \cdot (\overline{x_1} + x_3 + \overline{x_4}) \cdot (\overline{x_2} + \overline{x_3} + \overline{x_4}) \cdot (\overline{x_1} + \overline{x_2} + \overline{x_3})$$
$$= \overline{\overline{(x_1 + x_3 + x_4)} + \overline{(\overline{x_1} + x_3 + \overline{x_4})} + \overline{(\overline{x_2} + \overline{x_3} + \overline{x_4})} + \overline{(\overline{x_1} + \overline{x_2} + \overline{x_3})}}$$

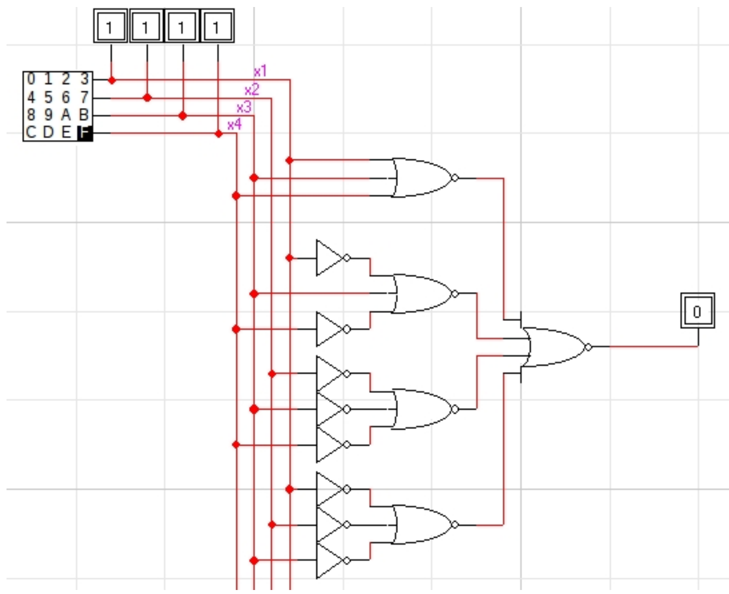

Figure 7: Circuit $y_2$, $F_{CM}$.

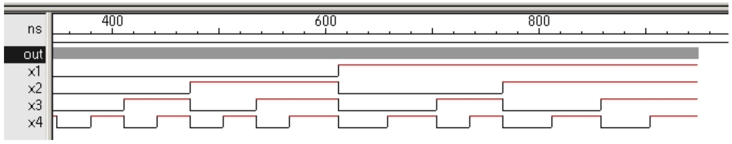

Figure 8: Circuit $y_2$, $F_{CM}$ Timer.

C = 24Q
$T_d = 3r$

## 3 Conclusion

- De Morgan's laws helps us very much in minimizing the expression. It allows us to use only one type of gate. In this way, we can create a much cheaper circuit, since we have to buy only one kind of gate.
- Karnaugh maps are a much better representation of a circuit than a truth table. But we can't represent the circuits with too many signals in it.