

# Report

№: 3

ASDN

**Subject:** The Analysis and Synthesis of numerical devices

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# 1 Objectives

- verify the correct operation of the laboratory bench integrated circuits;
- assemble and adjust the schema of a binary-decimal decoder in the home theme in the AND-NO set;
- assemble and adjust the schema of a binary-decimal encoder in the home theme in the AND-NO set;
- for the assembled circuits the cost and the retention time are determined;

# 2 Docoder

Encoder: 8 3 2 (-4)

Decoder: 5 2 1 1

Decimal numbers	Code				Functions									
	8	3	2	(-4)										
	$x_1$	$x_2$	$x_3$	$x_4$	$y_0$	$y_1$	$y_2$	$y_3$	$y_4$	$y_5$	$y_6$	$y_7$	$y_8$	$y_9$
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	1	0	0	0	0	0	0	0
3	0	1	0	0	0	0	0	1	0	0	0	0	0	0
4	1	0	0	1	0	0	0	0	1	0	0	0	0	0
5	0	1	1	0	0	0	0	0	0	1	0	0	0	0
6	1	0	1	1	0	0	0	0	0	0	1	0	0	0
7	1	1	0	1	0	0	0	0	0	0	0	1	0	0
8	1	0	0	0	0	0	0	0	0	0	0	0	1	0
9	1	1	1	1	0	0	0	0	0	0	0	0	0	1
	0	0	0	1										
	0	0	1	1										
	0	1	0	1										
	1	0	1	0										
	1	1	0	0										
	1	1	1	0										

**Tab 1:** Code decoder

$x_3x_4$		$x_1x_2$				$x_3x_4$		$x_1x_2$			
		00	01	11	10			00	01	11	10
00		1	0	*	0	00		0	0	*	0
01		*	*	0	0	01		*	*	0	0
11		*	0	0	0	11		*	1	0	0
10		0	0	*	*	10		0	0	*	*
$y_0 = \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3}$						$y_1 = \overline{x_1}x_4$					
$x_3x_4$		$x_1x_2$				$x_3x_4$		$x_1x_2$			
		00	01	11	10			00	01	11	10
00		0	0	*	0	00		0	1	*	0
01		*	*	0	0	01		*	*	0	0
11		*	0	0	0	11		*	0	0	0
10		1	0	*	*	10		0	0	*	*
$y_2 = \overline{x_1} \cdot \overline{x_2}x_3$						$y_3 = x_2\overline{x_3} \cdot \overline{x_4}$					
$x_3x_4$		$x_1x_2$				$x_3x_4$		$x_1x_2$			
		00	01	11	10			00	01	11	10
00		0	0	*	0	00		0	0	*	0
01		*	*	0	0	01		*	*	0	0
11		*	0	0	0	11		*	0	0	0
10		1	0	*	*	10		0	0	*	*
$y_4 = \overline{x_2} \cdot \overline{x_3}x_4$						$y_5 = x_2x_3\overline{x_4}$					
$x_3x_4$		$x_1x_2$				$x_3x_4$		$x_1x_2$			
		00	01	11	10			00	01	11	10
00		0	0	*	0	00		0	0	*	0
01		*	*	0	1	01		*	*	0	0
11		*	0	0	0	11		*	0	0	0
10		0	0	*	*	10		0	1	*	*

**Tab 2:** Karnaugh maps (1)



### 3 Encoder

Decimal number	Inputs										Outputs			
											5	2	1	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	0	0	0	0	0	1	1
3	0	0	0	1	0	0	0	0	0	0	0	1	0	1
4	0	0	0	0	1	0	0	0	0	0	0	1	1	1
5	0	0	0	0	0	1	0	0	0	0	1	0	0	0
6	0	0	0	0	0	0	1	0	0	0	1	0	1	0
7	0	0	0	0	0	0	0	1	0	0	1	1	0	0
8	0	0	0	0	0	0	0	0	1	0	1	1	1	0
9	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	$x_0$	$x_1$	$x_2$	$x_3$	$x_4$	$x_5$	$x_6$	$x_7$	$x_8$	$x_9$	$f_4$	$f_3$	$f_2$	$f_1$

Tab 4: Encoder

$$f_1 = \overline{x_1} \cdot \overline{x_2} \cdot \overline{x_3} \cdot \overline{x_4} \cdot \overline{x_9}$$

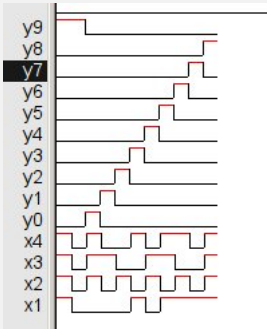
$$f_2 = \overline{x_2} \cdot \overline{x_4} \cdot \overline{x_6} \cdot \overline{x_8} \cdot \overline{x_9}$$

$$f_3 = \overline{x_3} \cdot \overline{x_4} \cdot \overline{x_7} \cdot \overline{x_8} \cdot \overline{x_9}$$

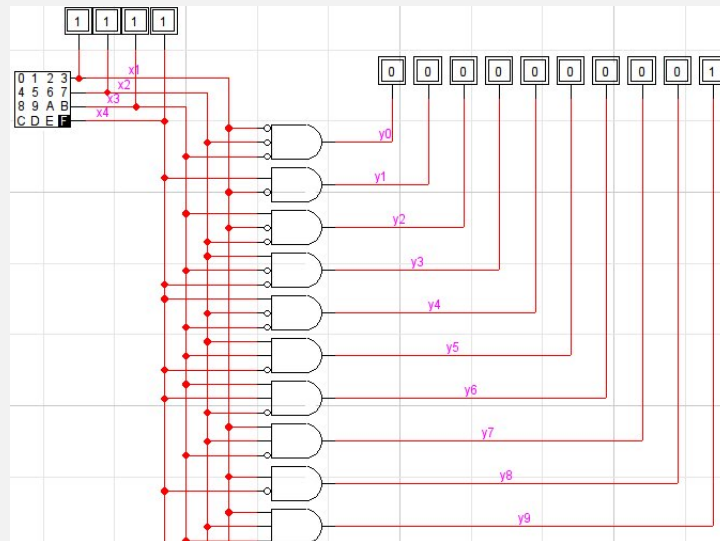
$$f_4 = \overline{x_5} \cdot \overline{x_6} \cdot \overline{x_7} \cdot \overline{x_8} \cdot \overline{x_9}$$

Tab 5: NAND form of decoder functions

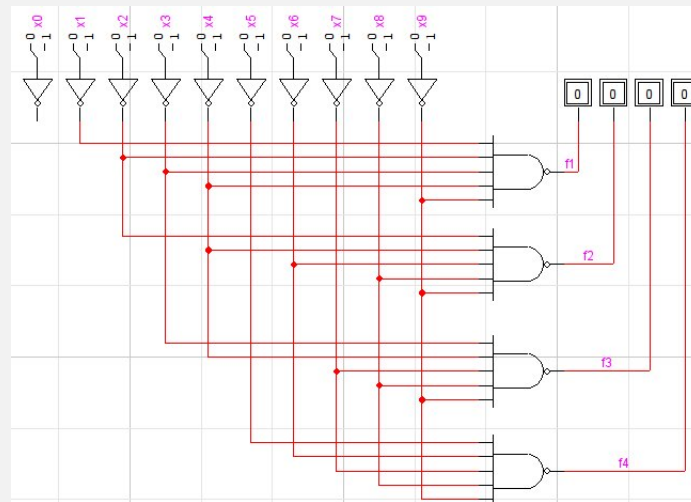
### 4 Circuits



Img 1: Decoder timer



**Img 2: Decoder**



**Img 3: Encoder**

Circuit	Cost	Time
1	28	1
2	30	2

**Tab 6: Cost and time**

## 5 Conclusion

This laboratory work taught me how to create circuits for decoders and encoders. They are extremely important parts of circuits and information interchange and processing can't be realized without them.