ECE 331 - Fall 2024

Homework 7

Assigned, November 20 - Due Monday,
December 2nd 11:59 PM

1. Consider 21 bit VPN 0x000E3C and page offset 0x22A. Assuming a 1KB page size, 2 byte page table entries, and 14 bit Physical Page Numbers, answer the following:

   (a) What is the capacity of the virtual memory?

   (b) What is the capacity of the physical memory?

   (c) How many page table entries are there?

   (d) What is the byte address of the PTE corresponding to the above VPN if the contents of the page register is Ox0002F4. How many bytes of RAM does the page table occupy?

2. Consider a fully associative TLB with a capacity of 16 virtual-to-physical page translations. Assuming that the physical memory has a capacity of 16K pages, each 2KB in size, and a 32-bit address, answer the following:

   (a) How many bits are associated with each PTE (including one valid bit and one dirty bit)?

   (b) How many bits are associated with each page translation in the TLB (including one valid bit and one dirty bit)?

   (c) How many bits must the page table register hold?

   (d) How many bits of left-shifting must the PPN undergo for determination of the physical memory address of the first byte of a physical page?

   (e) How many address bits are required for the physical memory? What is the capacity of this memory in bytes?

3. Solve the attached problem on virtual memory from a previous ECE 331 Final Exam.

Consider a processor with 32-bit virtual addresses. Assuming a 4 KB (2^{12} bytes) page size, 2 byte page table entries (which include one valid bit and one dirty bit), answer the following:

(a) [**2pt**] What is the capacity of the virtual memory in terms of bytes? Show all work. It is OK to leave your answer as a number raised to an exponent.

(b) [**2pt**] What is the maximum capacity of the physical memory this virtual memory system can support? Express your answer in bytes. Show your work.

(c) [**2pt**] What is the memory cost to store the whole page table in the memory? Express your answer in bytes. Show your work.

(d) [**14pt**] Consider a fully associative TLB with 4 virtual-to-physical page translation entries and the Least-Recently Used (LRU) method is used for the replacement strategy. The initial state of TLB is given in the first table. The initial state of page table is shown in the next page. If pages must be brought in from disk, increment the largest current page number in the table. For example, the next page fetched for the initial page table would be *0xD*. We have following memory accesses

```
0x00000FFF, 0x00007A28, 0x00003DAD, 0x00003A98, 0x00001B19,
0x00001300, 0x00002D00
```

Please update the TLB entry for each memory access by filling out the following TLB state tables. ***Please use hexadecimal numbers for VPN and PPN. Use "1" for valid and "0" for invalid.***

Initial TLB state:

Valid	Tag (VPN)	PPN
1	0xB	0xC
0	0x7	0x4
0	0x3	0x6
0	0x4	0x9

TLB state after the 1st access:

Valid	Tag (VPN)	PPN

TLB state after the 2nd access:

Valid	Tag (VPN)	PPN

TLB state after the 3rd access:

Valid	Tag (VPN)	PPN

TLB state after the 4th access:

Valid	Tag (VPN)	PPN

TLB state after the 5th access:

Valid	Tag (VPN)	PPN

TLB state after the 6th access:

Valid	Tag (VPN)	PPN

TLB state after the 7th access:

Valid	Tag (VPN)	PPN

The initial page table in the memory:

VPN	Valid:	PPN or in disk
0x0	1	0x5
0x1	0	Disk
0x2	0	Disk
0x3	1	0x6
0x4	0	Disk
0x5	1	0xB
0x6	0	Disk
0x7	1	0x4
0x8	0	Disk
0x9	0	Disk
0xA	1	0x3
0xB	1	0xC
More entries …	…	…

(e) [**5pt**] What is the final state of page table after memory accesses in (d)? Fill out the following table to show your answer.

VPN	Valid:	PPN or in disk
0x0		
0x1		
0x2		
0x3		
0x4		
0x5		
0x6		
0x7		
0x8		
0x9		
0xA		
0xB		
More entries …	…	…