ECE124: Discussion

Discussion #13

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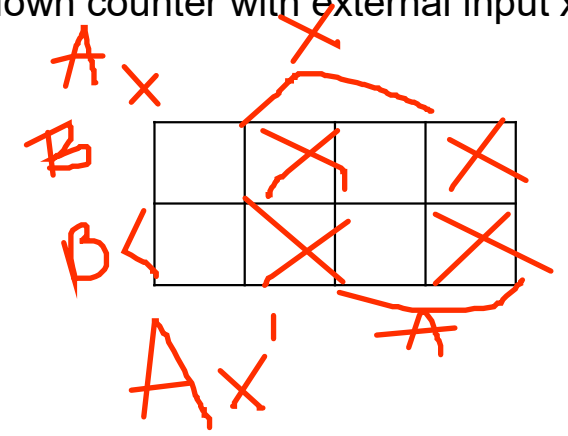
*Up-Down Counter Using T flip-flops, design a 2-bit up-down counter with external input x to determine whether Up or Down.

Present state		Input	Next state		FF inputs	
B	A	x	B(t+1)	A(t+1)	T_B	T_A
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

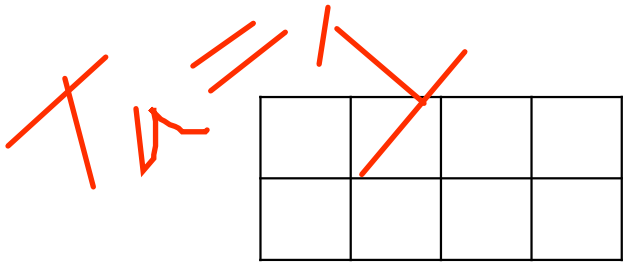


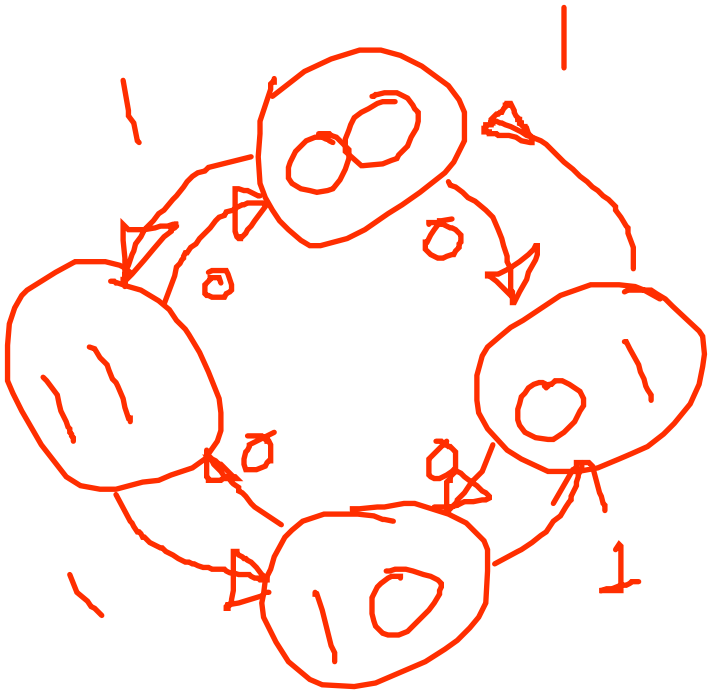
AX'+A'X

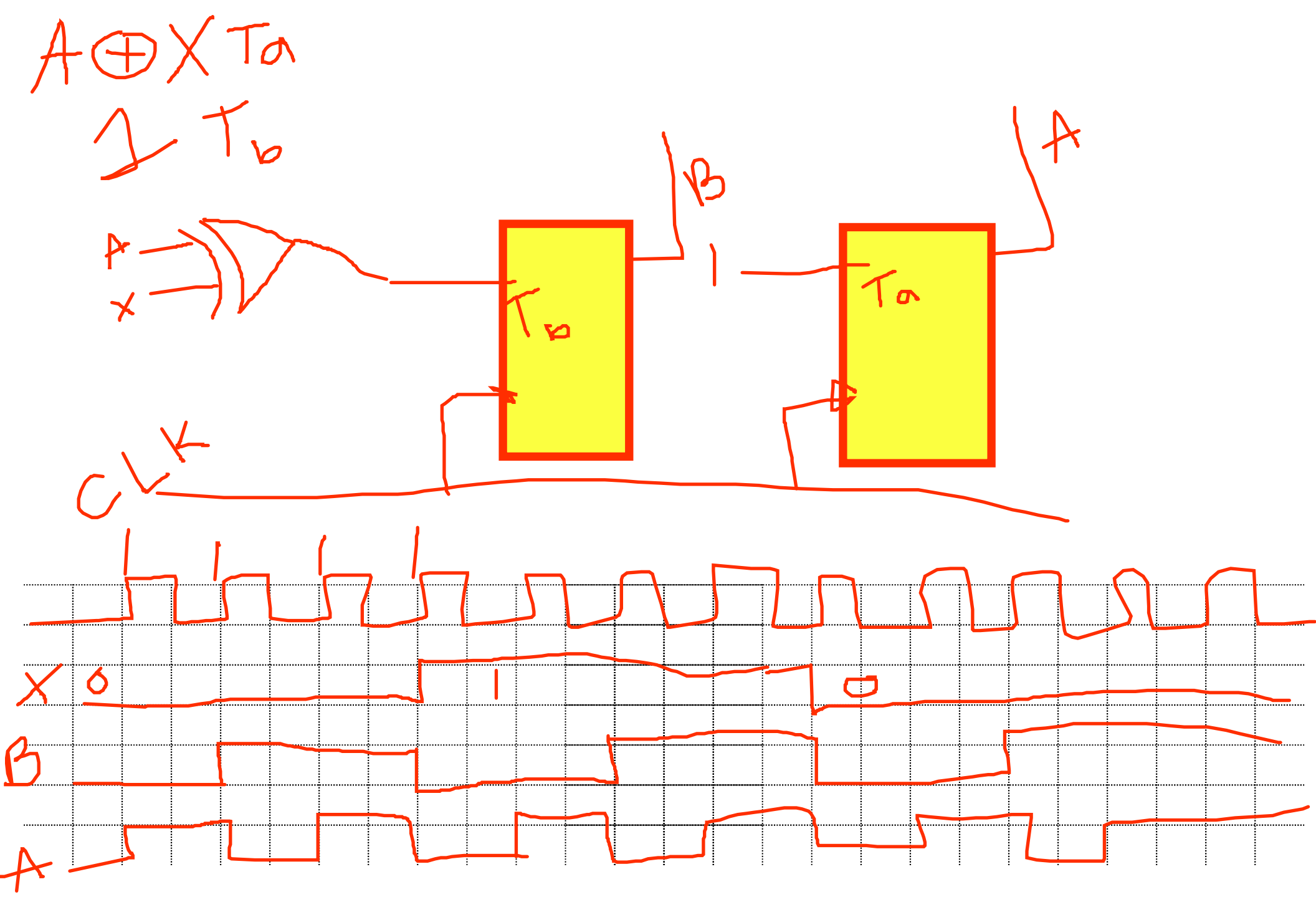
A XOR B

T flipflop table

Q(t) Q(t+1) T

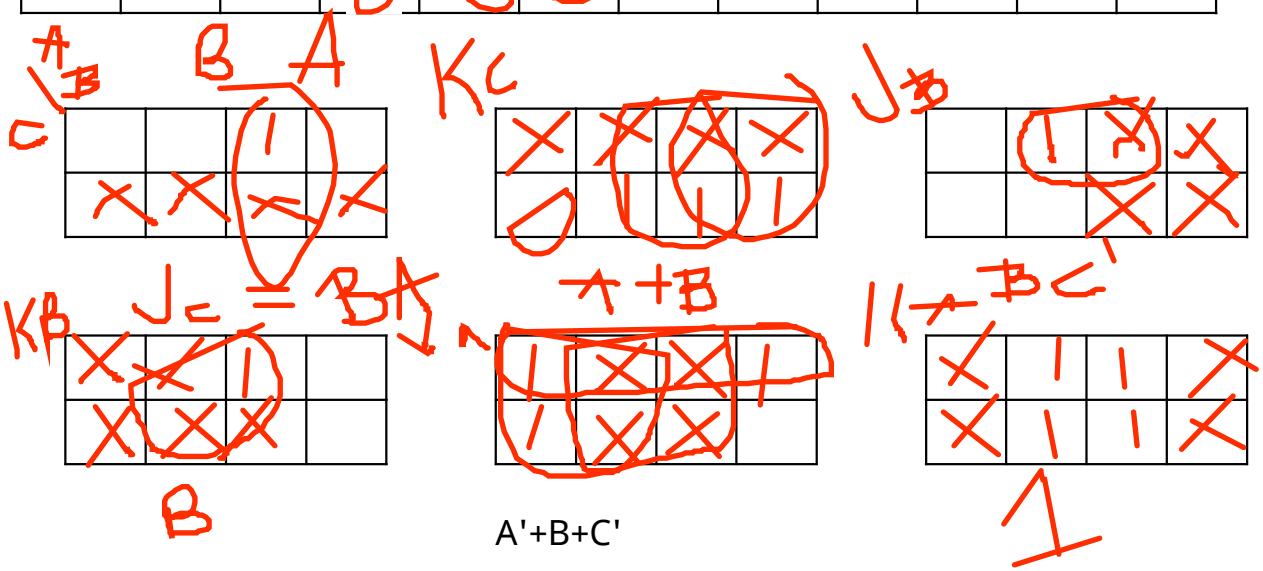


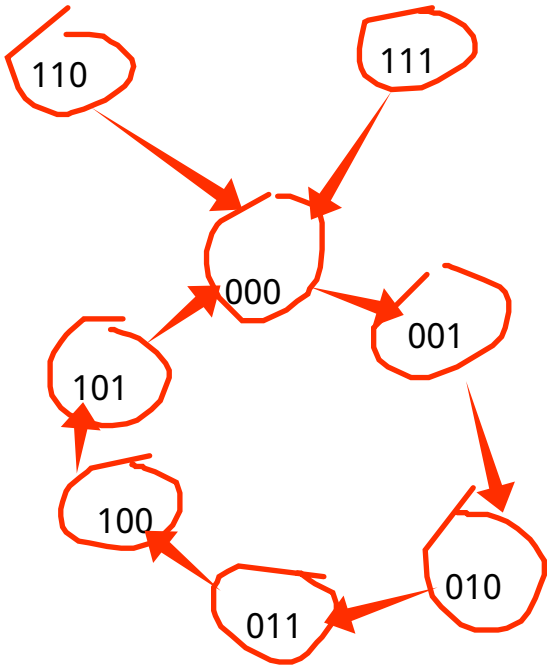


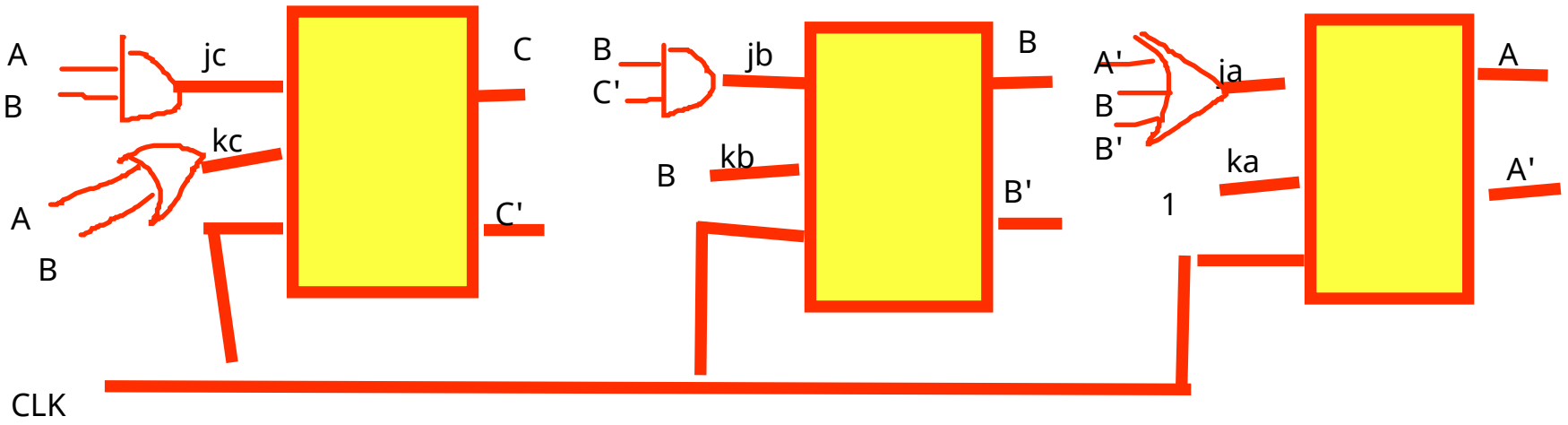

A⊕X To
J Tb
A
X
Tb
B
1
To
A
CLK
X
0
1
0
B
A

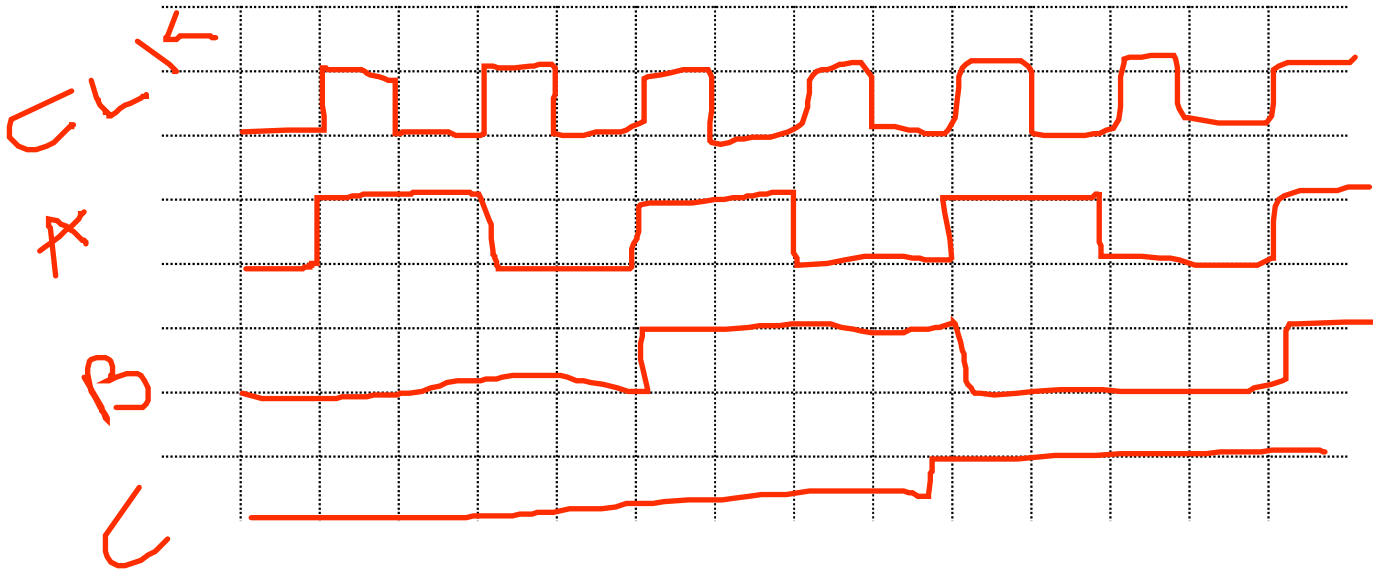
*Mod-6 Counter Using JK flip-flops, design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5. In case of 6 and 7, include the self correcting state to 0.

Present State			Next State			Inputs of JK Flip-flops					
C	B	A	C(t+1)	B(t+1)	A(t+1)	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1		X		X	1	X
0	0	1	0	1	0		x	1	x	X	1
0	1	0	0	1	1		x	x		1	x
0	1	1	1	0	0	1	x	x	1	X	1
1	0	0	1	0	1	x			x	1	x
1	0	1	0	0	0	x	1		x	x	1
1	1	0	0	0	0	x	1	x	1		x
1	1	1	0	0	0	x	1	x	x	x	1



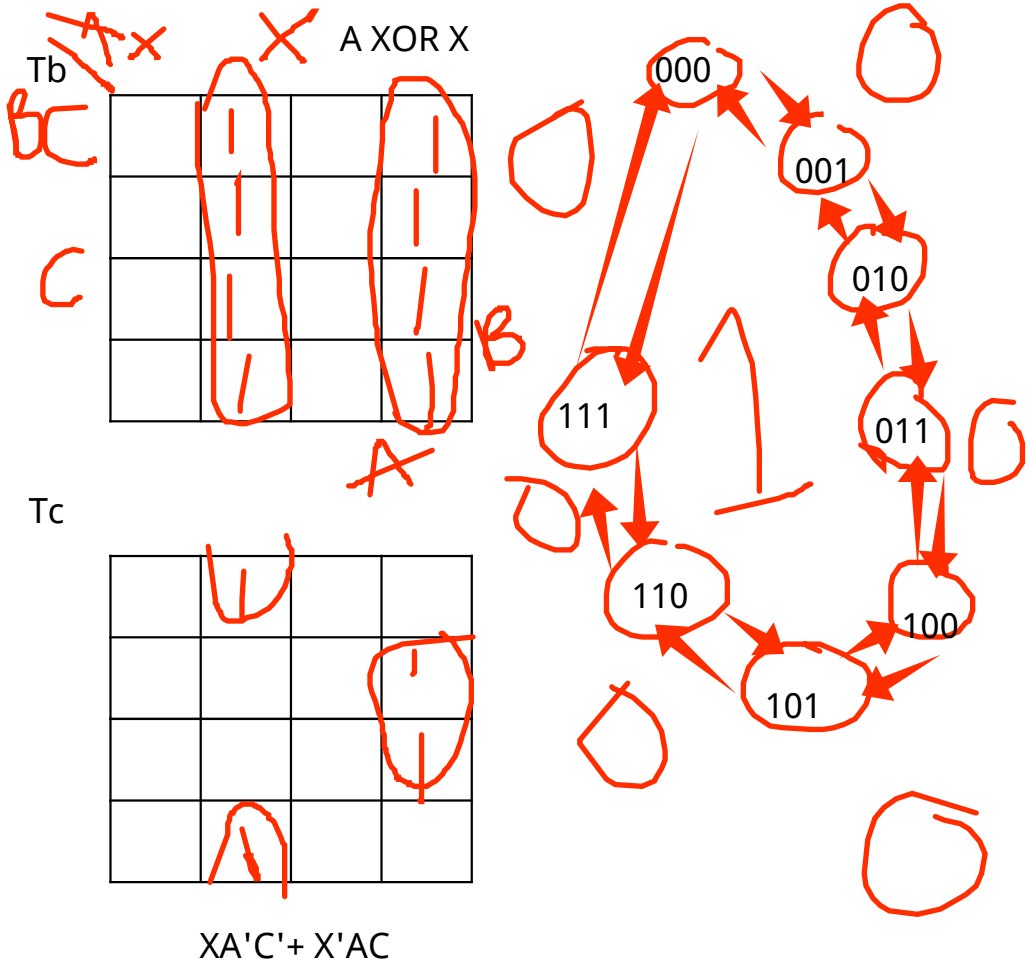



A
B
jc
kc
A
B
C
C'
B
C'
jb
kb
B
B
B'
A'
B
B'
ja
ka
1
A
A'
CLK

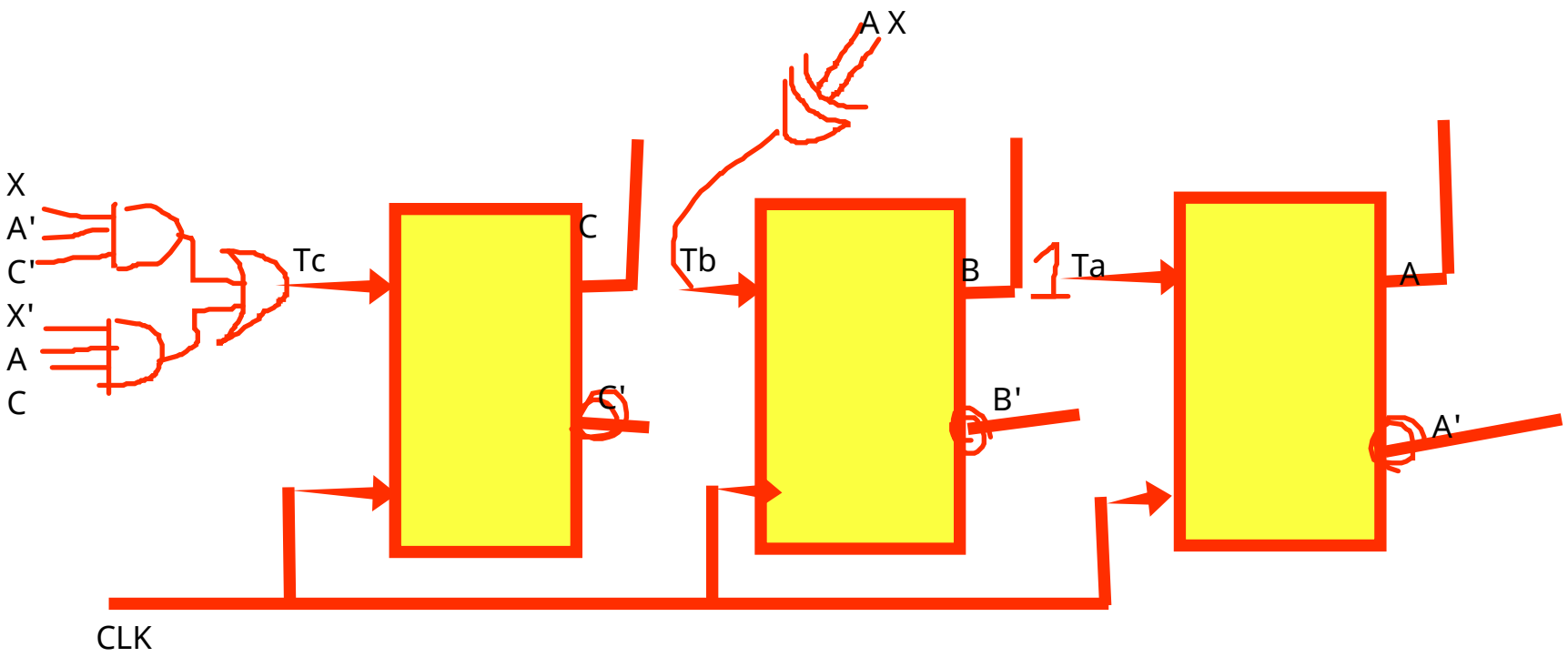

CLK
A
B
C

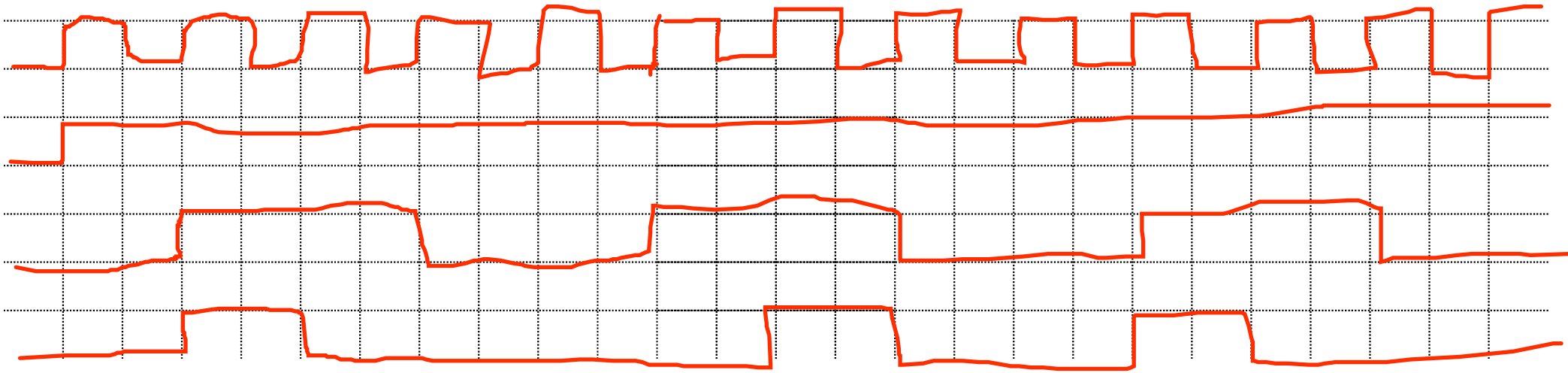
*Up-Down Counter Using T flip-flops, design a 3-bit up-down counter with external input x to determine whether Up or Down.

Present state			Input	Next state			FF inputs		
C	B	A	x	C(t+1)	B(t+1)	A(t+1)	T_C	T_B	T_A
0	0	0	0			1			1
0	0	0	1	1	1	1	1	1	1
0	0	1	0		1			1	1
0	0	1	1						1
0	1	0	0		1	1			1
0	1	0	1			1		1	1
0	1	1	0	1			1	1	1
0	1	1	1		1				1
1	0	0	0	1		1			1
1	0	0	1		1	1	1	1	1
1	0	1	0	1	1			1	1
1	0	1	1	1					1
1	1	0	0	1	1	1			1
1	1	0	1	1		1		1	1
1	1	1	0				1	1	1
1	1	1	1	1	1				1



Ta = 1

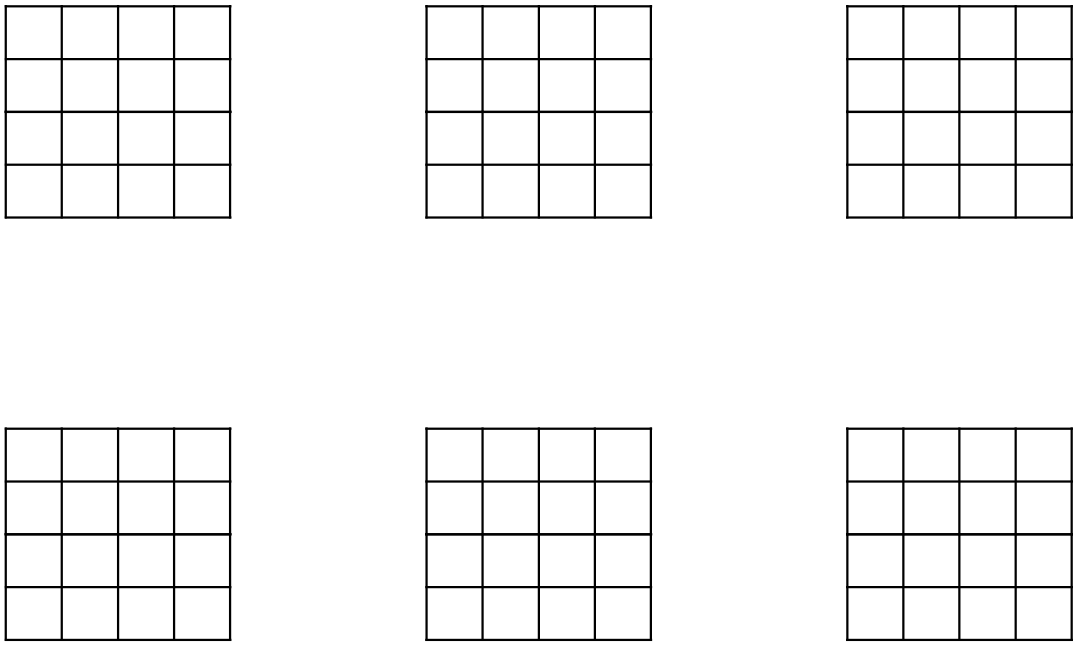

A X
X
A'
C'
X'
A
C
Tc
C
C'
Tb
B
B'
1
Ta
A
A'
CLK



- Design of 3-bit binary up/down counter

Present State	External Input	Next State	Inputs of FFs					
C B A	x	C B A	J_C	K_C	J_B	K_B	J_A	K_A
0 0 0	0	0 0 1	0	X	0	X	1	X
0 0 0	1	1 1 1	1	X	1	X	1	X
0 0 1	0	0 1 0	0	X	1	X	X	1
0 0 1	1	0 0 0	0	X	0	X	X	1
0 1 0	0	0 1 1	0	X	X	0	1	X
0 1 0	1	0 0 1	0	X	X	1	1	X
0 1 1	0	1 0 0	1	X	X	1	X	1
0 1 1	1	0 1 0	0	X	X	0	X	1
1 0 0	0	1 0 1	X	0	0	X	1	X
1 0 0	1	0 1 1	X	1	1	X	1	X
1 0 1	0	1 1 0	X	0	1	X	X	1
1 0 1	1	1 0 0	X	0	0	X	X	1
1 1 0	0	1 1 1	X	0	X	0	1	X
1 1 0	1	1 0 1	X	0	X	1	1	X
1 1 1	0	0 0 0	X	1	X	1	X	1
1 1 1	1	1 1 0	X	0	X	0	X	1

- Design of 3-bit binary up/down counter



- Design of 3-bit binary up/down counter