ECE124: Discussion

Discussion #9

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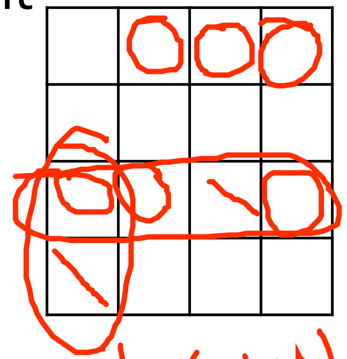
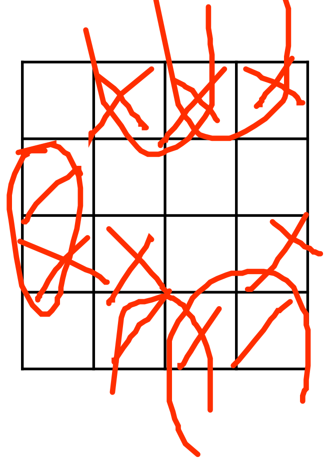
- Design a code converter that converts a decimal digit from
  (a) The 8, 4, -2, -1 code to BCD

dont care conditions are the minterms that exist outside the range bc 1 digit

	W	X	Y	Z	A	B	C	D
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								



A = WX+WY'



B = X'Z+X'Y+XY'Z'

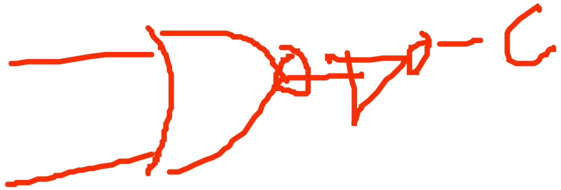
$C = YZ' + Y'Z$

NAND

$C' = (YZ' + Y'Z)' = (YZ')'(Y'Z)'$

$C'' = (((YZ')'(Y'Z)')'$

$C = (Y' + Z)' + (Y + Z')'$



- Carry Lookahead Equations

Recall $\begin{cases} G_i = A_i B_i \leftarrow \text{"carry generate" for stage } i \\ P_i = A_i \oplus B_i \leftarrow \text{carry "propagate" for "} \end{cases}$

Full adder $\begin{cases} C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i \\ S_i = A_i \oplus B_i \oplus C_i \end{cases}$

$$\begin{cases} C_{i+1} = G_i + P_i C_i \\ S_i = P_i \oplus C_i \end{cases}$$

$$\begin{cases} C_0 = \text{input carry} \\ C_1 = G_0 + P_0 C_0 \\ C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0 \\ C_3 = G_2 + P_2 C_2 = G_2 + P_2(G_1 + P_1 G_0 + P_1 P_0 C_0) = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \\ C_4 = G_3 + P_3 C_3 = G_3 + P_3(G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0) = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0 \end{cases}$$

$$\begin{cases} S_0 = P_0 \oplus C_0 \\ S_1 = P_1 \oplus C_1 \\ S_2 = P_2 \oplus C_2 \\ S_3 = P_3 \oplus C_3 \end{cases}$$

- Add two number A = 1101 and B = 1001 with input carry C0 = 0 using Boolean expression of IC type 74283, Carry Lookahead Adder.

$$P_i = A_i \oplus B_i \,, \quad G_i = A_i B_i \,, \quad S_i = \begin{cases} S_i = P_i \oplus C_i \\ C_{i+1} = G_i + P_i C_i \end{cases}$$

$C_0 = 0$

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 C_2 = G_2 + P_2(G_1 + P_1 G_0 + P_1 P_0 C_0)$

$C_4 = G_3 + P_3 C_3 = G_3 + P_3(G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0)$

$S_0 = P_0 \oplus C_0$

$S_1 = P_1 \oplus C_1$

$S_2 = P_2 \oplus C_2$

$S_3 = P_3 \oplus C_3$

$P_0 = A_0 \oplus B_0 = 1 \oplus 1 = 0 \,, \quad G_0 = A_0 B_0 = 1$

$P_1 = A_1 \oplus B_1 = 0 \oplus 0 = 0 \,, \quad G_1 = A_1 B_1 = 0$

$P_2 = A_2 \oplus B_2 = 1 \oplus 0 = 1 \,, \quad G_2 = A_2 B_2 = 0$

$P_3 = A_3 \oplus B_3 = 1 \oplus 1 = 0 \,, \quad G_3 = A_3 B_3 = 1$

$C_0 = 0$

$C_1 = G_0 + P_0 C_0 = 1 + (0 \cdot 0) = 1$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0 = 0 + (0 \cdot 1) + 0 \cdot 1 \cdot 0 = 0$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 = 0 + 0 + 0 + 0 = 0$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$
$= 1 + 0 + 0 + 0 + 0 = 1$

$S_0 = P_0 \oplus C_0 = 0 \oplus 0 = 0$

$S_1 = P_1 \oplus C_1 = 0 \oplus 1 = 1$

$S_2 = P_2 \oplus C_2 = 1 \oplus 0 = 1$

$S_3 = P_3 \oplus C_3 = 0 \oplus 0 = 0$

$$\begin{array}{rccccc}
 & & 1 & 0 & 0 & 1 \\
A = & & 1 & 1 & 0 & 1 \\
+\quad B = & & 1 & 0 & 0 & 1 \\
\hline
 & 1 & 0 & 1 & 1 & 0 \\
 & & S_3 & S_2 & S_1 & S_0
\end{array}$$

$\Longrightarrow$ $C_4 = 1$, $C_3 = 0$, $C_2 = 0$, $C_1 = 1$

$\therefore$ overflow

$V = C_4 \oplus C_3$
$= 1 \oplus 0$
$= 1$

- Design a combinational circuits for 3 x 3 multiplier using half-adder and full-adder.

$A_2A_1A_0$, $B_2B_1B_0$

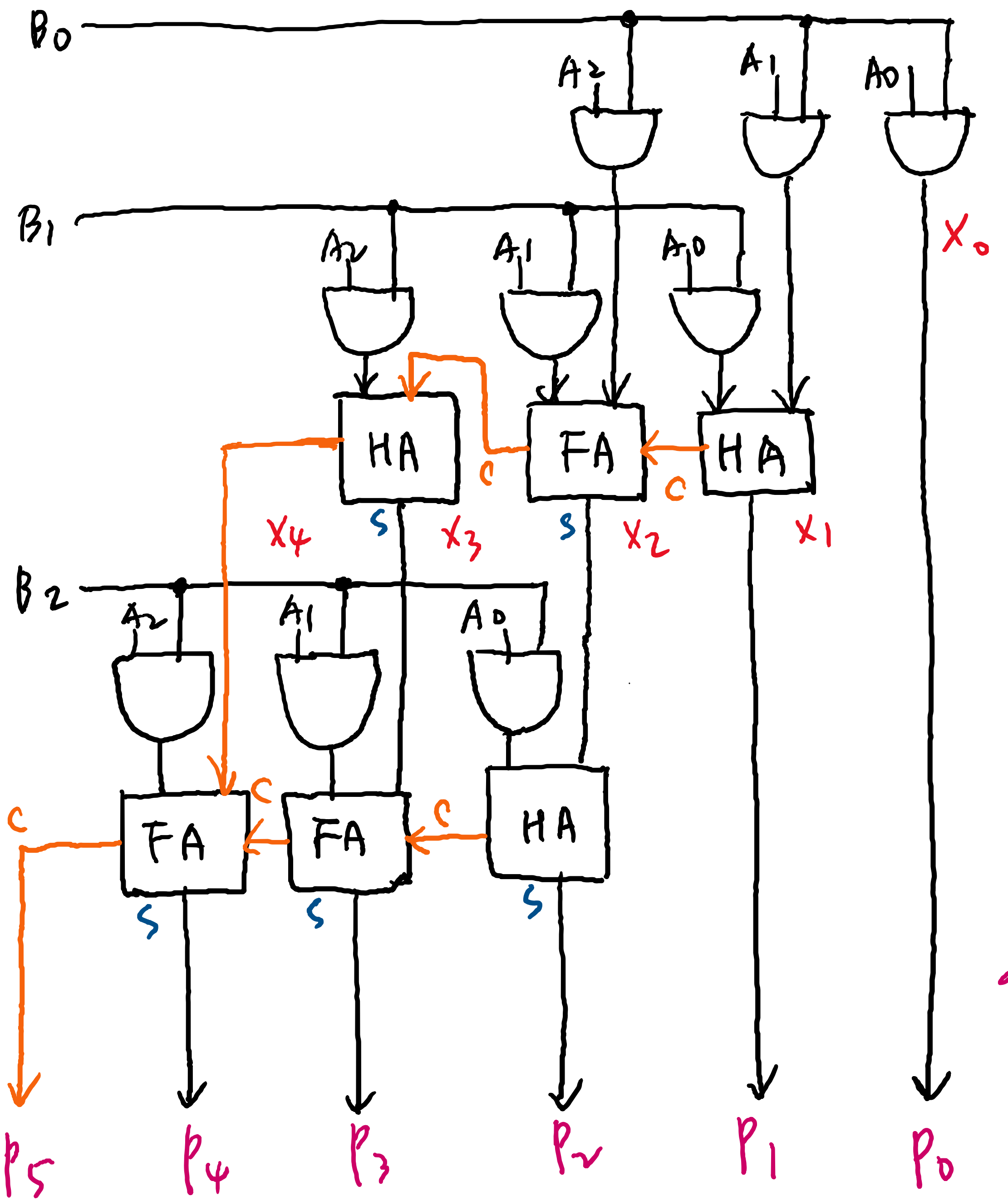
$$
\begin{array}{cccccc}
 & & & A_2 & A_1 & A_0 \\
 & & \times & B_2 & B_1 & B_0 \\
\hline
 & & & A_2B_0 & A_1B_0 & A_0B_0 \\
 & + & A_2B_1 & A_1B_1 & A_0B_1 & \\
\hline
 & X_4 & X_3 & X_2 & X_1 & X_0 \\
 & A_2B_2 & A_1B_2 & A_0B_2 & & \\
\hline
P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$

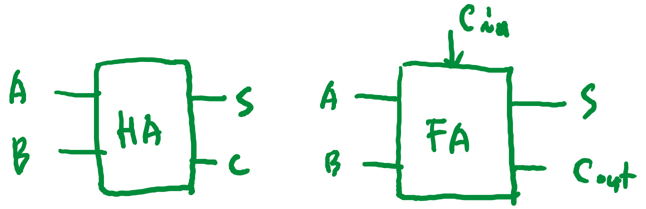
HA FA HA

FA FA HA

$$
\begin{cases}
X_0 = A_0B_0 \\
X_1 = A_1B_0 + A_0B_1 \\
X_2 = A_2B_0 + A_1B_1 + \text{carry from } X_1 \\
X_3 = A_2B_1 + \text{carry from } X_2 \\
X_4 = \text{carry from } X_3
\end{cases}
$$

$$
\begin{cases}
P_0 = X_0 \\
P_1 = X_1 \\
P_2 = X_2 + A_0B_2 \\
P_3 = X_3 + A_1B_2 + \text{carry from } P_2 \\
P_4 = X_4 + A_2B_2 + \text{carry from } P_3 \\
P_5 = \text{carry from } P_4
\end{cases}
$$





$x_0 = A_0B_0$

$x_1 = A_1B_0 + A_0B_1$

$x_2 = A_2B_0 + A_1B_1 +$ carry from x_1

$x_3 = A_2B_1 +$ carry from x_2

$x_4 =$ carry from x_3

$p_0 = x_0$

$p_1 = x_1$

$p_2 = x_2 + A_0B_2$

$p_3 = x_3 + A_1B_2 +$ carry from p_2

$p_4 = x_4 + A_2B_2 +$ carry from p_3

$p_5 =$ carry from p_4

$$
\begin{cases}
X_0 = A_0B_0 \\
X_1 = A_1B_0 + A_0B_1 \\
X_2 = A_2B_0 + A_1B_1 + \text{carry from } X_1 \\
X_3 = A_2B_1 + \text{carry from } X_2 \\
X_4 = \text{carry from } X_3
\end{cases}
$$

Ex)

$$
\begin{array}{rcccccc}
 & & & & 1 & 0 & 1 \\
 & & & \times & 1 & 1 & 1 \\
\hline
 & & & & 1 & 0 & 1 \\
+ & & & 1 & 0 & 1 & \\
\hline
 & & X_4 & X_3 & X_2 & X_1 & X_0 \\
 & & 0 & 1 & 1 & 1 & 1 \\
+ & 1 & 0 & 1 & & & \\
\hline
 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0 \\
 & 1 & 0 & 0 & 0 & 1 & 1
\end{array}
$$

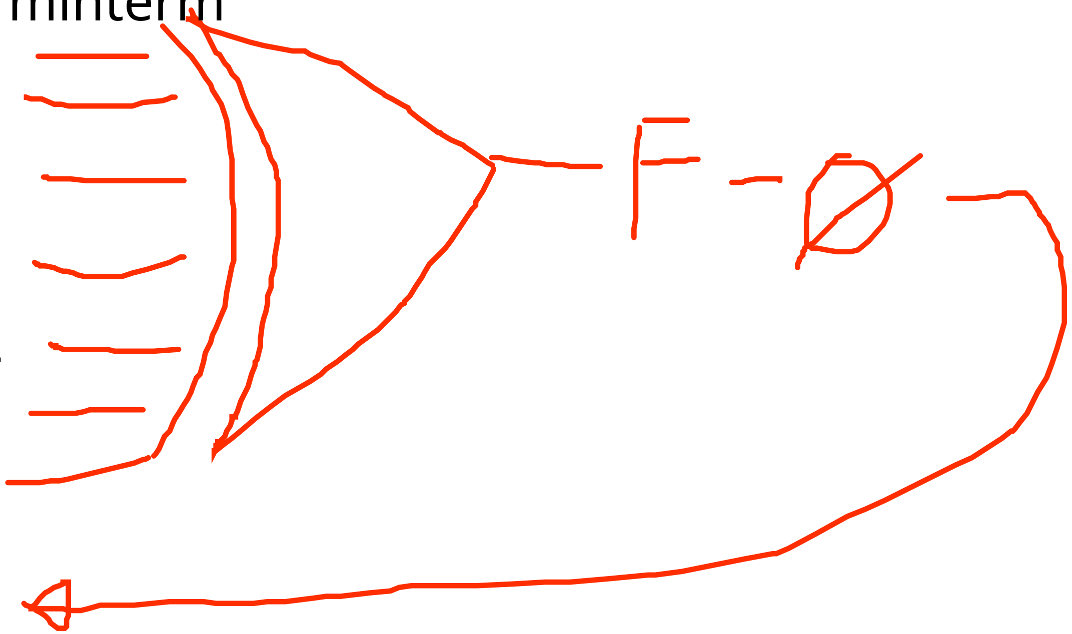
$$
\begin{cases}
X_0 = 1 \\
X_1 = 0 + 1 = 1, \quad c = 0 \\
X_2 = 1 + 0 + 0 = 1, \quad c = 0 \\
X_3 = 1 + 0 = 1, \quad c = 0 \\
X_4 = 0
\end{cases}
$$

$$
\begin{cases}
P_0 = X_0 \\
P_1 = X_1 \\
P_2 = X_2 + A_0B_2 \\
P_3 = X_3 + A_1B_2 + \text{carry from } P_2 \\
P_4 = X_4 + A_2B_2 + \text{carry from } P_3 \\
P_5 = \text{carry from } P_4
\end{cases}
$$

$$
\begin{cases}
P_0 = X_0 = 1 \\
P_1 = X_1 = 1 \\
P_2 = 1 + 1 = 0, \quad c = 1 \\
P_3 = 1 + 0 + 1 = 0, \quad c = 1 \\
P_4 = 0 + 1 + 1 = 0, \quad c = 1 \\
P_5 = 1
\end{cases}
$$

- Design a combinational circuits for parity generator/checker

binary	minterm
1	1
1	2
	3
1	4
1	5
	6
0	7



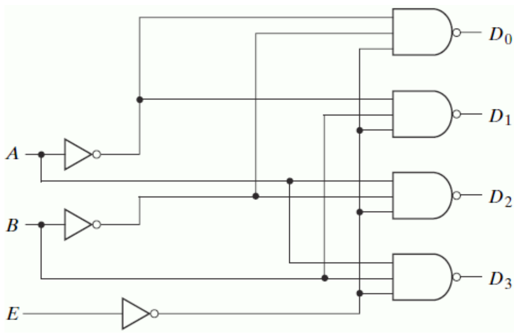
xor truth table

odd number of 1s
= true output

4.27 A combinational circuit is specified by the following three Boolean functions:

$$F_1(A, B, C) = \Sigma\,(1, 4, 6),\ F_2(A, B, C) = \Sigma\,(3, 5),\ F_3(A, B, C) = \Sigma\,(2, 4, 6, 7)$$

Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decode. Minimize the number of inputs in the external gates.



E	A	B	D0	D1	D2	D3
1	X	X	X	X	X	X
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0