ECE 124: Homework 7
Spring 2023

Assigned: Friday, May 12th
Due: Friday, May 19th
Late submission Due: Saturday, May 20th

Show your work! (No credit even for correct answers without justification.)

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1) Combinational circuit (50 points)

Implement a 4-bit magnitude comparator using Verilog and verify its functionality using a testbench. Include the code for the design and the testbench.

This circuit takes in two 4-bit inputs, 'a' and 'b', and produces three 1-bit outputs: 'eq', 'gt', and 'lt'. When both inputs are equal, the 'eq' output is set high and the other two outputs are low. If 'a' is greater than 'b', then the 'gt' output is set high and the other two outputs are low. Similarly, if 'a' is less than 'b', then the 'lt' output is set high and the other two outputs are low.

2) Sequential circuit (50 points)

Design a 4-bit shift register with a left shift functionality in verilog. Write a test bench to verify the circuit's functionality for at least four cycles.

In this case, you are asked to design a 4-bit shift register with left shift functionality, which means that the input bits are shifted to the left and a new input bit is inserted in the rightmost bit position.

To design the shift register in Verilog, you can use a reg data type to represent the input, and an output reg data type to represent the shifted output. You will also need to use an always block to describe the behavior of the circuit on the rising edge of the clock signal. The block should include a conditional statement that specifies the behavior of the circuit based on the input and control signals.