ECE124: Discussion

Discussion #8

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3.21 Draw (a) the multiple-level NAND circuit for the following expression and (b) repeat (a) for a NOR circuit.

w(x + y + z) + xyz

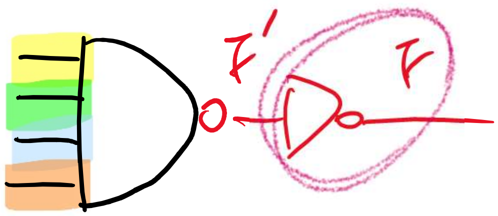
$F = (A \cdot B)'$

$$F(w,x,y,z) = w(x+y+z) + xyz$$

$$F' = \{w(x+y+z) + xyz\}'$$

① $\{wx + wy + wz + xyz\}'$

$$F' = (wx)' \cdot (wy)' \cdot (wz)' \cdot (xyz)'$$



$$(F')' = \{(wx)' \cdot (wy)' \cdot (wz)' \cdot (xyz)'\}'$$

② $F' = \{w \cdot (x' \cdot y' \cdot z')' + xyz\}'$

$$= \{w \cdot (x' \cdot y' \cdot z')'\}' \cdot (xyz)'$$

$$(F')' = [\{w \cdot (x' \cdot y' \cdot z')'\}' \cdot (xyz)']'$$

3.21 (b) repeat (a) for a NOR circuit.

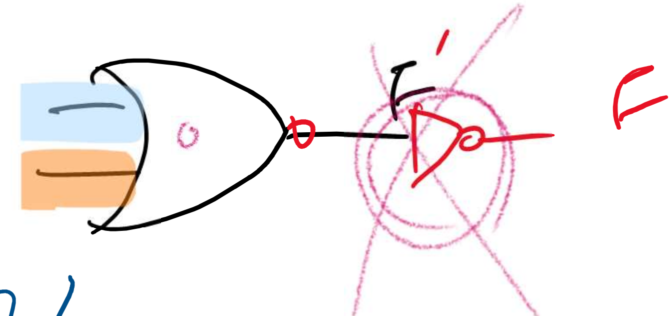
$F = (A+B)'$

w(x + y + z) + xyz

$$F' = \{ w(x+y+z) + xyz \}'$$

$$= \{ w(x+y+z) \}' \cdot (xyz)'$$

$$F = (F')' = \left[\{ w' + (x+y+z)' \} \cdot (x'+y'+z') \right]'$$



$$F = \left\{ \left[\{ w' + (x+y+z)' \}' + (x'+y'+z')' \right]' \right\}'$$

3.26 With the use of maps, find the simplest sum-of-products form of the function F = *fg*, where

f = abc′ + c′d + a′cd′ + b′cd′ *g* = (a + b + c′ + d′)(b′ + c′ + d)(a′ + c + d′)

$a' + b + c + d'$

1 0 0 1

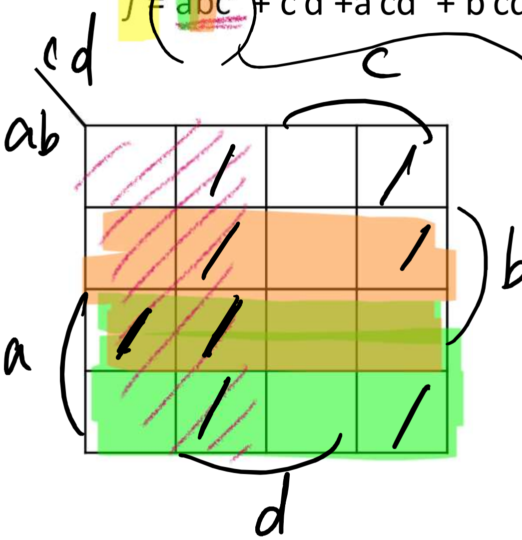
1 1 0 1

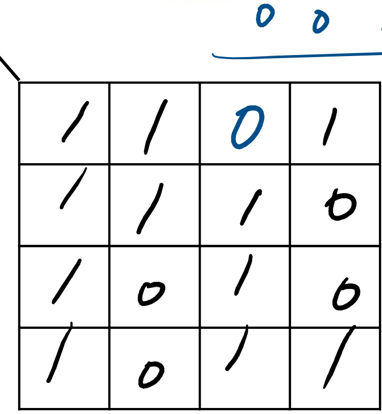
abc′d

1 1 0 0

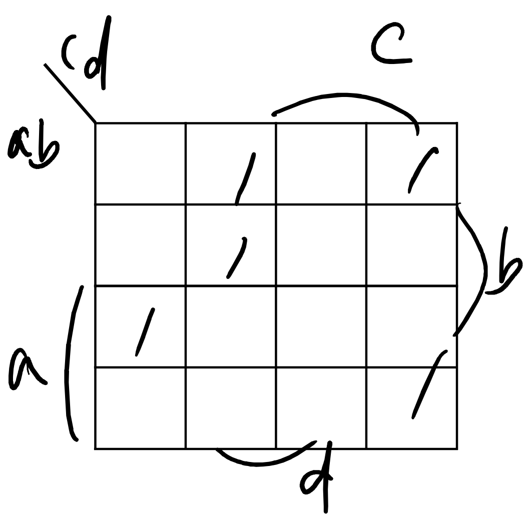
1 1 0 1

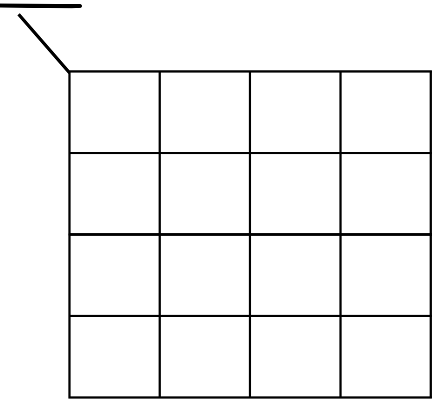
0 0 1 1 = M_3





G = f + g





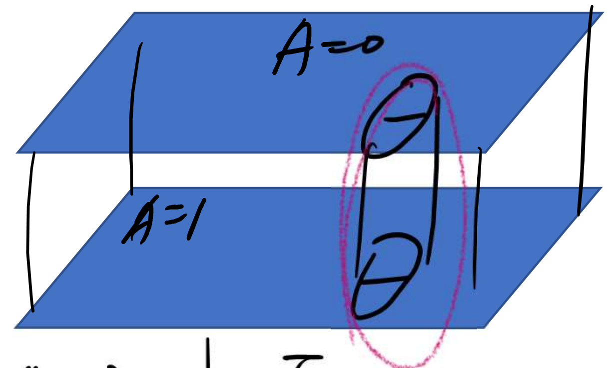
- 5 variables K-map: F(A, B, C, D, E) = Σ(4, 5, 6, 7, 9, 11, 13, 15, 16, 18, 27, 28, 31)

A = 0

BC \ DE				
	1	1	1	1
		1	1	
		1	1	

A = 1

BC \ DE				
	1			1
	1		1	
			1	

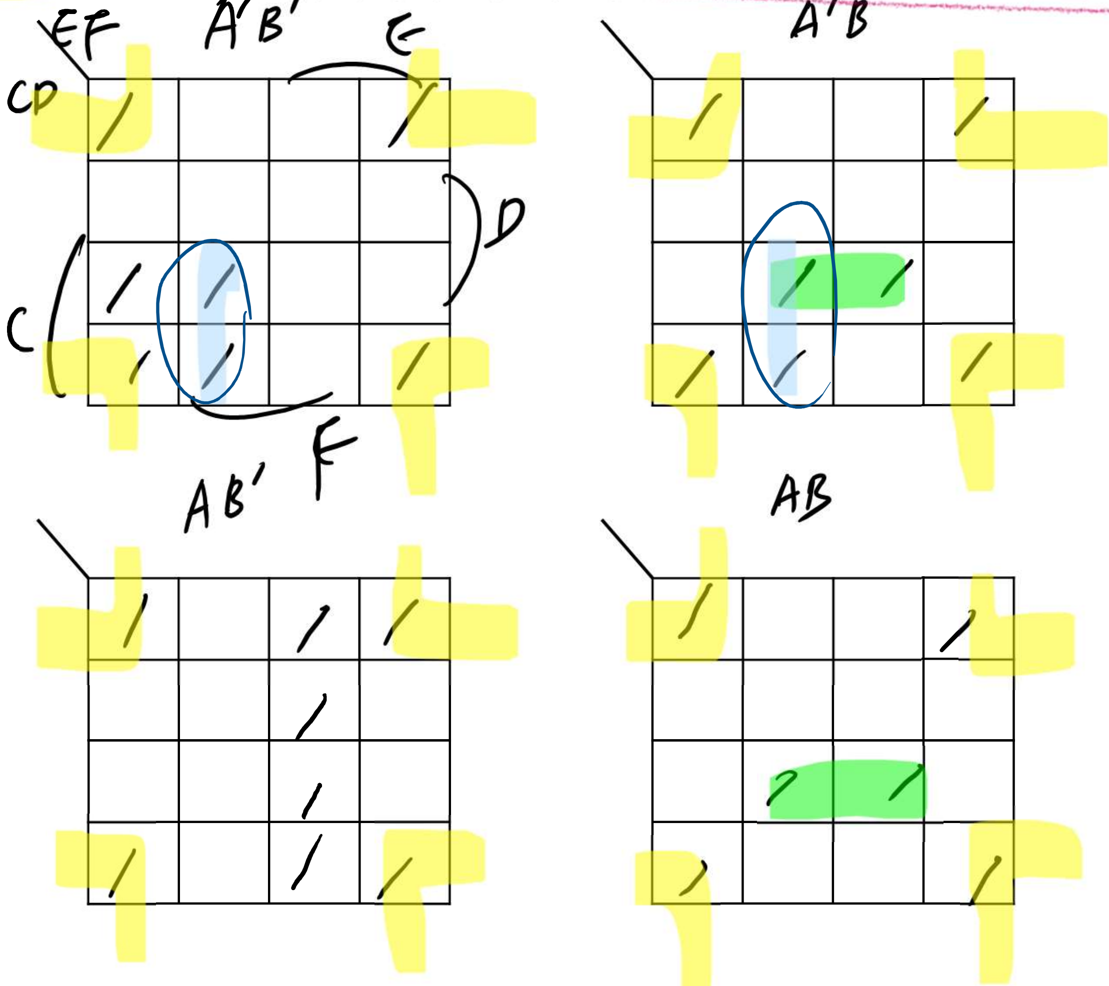


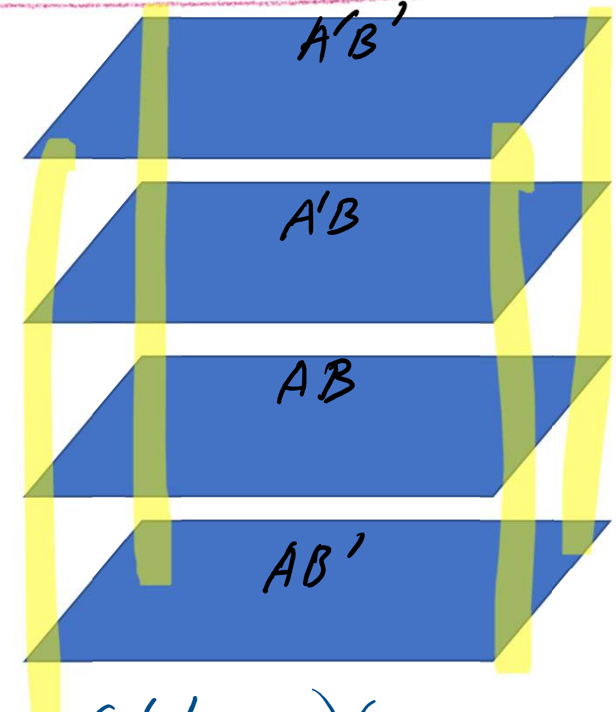
cf

x	y	z	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

- 6 variables K-map:

F(A, B, C, D, E, F) = Σ(0, 2, 8, 9, 10, 12, 13, 16, 18, 24, 25, 26, 29, 31, 32, 34, 35, 39, 40, 42, 43, 47, 48, 50, 56, 58, 61, 63)





$0 : (A'B' + A'B)(\quad)$

$A' \cdot (C \cdot E'F)$

4.13 The adder-substractor circuit of Fig. 4.13 has the following values for mode input M and data inputs A and B. In each case, determine the values of the four SUM outputs, the carry C, and overflow V.

	M	A	B
(a)	0	0111	0110
(b)	1	1000	1001

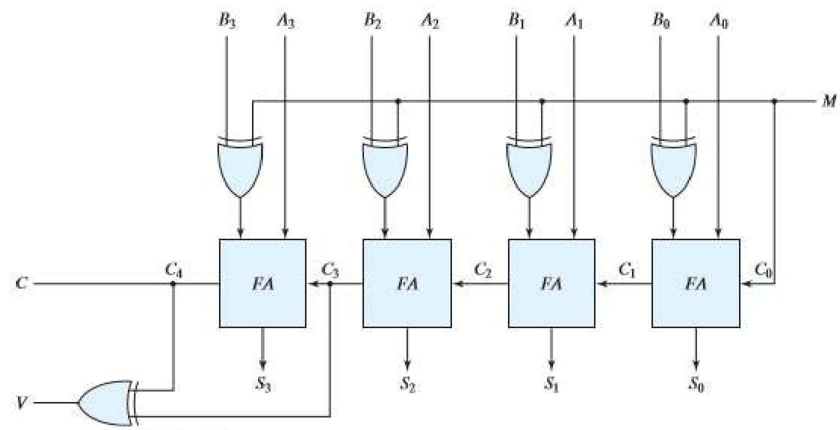


FIGURE 4.13
Four-bit adder–subtractor (with overflow detection)

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	M	A	B
(a)	0	0111	0110
			1011(?)
			0101

$-8 <$ 4-bit signed # $< +7$

$7 + (-5) = +2$

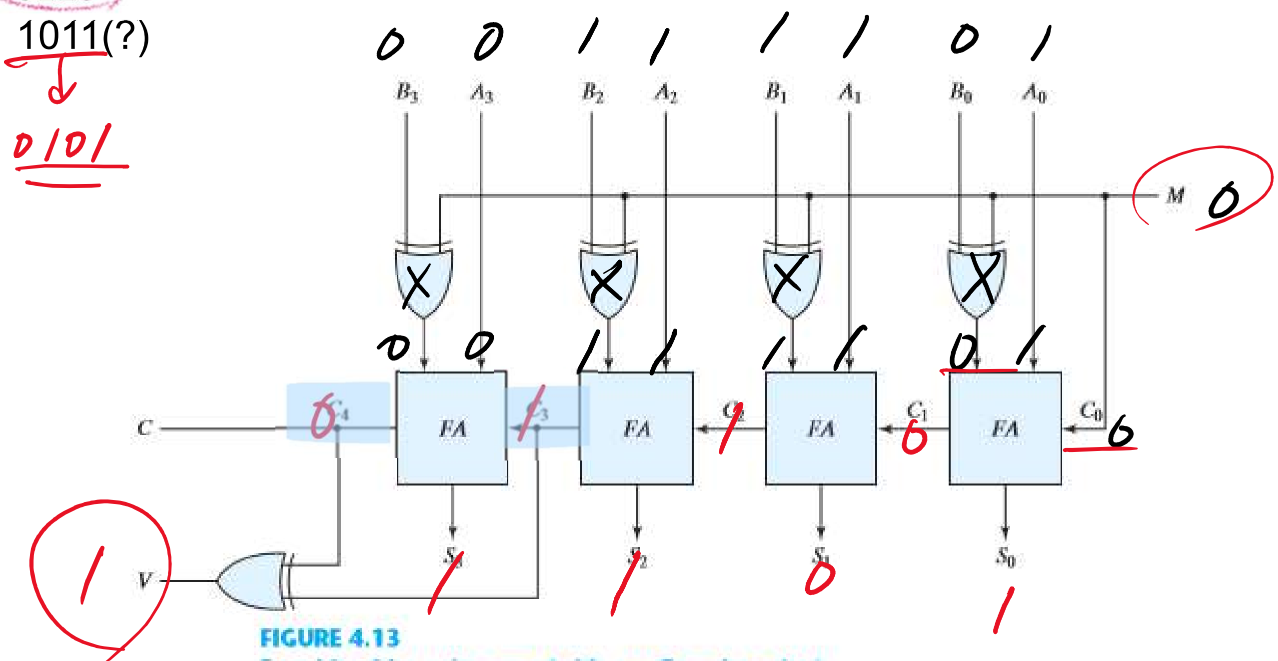

FIGURE 4.13
Four-bit adder–subtractor (with overflow detection)

4.13 The adder-substractor circuit of Fig. 4.13 has the following values for mode input M and data inputs A and B. determine the values of the four SUM outputs, the carry C, and overflow V.

	M	A	B
(b)	1	1000	1001

A ← −8

$(A) - (B)$

$(-A) - (-B)$

$\Rightarrow (-A) + (-(-B))$

1000 ↓ 2's 1000

1001 ↓ 2's 0111

$(-8) - (-7)$

$\Rightarrow (-8) + (\text{2's CR of } (-7))$

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

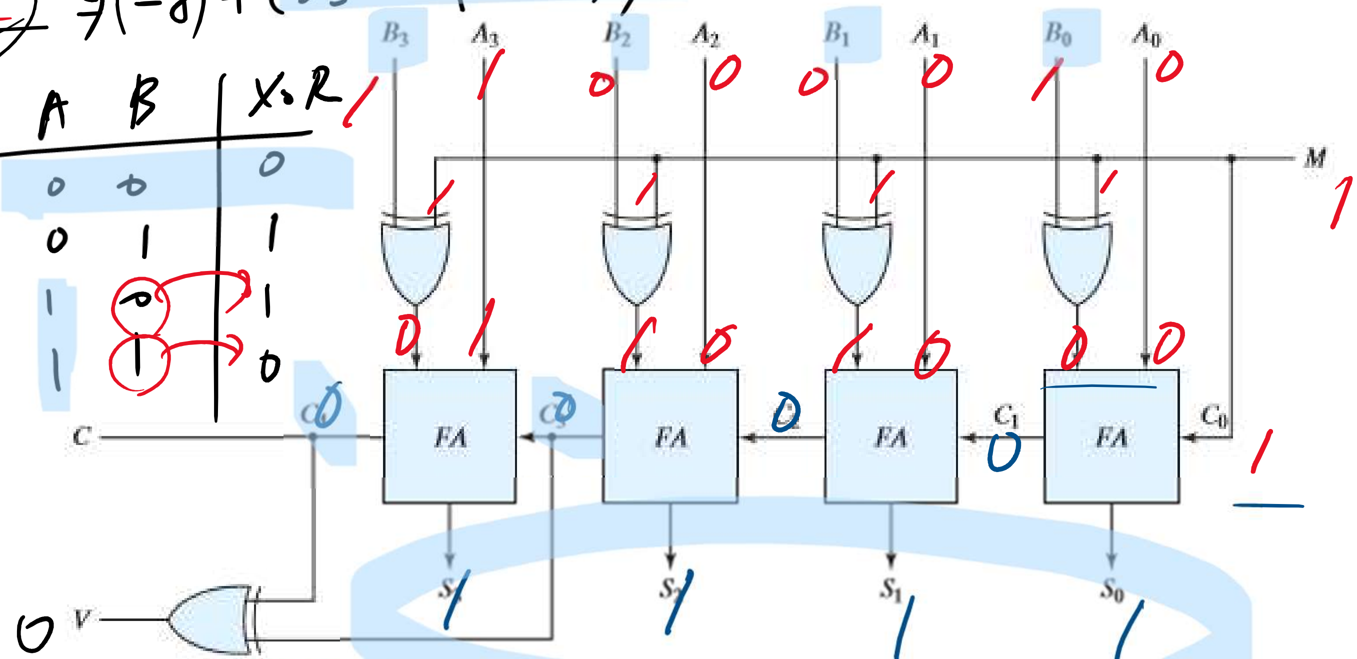

FIGURE 4.13
Four-bit adder–subtractor (with overflow detection)