ECE124: Discussion

Discussion #12

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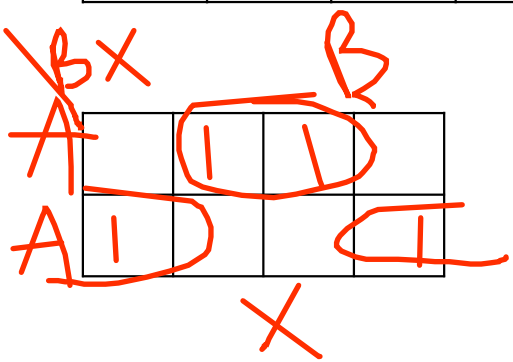
5.16 Design a sequential circuit with two D flip-flops A and B, and on input x_in.

(b) When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeat.

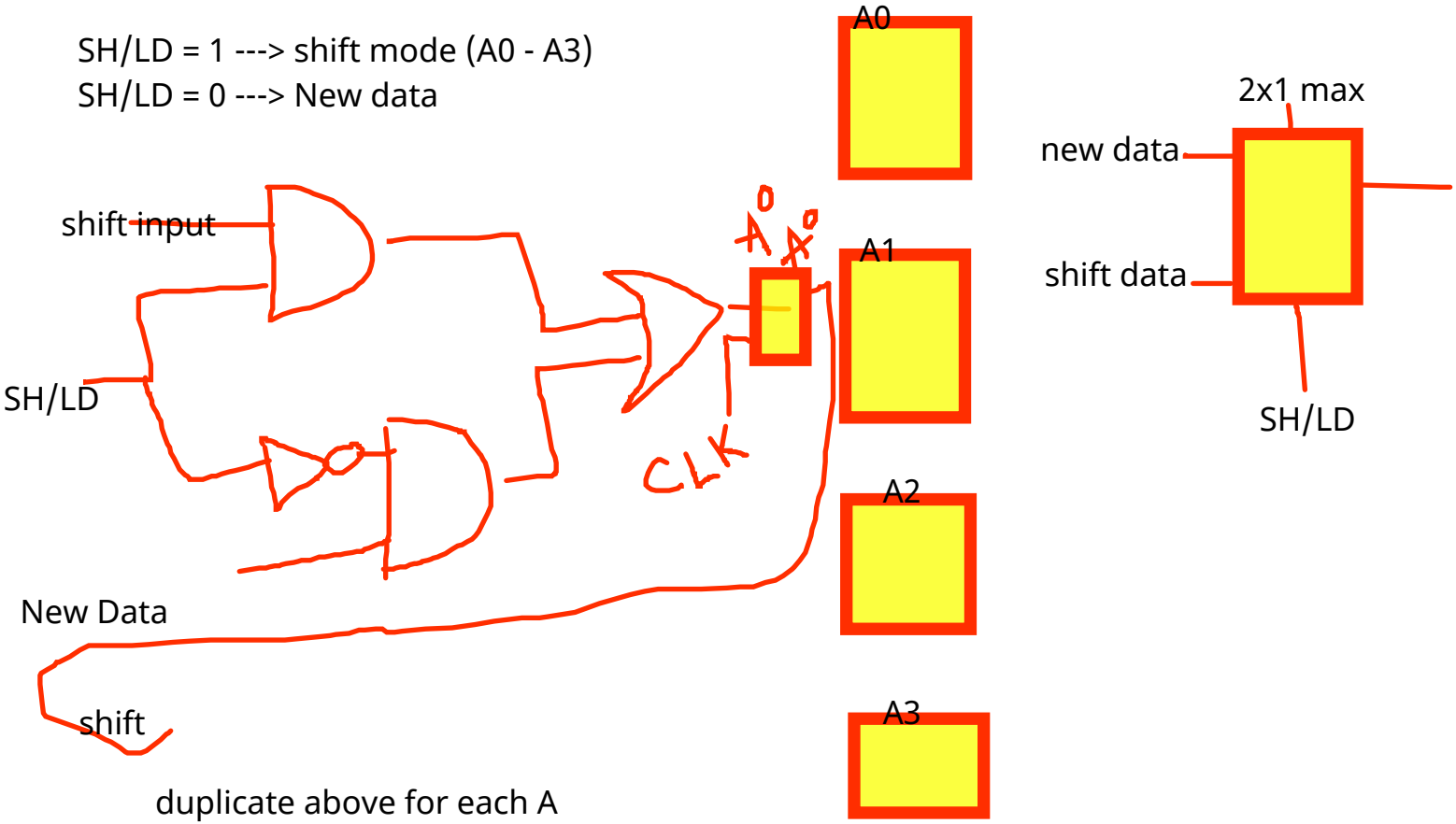
Current State		Input	Next State	
A	B	x	A	B
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1



A(t+1) = A'X+AX'

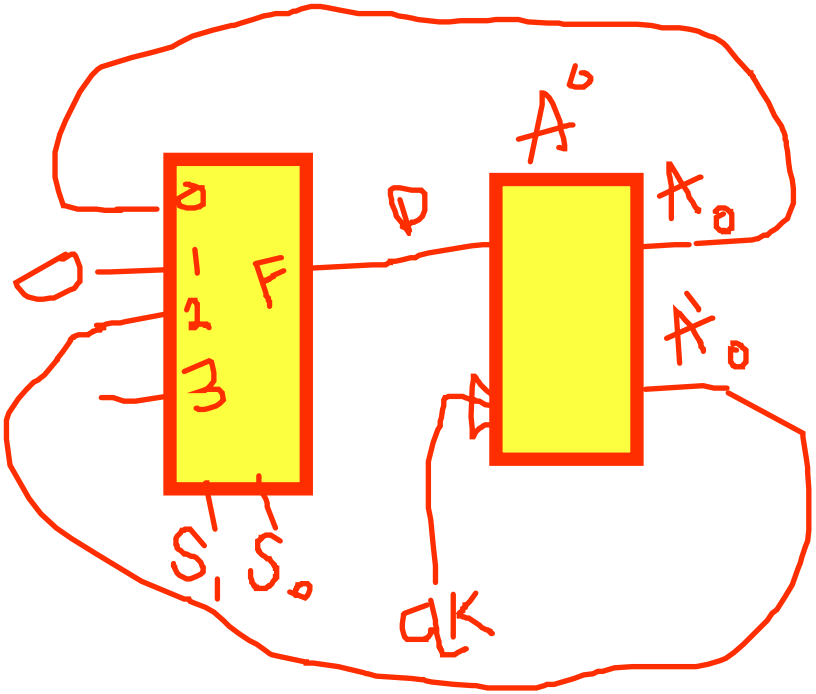
B(t+1) = AB + A'B'X+ABX

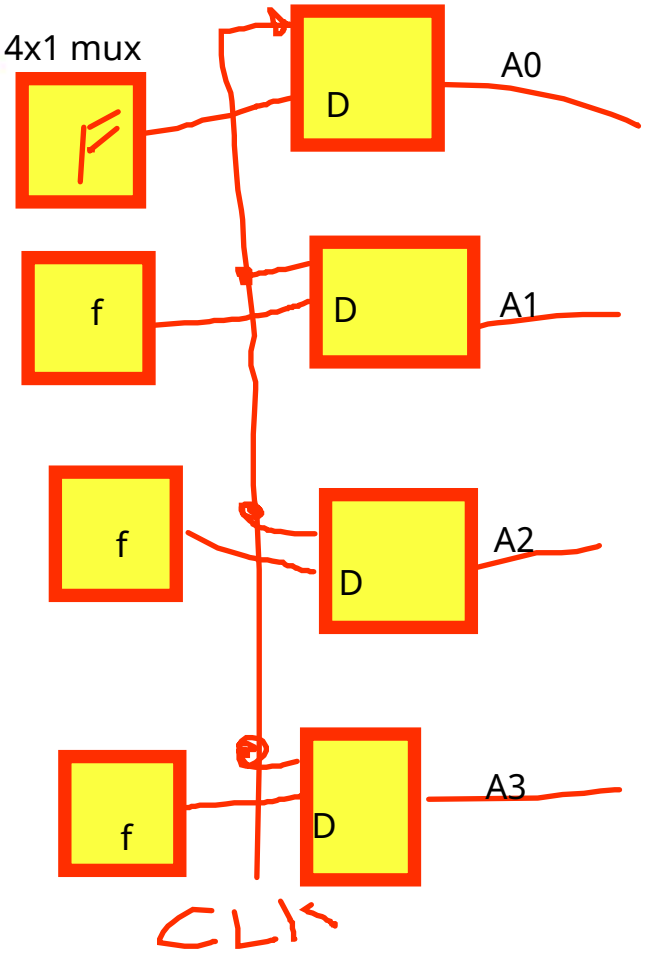
Modified 6.6 Design a four-bit shift register with parallel load using D flip-flops. There is one control input: shift/Load ($SH/\overline{LD}$). When $SH/\overline{LD}$ = 1, the content of the register is shifted toward A_3 by one position. New data are transferred into the register when $SH/\overline{LD}$ = 0.



6.7 Draw the logic diagram of a four-bit register with four D flip-flops and four 4 × 1 multiplexers with mode selection inputs s_1 and s_0. The register operates according to the following function table.

s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data





6.8 The serial adder of Fig. 6.6 uses two four-bit registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop is initially reset to 0. List the binary values in register A and the carry flip-flop after each shift.

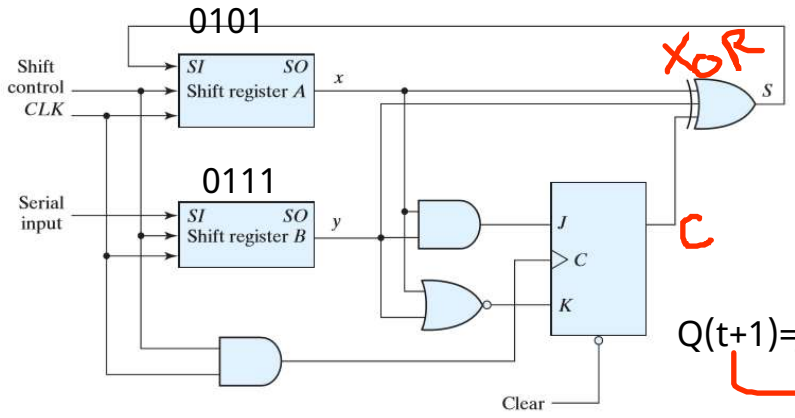


FIGURE 6.6
Second form of serial adder

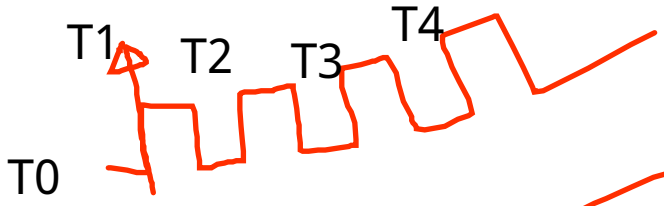
S = X⊕Y⊕C

C(t+1) = (XY)C'+(X+Y)C

XYC'+XC+YC

XYC'+XY'C+XYC+X'YC

XY+C(XY'+X'Y)



Q(t+1)=JQ'+K'Q

Q(t) J K

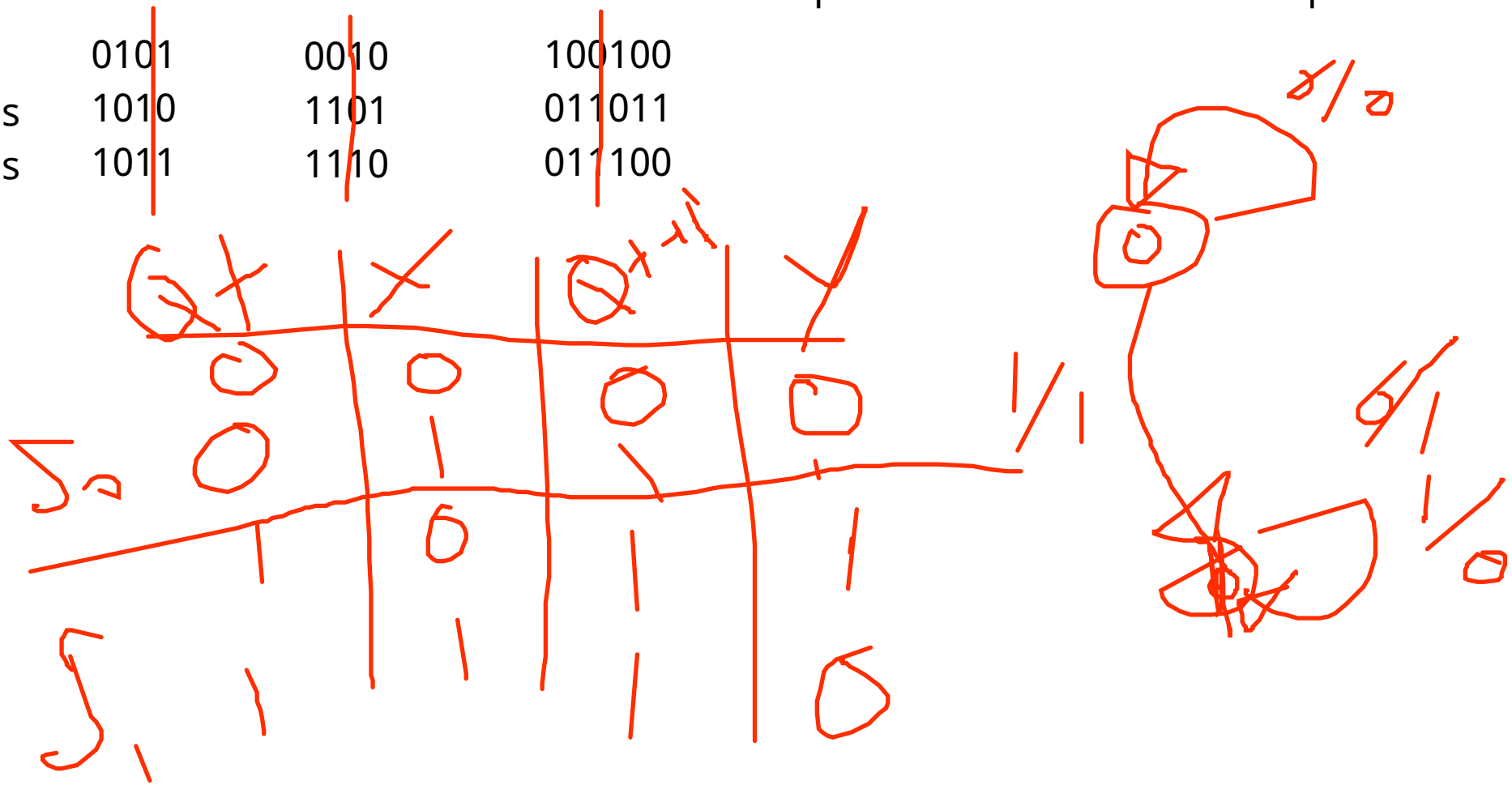
	Reg A	Reg B	X	Y	J	K	S	C
T0	0101	0111	X	X	X	X	X	
T1	0010	X011	1	1	1			1
T2	0001	XX01						
T3	1000	XXX0						
T4	1100	XXXX						

6.10 Design a serial 2's complementer with a shift register and a D flip-flop. The binary number is shifted out from one side and its 2's complement shifted into the other side of the shift register.

- Using the characteristic of 2's complement

pick the first 1 in the bit sequence

	0101	0010	100100
1s	1010	1101	011011
2s	1011	1110	011100



6.10 Design a serial 2's complementer with a shift register and a D flip-flop. The binary number is shifted out from one side and its 2's complement shifted into the other side of the shift register.

- Using the characteristic of 2's complement

$Q(t+1) = Q(t) + x$

$y = Q(t) \oplus x$

6.17 Design a four-bit binary synchronous counter with D flip-flops.

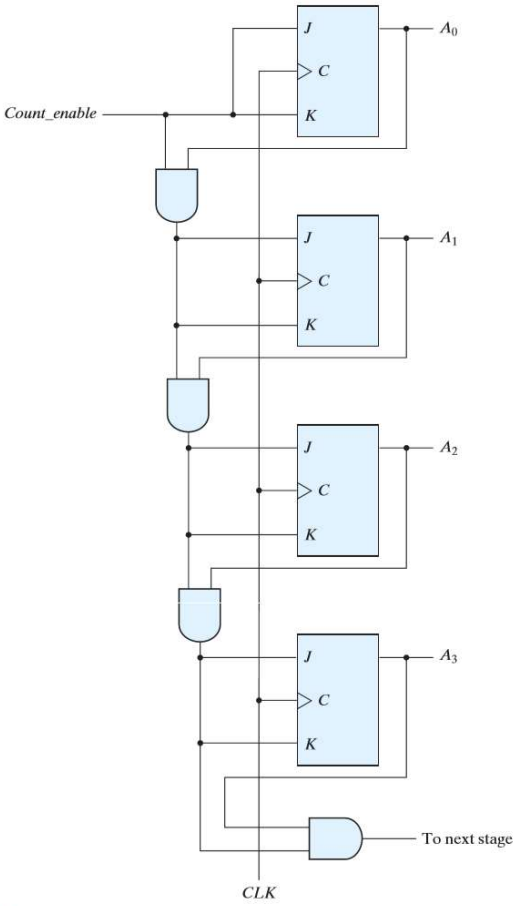


FIGURE 6.12
Four-bit synchronous binary counter

T0 = E
T1 = A0E
T2 = A1A0E
T3 = A2A1A0E

t0(t+1) = A0 XOR E
t1(t+1) = A1 XOR A0E
t2(t+1) = A2 XOR A1A0E
t3(t+1) = A3 XOR A2A1A0E

ABCD	ABCD
0000	0001
0001	0010
...	...

*Up-Down Counter Using T flip-flops, design a 2-bit up-down counter with external input x to determine whether Up or Down.

Present state		Input	Next state		FF inputs	
B	A	x	B(t+1)	A(t+1)	T_B	T_A
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1