ECE 331 – Fall 2024
Homework 5
Assigned Friday, October 18th
Due Friday, October 25th

1. (20 points) The following sequence of instruction is executed in a basic five-stage pipelined processor discussed in the class. There is NO forwarding support.

```
ldur     x2,[x1,#0]
add      x3,x3,x2
add      x4,x1,x3
sub      x1,x4,x1
cbz      x1, exit
stur     x3,[x1,#0]
ldur     x5,[x1,#8]
sub      x2,x5,x6
add      x6,x2,x3
exit:
         add x1,x2,x3
```

(a) List all hazards in the above code. For each hazard, indicate the instruction which creates the hazard and all affected instructions.

(b) Rewrite the code including minimum number of nop instructions to eliminate potential hazards. You can reorder the instructions. Assume that the pipeline has full forwarding support. Also, assume that register read and write at the same address can happen in one clock cycle.

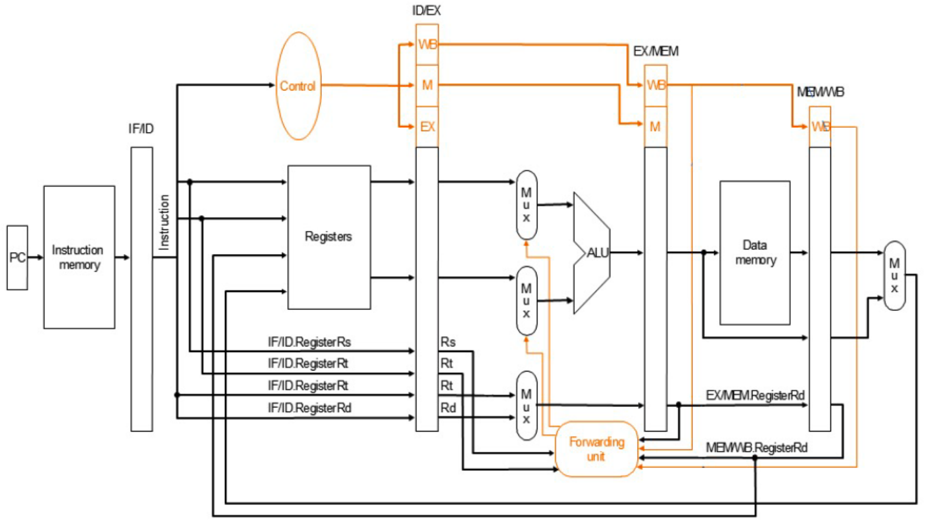
(c) Could branch prediction help eliminate the hazards in the code for this question? Please explain why or why not in one or two sentences.

2. (20 points) Consider execution of the following sequence of instructions in a pipelined Arm processor with full forwarding support. Reorder the instructions to eliminate as many nop instructions as possible while maintaining correct code execution.

```
Ldur  x1[x19,#0]
ldur  x2,[x19,#8]
nop
nop
nop
nop
sub   x2,x2,x1
nop
nop
add   x4,x2,x1
ldur  x4,[x0,#8]
nop
nop
nop
nop
add   x5,x4,x1
```

3. (30 points) Consider the following Arm code. Assume that the instructions cannot be reordered. Add all necessary forwarding circuitry and wires to the following figure to avoid the hazard(s) created by the following code – only add circuitry necessary to avoid the hazard(s).

```
ldur     x20,[x19,#0]
add      x2,x2,x21
sub      x3,x20,x4
```



* special note: questions about the homework should use the Piazza forum (preferred):
piazza.com/umass/spring2024/ece331/home