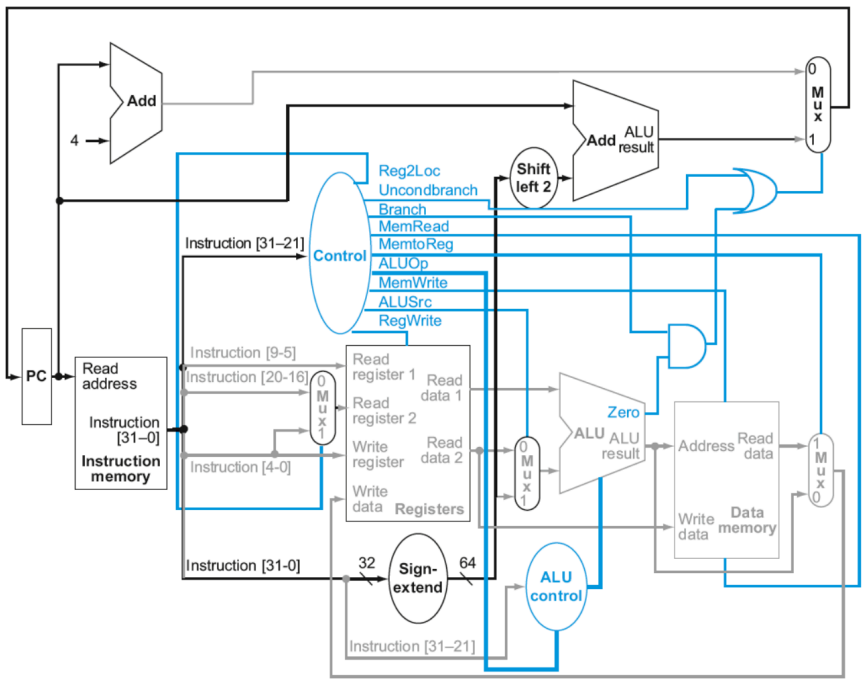
ECE331 Homework 4

ECE 331 – Fall 2025
Homework 4
Assigned Friday, October 11
Due Friday, October 18

1. (50 pts) Use the Arm control datapath diagram below to solve the problems that follow:



(a) Fill out the values of the control signals for each instruction with either a 1, 0, or X (to indicate don't care). The 'ALUOp' control signal consists of two bits.

Instr.	Reg2Loc	Unc.b	Branch	MemRead	MemtoReg	ALUOp[1:0]	MemWrite	ALUSrc	RegWrite
add									
b									
cbz									
stur									

(30 pts) Do Zybooks 4.17.7: [20] <COD §4.4> in chapter 4.17, but with the following latencies:

Instruction Memory	Add	Mux	Alu	Registers	Data Memory
250 ps	90 ps	45 ps	110 ps	130 ps	250 ps

Sign Extend	Shift Left2	single gate	control	register file
26 ps	25 ps	5 ps	50 ps	150 ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

1. Although the control unit as a whole requires 50 ps, it so happens that we can extract the correct value of the `Reg2Loc` control wire directly from the instruction. Thus, the value of this control wire is available at the same time as the instruction. Explain how we can extract this value directly from the instruction. Hints: Carefully examine the opcodes shown in COD Figure 2.20 (LEGv8 instruction encoding). Also, remember that `LSR` and `LSL` do not use the Rm field. Finally, ignore `STXR`.
    1. to extract the value of the Reg2Loc wire we can look in the instruction, the way we do this is to look in the type of the instruction, in R type instructions: the second source register is in the rm field of the command, meanwhile commands like LSR dont need to use the Reg2Loc wire allowing us to extract the command directly without consulting the control
2. What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?
    1. intruction memory : 250 ps
    2. register read: 130 ps
    3. ALU: 110 ps
    4. register write: 130 ps
    5. summing all of these we get 620 ps
3. What is the latency of `LDUR`? (Check your answer carefully. Many students place extra muxes on the critical path.)

    1. instruction memory: 250 ps
    2. register read: 130 ps
    3. Sign Extend: 26 ps
    4. ALU: 110 ps
    5. Data Memory: 250 ps
    6. register write: 130 ps
    7. summing all of these we get 896 ps
4. What is the latency of `STUR`? (Check your answer carefully. Many students place extra muxes on the critical path.)
    1. instruction memory: 250 ps
    2. register read: 130 ps
    3. Sign extend: 26 ps
    4. ALU: 110 ps
    5. Data Memory: 250
    6. summing all of these we get 516 ps
5. What is the latency of `CBZ`?
    1. Instruction Memory: 250 ps
    2. Register read: 130 ps
    3. ALU: 110 ps
    4. Adder: 90 ps
    5. summing all of these we get 580 ps
6. What is the latency of `B`?
    1. instruction memory: 250 ps
    2. adder: 90 ps
    3. adding these up we get 340 ps
7. What is the latency of an I-type instruction?
    1. instruction memory: 250 ps
    2. register read: 130 ps
    3. sign extend: 26 ps
    4. ALU: 110 ps
    5. register: 130 ps
    6. adding these up we get 646 ps
8. What is the minimum clock period for this CPU?
    1. highest ps is 896 with LDUR so that is the minimum clock period