ECE 124: Homework 6
Spring 2023

Assigned: Friday, May 5th at midnight
Due: Friday, May 12th at midnight
Late Submission Due: Saturday, May 13th at midnight

Show your work! (No credit even for correct answers without justification.)

Problems from the textbook (Digital Design 6th Ed., M. Mano and M. Ciletti)

1) 5.3 (20 points)

Show that the characteristic equation for the complement output of a JK flip-flop is

$$Q'(t+1) = J'Q' + KQ$$

2) 5.7 (20 points)

A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. P5.7. Derive the state table and state diagram of the sequential circuit.

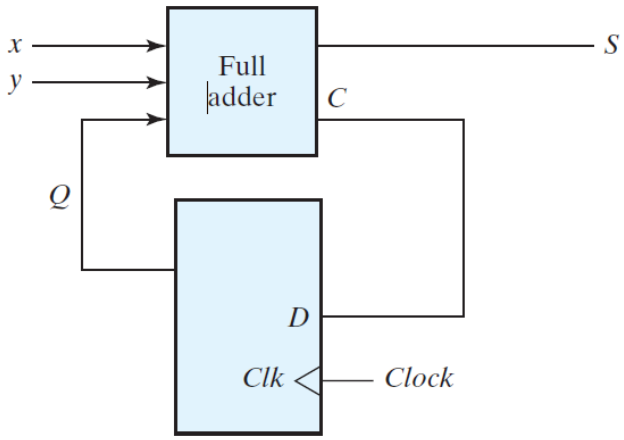

FIGURE P5.7

3) 5.9 (20 points)

A sequential circuit has two JK flip-flops A and B, one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x\,K_A = B, \qquad J_B = x\,K_B = A'$$

(a) **Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.**
(b) **Draw the state diagram of the circuit.**

4) 6.6 (20 points)

Design a four-bit shift register with parallel load using D flip-flops. There is two control inputs: shift and load. When shift = 1, the content of the register is shifted toward A3 by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change.

5) 6.17 (20 points)

Design a four-bit binary synchronous counter with D flip-flops.