UMass ECE 210 – Fall 2023

Lab 11: MOSFET SCS

Concepts:

- MOSFET IV Curves
- Saturation mode vs. Triode/Linear/Ohmic operation

DATA required for Lab report:

PLOT – NMOS current vs. Gate voltage
PLOT – NMOS current vs. Drain voltage
PLOT – PMOS current vs. Gate voltage

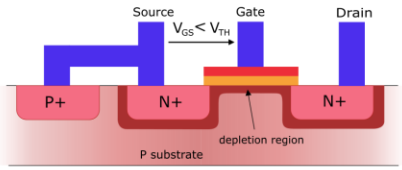
Metal Oxide Semiconductor (MOS) Field Effect Transistors (FETs) form the basis for all complex logical functions in digital electronics. There are two types for each polarity of charge carriers, NMOS (for electrons) and PMOS (for holes).

MOSFET operation is summarized below in three regimes (NMOS shown):

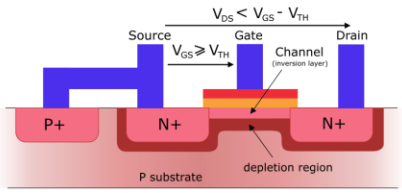
1. **Cut off** – No bias applied and/or gate closed hard (no current flow)
2. **Triode** (Linear\Ohmic regime) – Small bias applied with the gate open (bias controls current)
3. **Saturation** – Large Bias applied with gate open (gate controls current)

No Bias Voltage
➔No flow

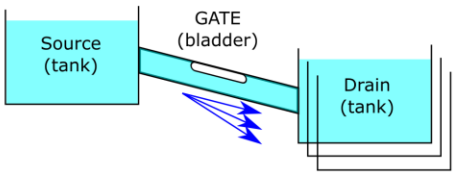
Gate closed
➔No flow



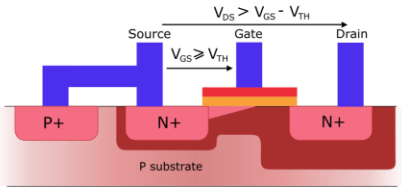
Small Bias Voltage
Gate open
➔Bias controls flow



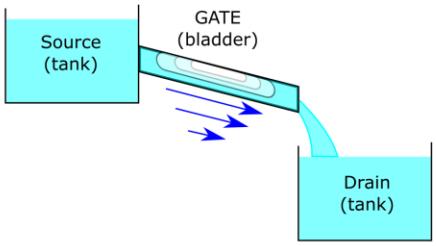
Triode/Linear operating region (ohmic mode)



Large Bias Voltage
Gate open
➔Gate controls flow



Saturation mode

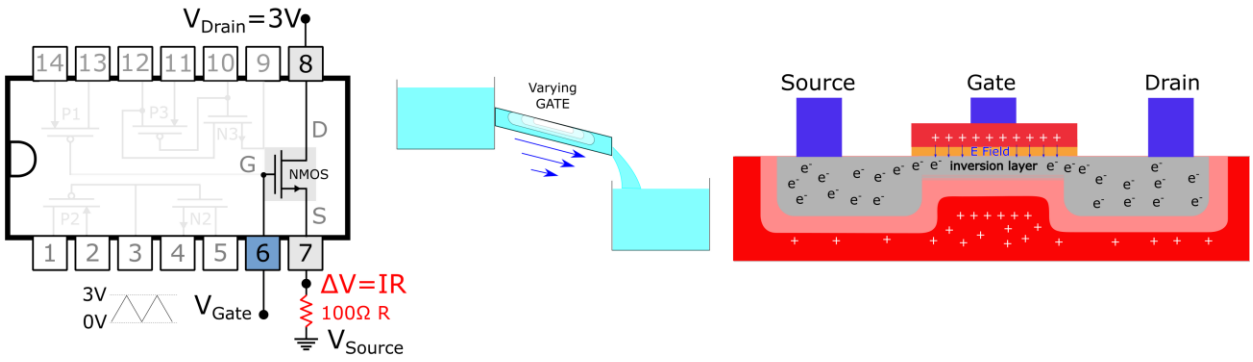


Measuring Gate Voltage Threshold (V_{TN}):

To verify the gate voltage threshold at which the NMOS starts conducting we will measure the current through the entire circuit using a small resistor like before.

We'll see that the gate doesn't open immediately. The gate requires charge to build up before the electric field is strong enough to create an inversion layer within the depletion region. Almost like a capacitor that has some charge in it already that must be canceled before it charges and creates an electric field between its parallel plates *(hence, 'Field Effect' transistor in MOSFET).*

Then continued charging of the gate increases the electric field and increases the depth of the inversion layer in the substrate allowing more current to flow between source and drain.



Assemble the NMOS device:

1. Insert a CD4007 into your breadboard
2. Supply 3V to V_{Drain} (pin 8)

3. Insert a small resistor between V_{Source} (pin 7) and ground

4. Send in a triangle wave to the gate input V_{Gate} (pin 6)
   (Min=0V, Max=3V, freq.=1kHz)

5. Monitor the input wave on oscilloscope Ch1
6. Measure the output (pin 7) on oscilloscope Ch2

7. Change your oscilloscope from YT mode to XY mode by pressing:
   HORIZONTAL>MENU>TIME BASE> XY

8. RECORD your PLOT and RECORD the CSV for your lab report

9. Estimate and RECORD the gate voltage threshold (V_{TN})

Measuring the Conductance Coefficient Parameter (K) :

The conductance of the transistor vs. gate voltage defines how much current the transistor drives under an applied voltage. We can see from our measurements that the drive current depends on the applied gate voltage **quadratically** (once it is above threshold).

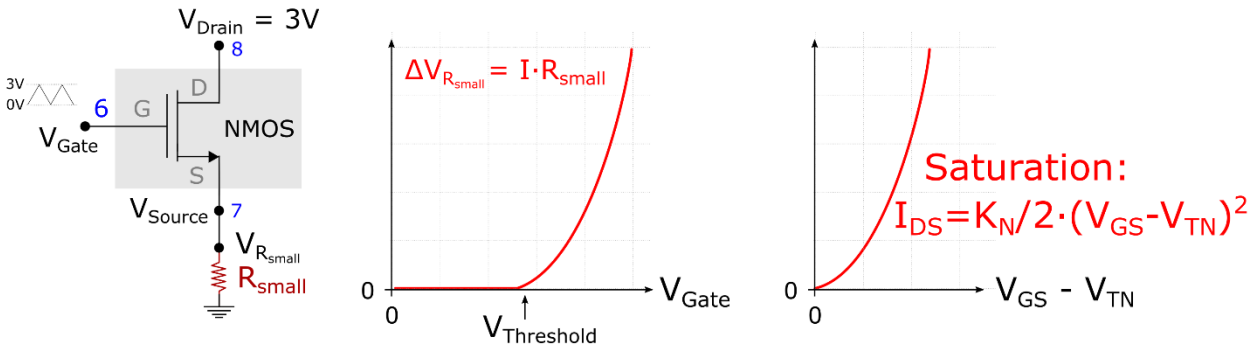
If we can measure the coefficient of conductance parameter (K) then we can model the transistor.

As we will see in the next section, we are in the SATURATION regime, so the drive current is:

$$I_{DS} = \frac{K_N}{2} \cdot (V_{GS} - V_{TN})^2$$

Roughly estimate and RECORD the conductance coefficient parameter (K) by taking the maximum current and the maximum gate voltage and solving the above equation for K.

What units do you expect?



For your Lab report:

1. Plot the CSV of your measured drive current vs. gate voltage
2. Fit your data to precisely determine the conductance parameter (K)

   (Bonus: Fit your data to precisely determine the voltage threshold!)

Triode vs. Saturation:

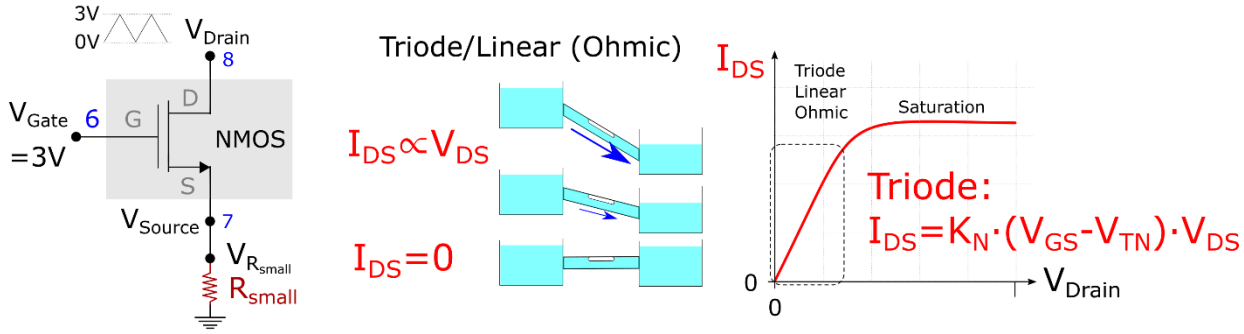
We were just operating the transistor in Saturation mode.
The drain voltage was fixed, we varied the gate voltage and as the gate opened, current flowed.

Next, we'll lower the drain voltage which biases the transistor while keeping the gate voltage fixed. At zero applied bias voltage between the drain and source there is no current.
As the relative potential between the drain and source is increased, current starts to flow.

Triode (linear/ohmic) drive current:

$$I_{DS} = K_N \cdot (V_{GS} - V_{TN}) \cdot V_{DS}$$

As the drain voltage increases the current saturates and we're back in the saturation regime.



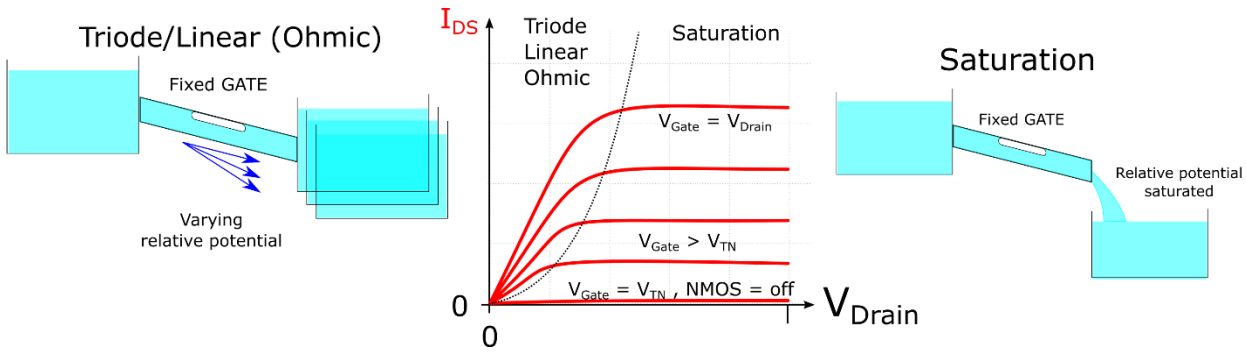
NMOS IV curve vs. V_{Drain}:

1. Turn off the power supply (so you can swap the gate and drain connections)
2. Move the triangle wave input from the gate (pin 6) to the drain (pin 8)
3. Move the power supply (3V) from the drain (pin 8) to the gate (pin 6)
4. Monitor the triangle wave input on oscilloscope Ch1
5. Measure the voltage drop across the small resistor (pin 7) on oscilloscope Ch2
6. RECORD the current vs Drain voltage
7. Reduce the triangle wave maximum until the IV curve is purely linear (TRIODE)
8. Roughly Estimate and RECORD the conductance coefficient (K_N) in the Triode regime.

   Does it agree with your estimate from the saturation regime?
9. Increase the triangle wave max voltage back to 3V for the next steps.

MOSFET IV Curves:

If we repeat these sweeps at different gate voltages, we can see that as the gate voltage decreases, the saturation current decreases.



Verify the gate voltage threshold at which no current flows and the IV curve is flat.

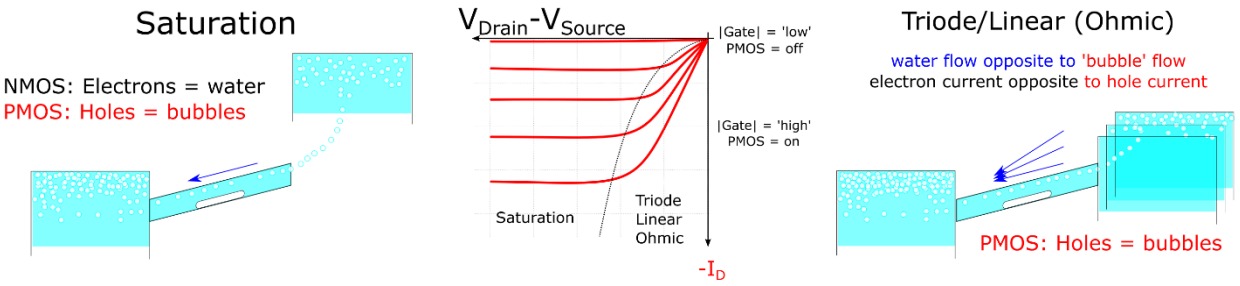
Measure and RECORD the saturation current at each gate voltage:

1. V_{Gate} = 3.0V (just measured)
2. V_{Gate} = 2.5V
3. V_{Gate} = 2.0V
4. $V_{Gate} = V_{TN}$ (just verified)
5. V_{Gate} = 1.0V
6. V_{Gate} = 0.0V

PMOS:

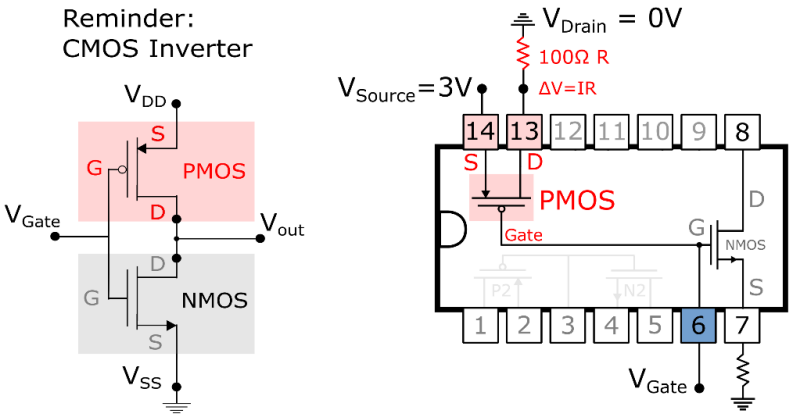
PMOS devices use the absence of electrons ('holes') within the semiconductor to drive current. Therefore, all of the voltages are relative to the high voltage (not ground anymore), because ground is the highest energy for holes and the high voltage is the lowest energy for holes (and therefore the 'source' of holes!)

Our definitions for gate voltage and drain voltage for NMOS technically also were relative to the source voltage, but for NMOS the source voltage is zero (ground) so we could ignore them.



To continue the water analogy, imagine 'holes' of water as bubbles.
(Arguably it should have been the reverse the 'hole' time)

Assemble the PMOS device:

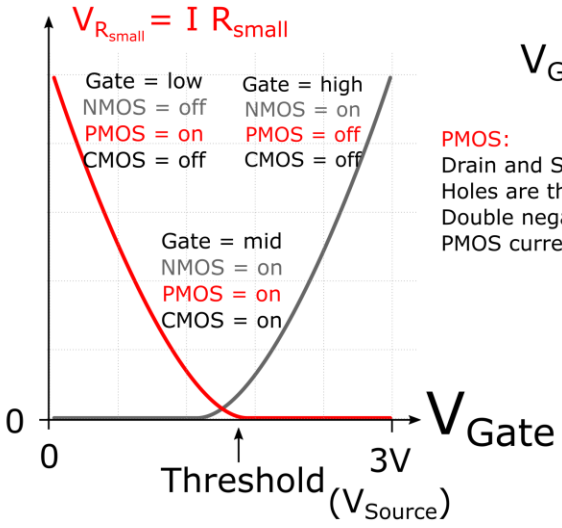


1. Move the power supply 3V to V_{Source} (pin 14)
2. Insert a new small resistor (100Ω) between V_{Drain} (pin 13) and ground (Keep pin 7 grounded through the small resistor)

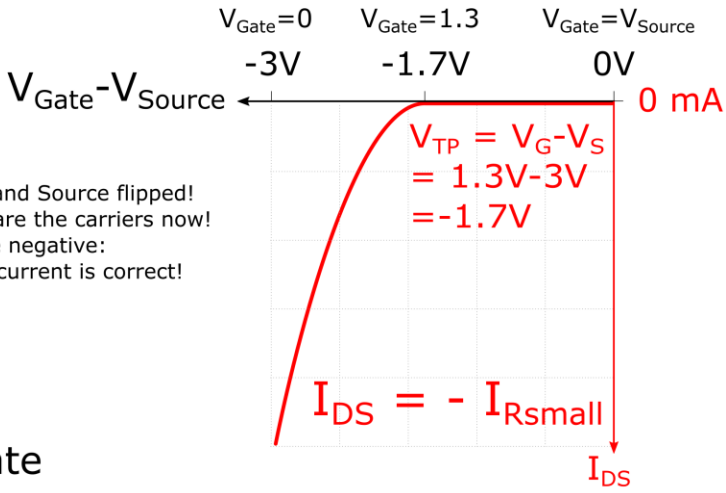
3. Continue sending in a triangle wave to the gate input V_{Gate} (pin 6) (Min=0V, Max=3V, freq.=1kHz)
4. Monitor the input wave on oscilloscope Ch1

5. Measure the output (pin 13) on oscilloscope Ch2
6. Change your oscilloscope from YT mode to XY mode.
7. RECORD your PLOT and save the CSV
8. For your lab report: Replot relative to the source voltage with the proper signs

9. Estimate and RECORD the gate voltage threshold (V_{TP}) (Remember it is relative to V_{Source} which is not zero!)



PMOS:
Drain and Source flipped!
Holes are the carriers now!
Double negative:
PMOS current is correct!



Lab Report 11 – Rubric

2,000-word limit 1 report/group

		Points	Grade
	Introduce and define concepts (with citations)	5	
	Motivation for experiment	5	
1	Experimental Diagram (drawing + PICTURE with labels)	5	
	PLOT – **NMOS IV curve vs. Gate voltage** (with input)	5	
	Analysis (remember to show your work for calculations)	5	
2	PLOT – **NMOS IV curves vs. Drain Voltage** (with input)	5	
	Analysis (remember to show your work for calculations)	5	
3	Experimental Diagram (drawing + PICTURE with labels)	5	
	PLOT – **PMOS IV curve vs. Gate voltage** (with input)	5	
	Analysis (remember to show your work for calculations)	5	
	Conclusion	5	
		55	