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Lab 11 Report

Introduce and define concepts (with citations)

NMOS- A MOSFET circuit (Metal Oxide Semiconductor Field Effect Transistors) that uses n-type semiconductor material for the channel between the source and drain terminals.
https://builtin.com/hardware/nmos-transistor

PMOS- PMOS is another type of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) that employs p-type semiconductor material for the channel.
https://builtin.com/hardware/nmos-transistor

Gate voltage - Gate voltage is the voltage applied to the gate terminal of a transistor, influencing the flow of charge carriers (electrons or holes) between the source and drain terminals.
https://www.britannica.com/science/gate-voltage

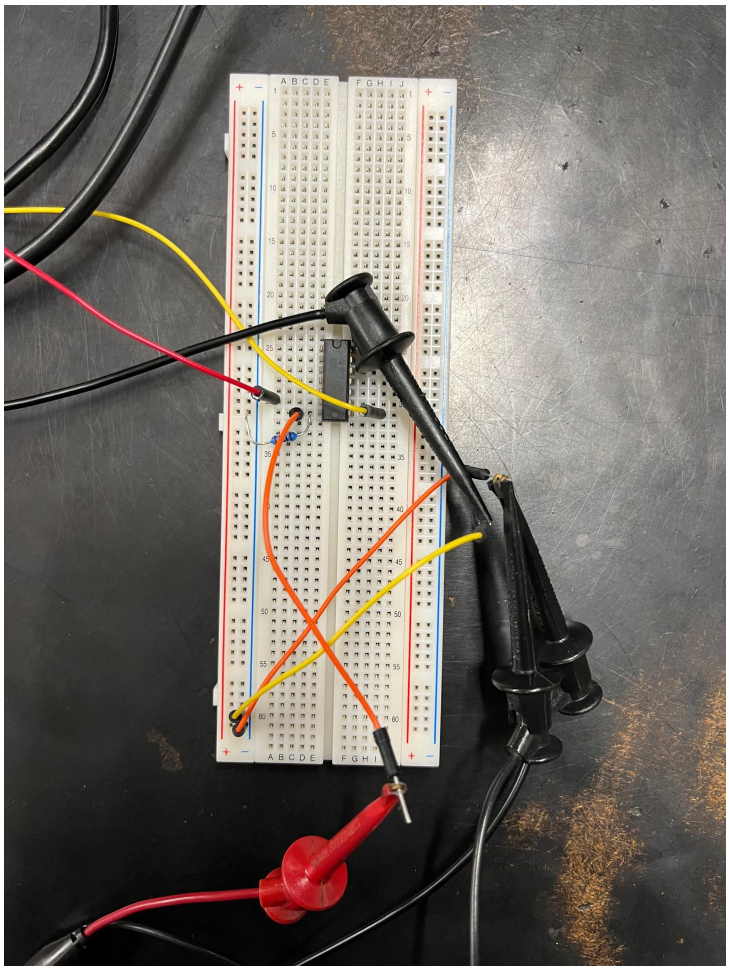
Drain voltage - refers to the voltage applied to the drain terminal of a transistor, influencing the current flowing through the transistor.
https://www.everythingpe.com/.

Conductance coefficient- refers to the voltage applied to the drain terminal of a transistor, influencing the current flowing through the transistor.
https://www.techtarget.com/searchnetworking/definition/conductance

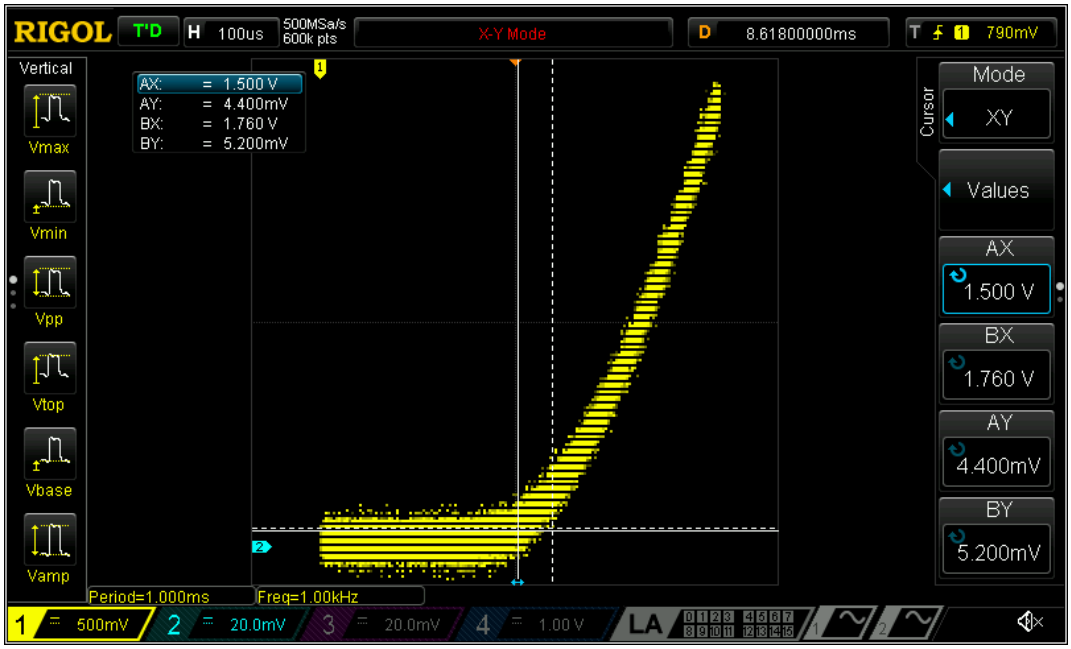
Motivation for experiment

The motivation behind this lab is to expand our understanding in what is one of the most important innovations in computer circuits, the MOSFET transistor. By studying concepts such as the gate voltage, drain voltage, and operating modes (specifically triode and saturation modes) we gain an understanding of how this type of component works in the real world. This is not only important to this class, but has applications as a gateway into the world of electronics. This experiment is motivated by the need to understand and comprehend the behavior of MOSFETs in a real world environment. It branches the theoretical to the real world.

1 Experimental Diagram



PLOT – NMOS IV curve vs. Gate voltage (with input)



Analysis

Referring to the plot above, we can find the gate threshold voltage where the curve starts increasing. The gate voltage threshold seems to be 1.5v which is where the graph begins to trend upwards, this is about half of the input voltage.

Solving for coefficient K

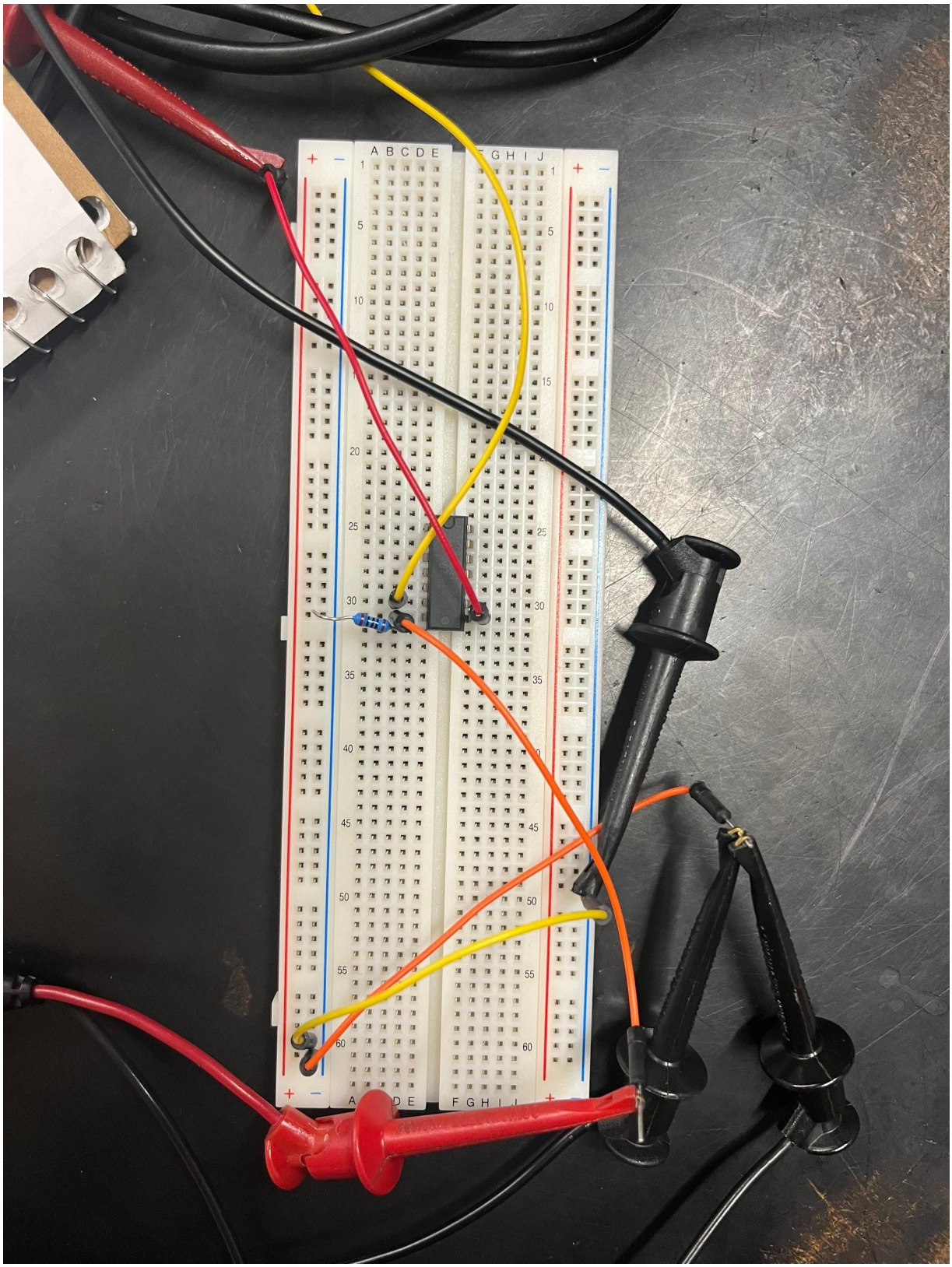
$I_{ds} = \frac{K}{2}(Vgs - Vth)^2$

$Vgs = 140mv\ (input\ voltage)$

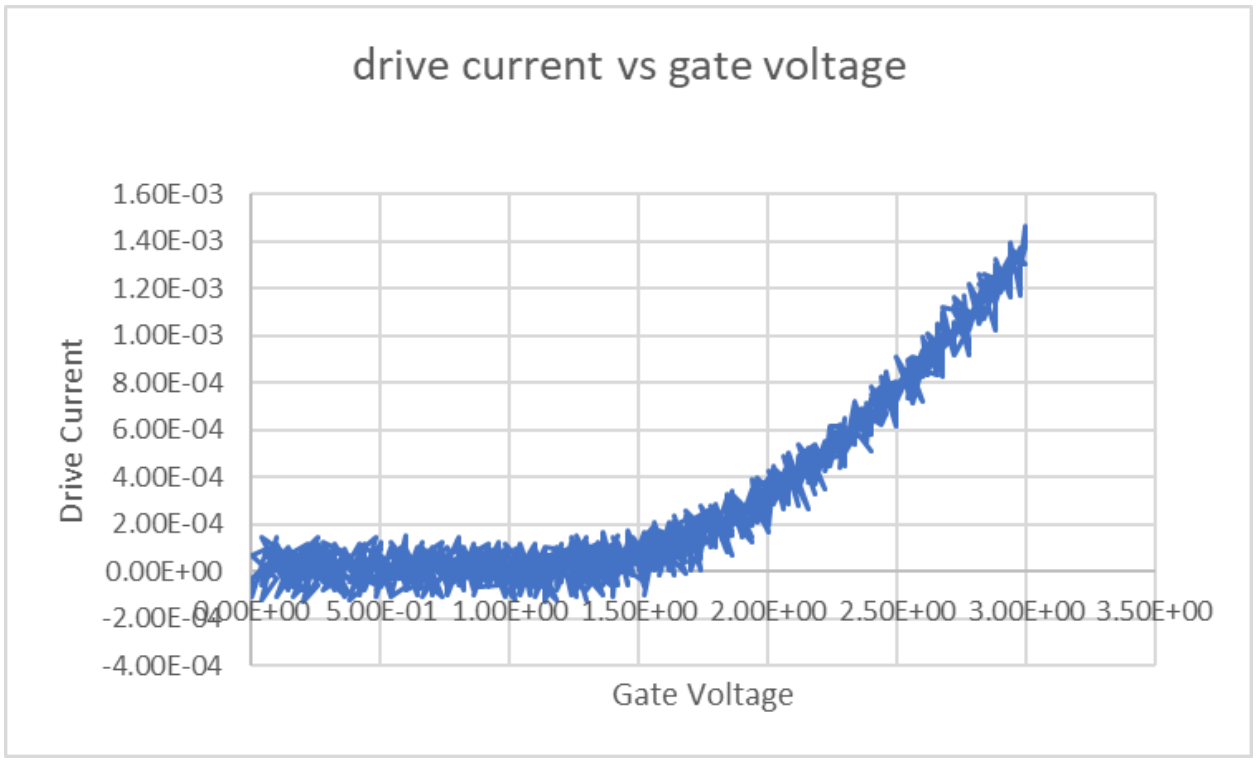
$Vth = 1.5V\ (by\ plot\ analysis)$

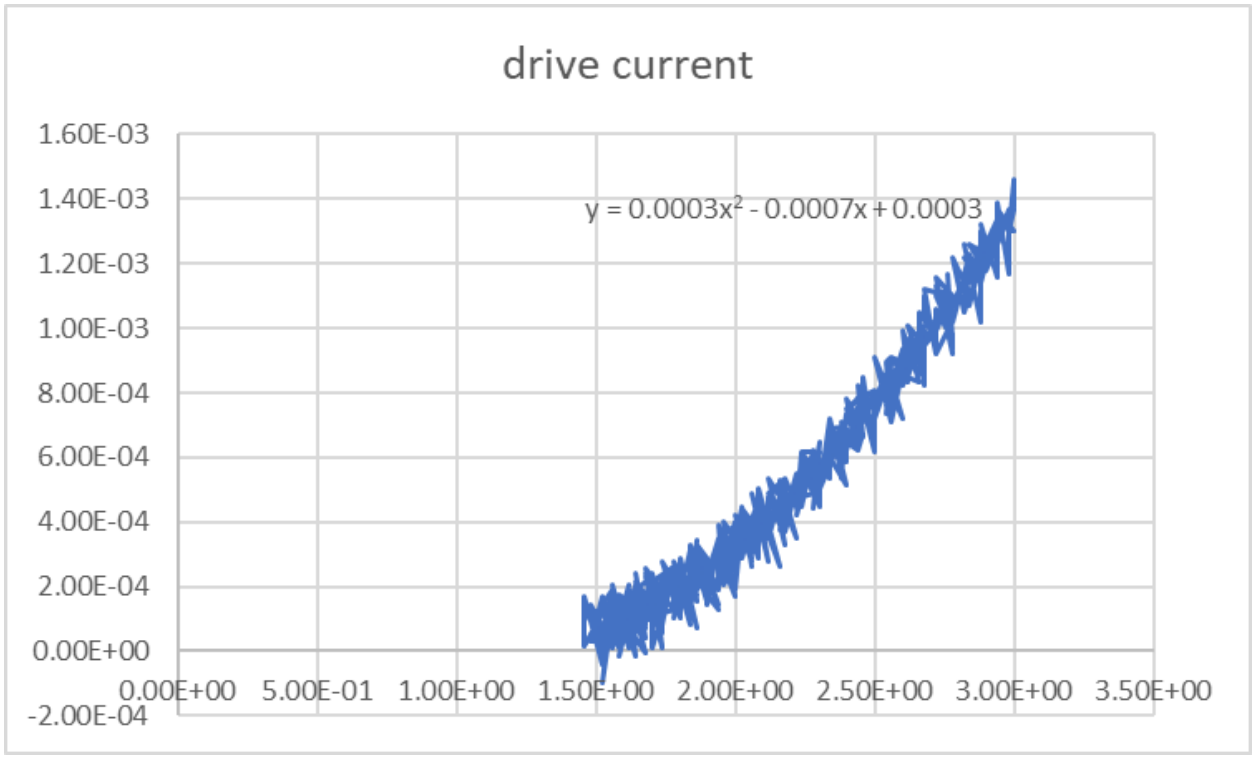
$Ids \ --> \ V = IR \ --> \frac{140mV}{100\ ohm} = 0.0011\ A/V^2$

2 Experimental diagram



2 PLOT – NMOS IV curves vs. Drain Voltage (with input)





Analysis

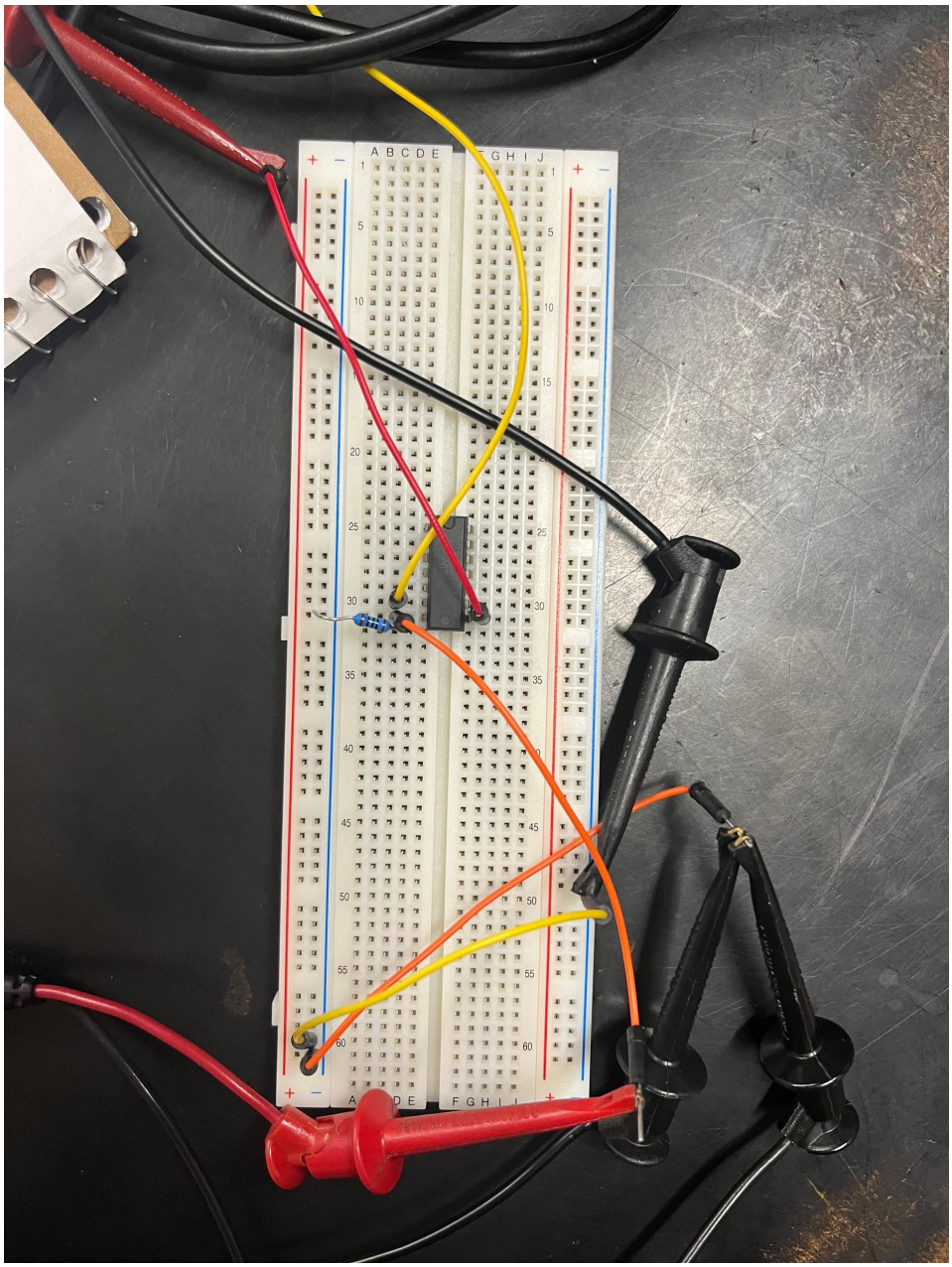
-From the circuit, after moving the triangle wave input and the power supply, we were able to plot this current versus Drain voltage curve. After some time, the input signal changes from linear to a slope of zero.

-Reducing the triangle wave signal, we can cut off the signal before it hits its maximum, providing a nice linear relationship (triode)

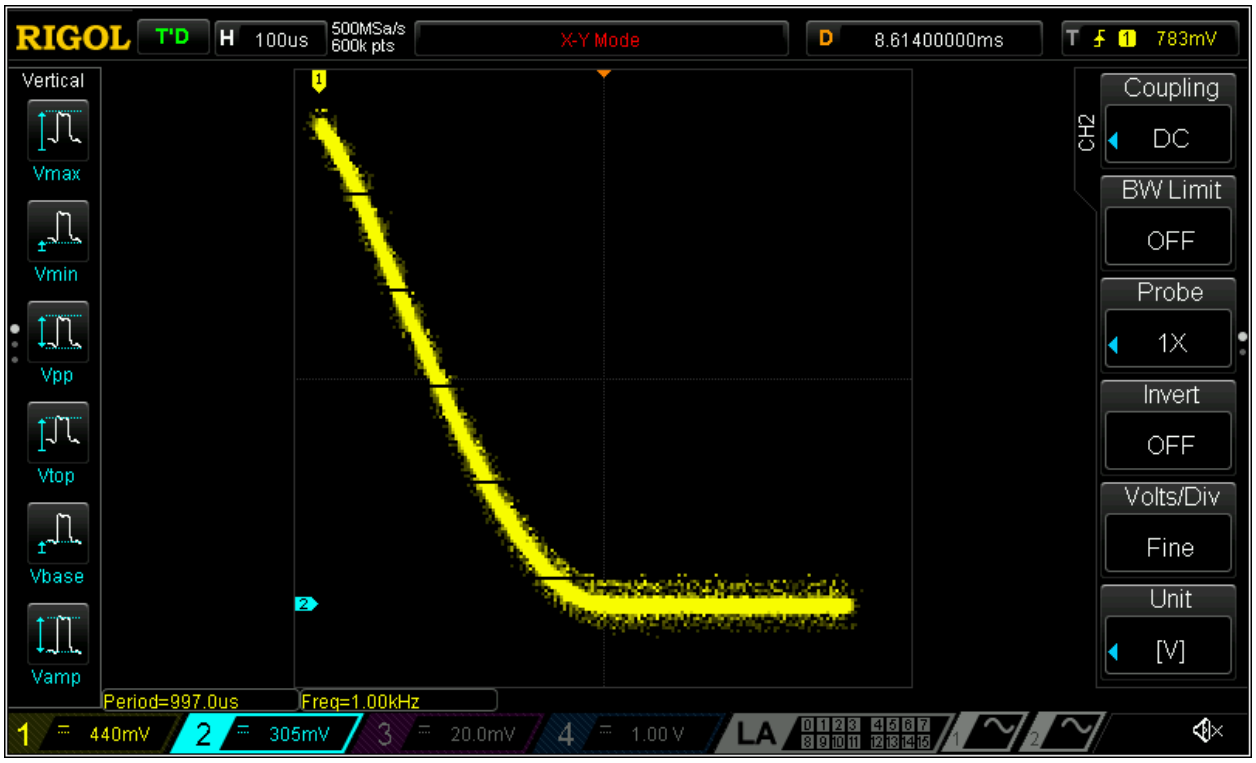
Using the above triode regime curve from the plot, we can estimate the conductance coefficient K

$Ids = 140mV/100\ ohms = 0.0014A$
$Vgs = 3V\ (input\ voltage)$
$Vth = 1.5\ (plot\ analysis)$
$Vds = 3\ (gate\ to\ source\ voltage)$
$Ids = Kn\,(Vgs - Vtn)\,Vds \ ---> \ 0.0014 = Kn\,(3 - 1.5) \times 3$
$Kn = 0.0016\ A/V^2$

3 Experimental Diagram (drawing + PICTURE with labels)



PLOT – PMOS IV curve vs. Gate voltage (with input)



Gate Voltage	Saturation Current mA
3	.140
2.5	.078
2	.033
1.5	.007
1	0
0	0

Analysis

Referencing the first part, we already estimated the Vtp of the circuit to be 1.5V. On the curve, 1.5 is where the slope changes from zero to linear.

Conclusion

In part 1 we measured the voltage threshold and got a value of 1.5v the same as the advertised value. Using this value and the input voltage we calculated the value of K with this formula $I_{ds} = \frac{K}{2}(Vgs - Vth)^2$, plugging in we get $Ids \; --> \; V = IR \; --> \frac{140mV}{100\,ohm} = 0.0011\,A/V^2$. for part 2 we plotted the current versus Drain voltage curve so we can visually see the behavior of the MOSFET as the current rose and fell. Using this information again we can plug into this equation $Ids = Kn\,(Vgs - Vtn)\,Vds \; --->\; 0.0014 = Kn\,(3 - 1.5) \times 3$ to get a Kn value of .0016 A/V^2. Finally in part 3 we measured the saturation current at various gate voltages, to see how voltage affects the current through the MOSFET. Overall, In this experiment we had the opportunity to gain hands-on experience with NMOS and PMOS transistors, which reinforced our understanding of their behavior. We plotted IV curves that illustrate the operation of the components and how the gate and voltage drain impacted it. The experiment showed us how to measure important parameters like the threshold voltage and conductance coefficient (K) which play an essential role in the transistor's functionality. In particular we saw how the values change between triode and saturation modes. With PMOS devices we further explored the role of electron absence or holes and the importance of voltage manipulation relative to a high source. The law expanded our understanding of MOSFETs beyond theory and brought it into the real world.