# UMass ECE 210 – Fall 2023

## Lab 9: CMOS inverter

**Concepts:**

- CMOS Inverter transfer curve
- CMOS noise margins
- CMOS power dissipation

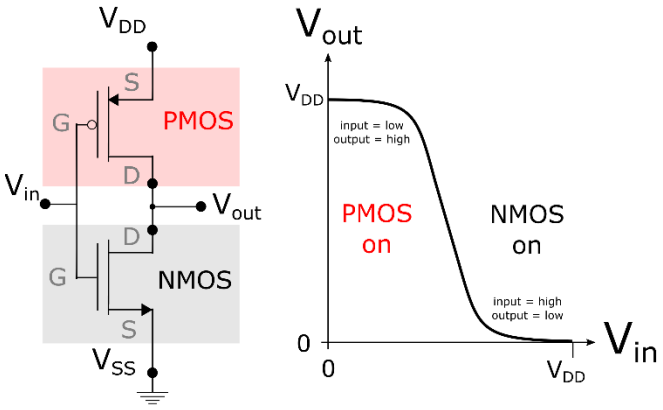
**DATA required for Lab report:**

| |
|---|
| PLOT – Output of CMOS transfer curve |
| TABLE – Noise margins for CMOS device from transfer curve |
| PLOT – Output of CMOS transfer curve WITH power dissipation |

The Complementary Metal Oxide Semiconductor (CMOS) inverter forms the basis for all logical functions in digital electronics and is composed of 'complementary' pair of MOSFETs (Field Effect Transistors), one positive (PMOS) and one negative (NMOS).

**CMOS Transfer Curve Characteristic**

Below is a rough voltage transfer characteristic ($V_{out}$ vs. $V_{in}$) of the CMOS inverter.
Showing how when the gate voltage is low the PMOS is on but the NMOS is off and when the gate voltage is high the PMOS turns off but the NMOS turns on. Together, they're only 'on' for a brief period in the middle when the gate is not high nor low and both are partially on.

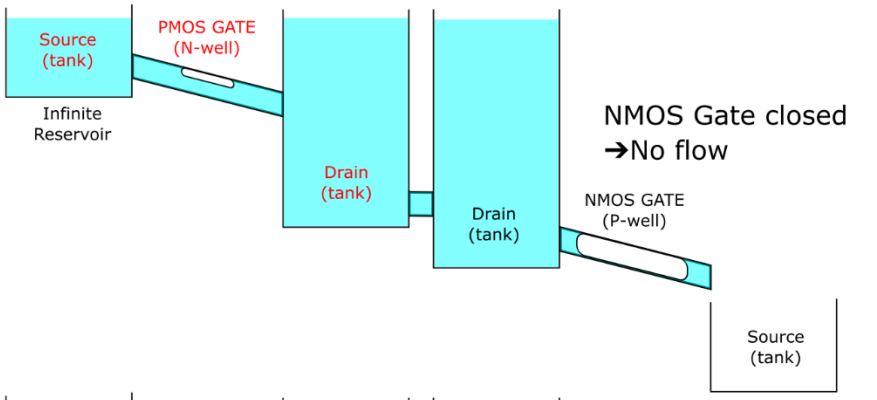



| Input ($V_{in}$) | PMOS | NMOS | Output ($V_{out}$) |
|---|---|---|---|
| 'High' ($V_{DD}$) | OFF | ON | 'Low' (zero) |
| 'Low' (zero) | ON | OFF | 'High' ($V_{DD}$) |

The PMOS is 'off' for a high input voltage and 'on' for a low input.
The NMOS is 'on' for a high input and 'off' for a low input.
So, the CMOS pair is 'off' for both high and low inputs and therefore uses very little power.

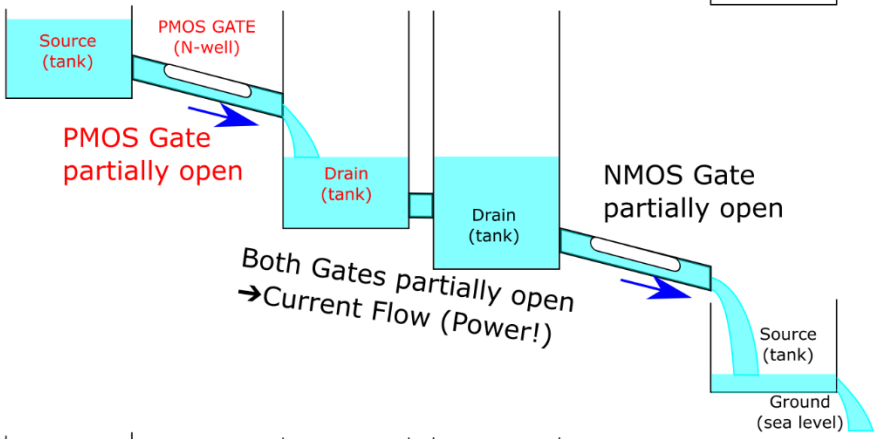
## Water/Hydraulic Analogy:

To understand how a CMOS inverter works we can use an analogy with water.
Where voltage is analogous to the water pressure (shown by the height of the water in each tank).
Each gate is a valve. In CMOS only one of the gates is fully open at a time. So if the PMOS is fully open then the NMOS is closed, reducing static power consumption.



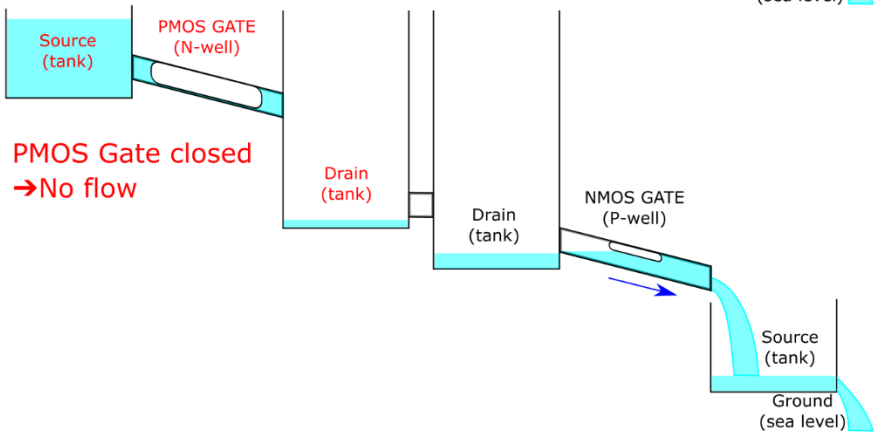

**Gate Input = 0V:**

PMOS on
NMOS off
Output=$V_{DD}$
No current flow
No power dissipation




**Gate input = $V_{DD}/2$:**

PMOS partially on
NMOS partially on
Output ~$V_{DD}/2$
Current flowing
Power dissipated




**Gate input = $V_{DD}$:**

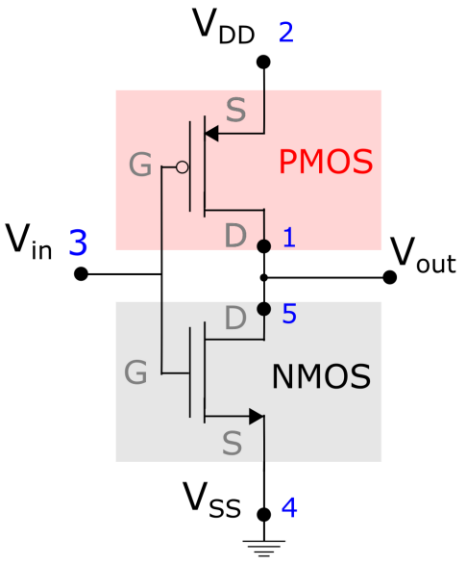
PMOS off
NMOS on
Output=0V
No current flow
No power dissipation

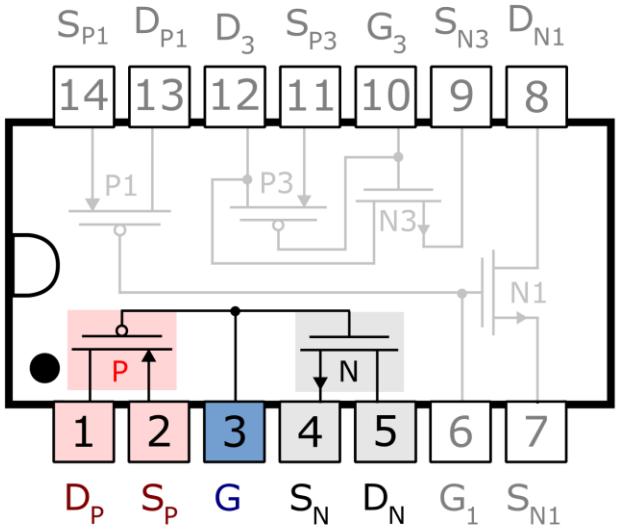
## Building a CMOS Inverter with the CD4007:

1. Insert a CD4007 into your breadboard
2. Supply 5V to $V_{DD}$ (pin 2)
3. Ground $V_{SS}$ (pin 4)
4. Ground the substrate (pin 7)
5. Send in a square wave (min=0V, max=5V) to the gate input $V_{in}$ (pin 3)
6. Monitor the input square wave on oscilloscope Ch1

7. Connect the drains with a wire (pins 1 and pin 5)
8. Measure the output (pin 1 or 5) on oscilloscope Ch2

9. Verify the output is the inverse of the input.
10. Record your measurements of the input and output inverting




## Measure the Transfer Curve:

To measure the Transfer Curve we will use a triangle wave to sweep $V_{in}$.

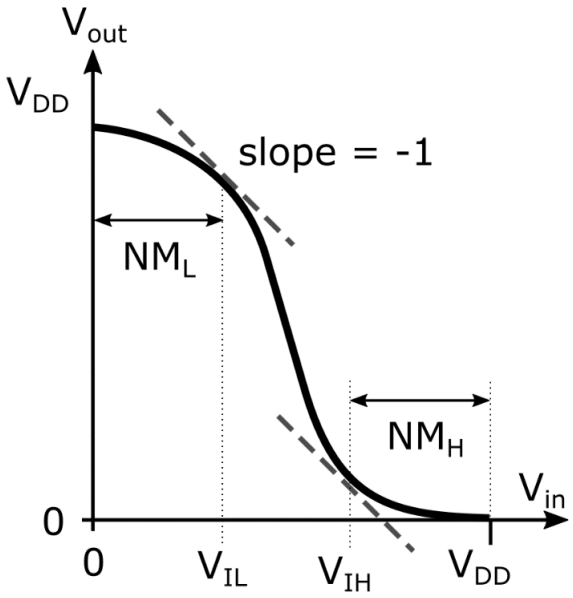
1. Change your square wave to a triangle ramp
2. Set the frequency to f=1kHz

3. Change your oscilloscope from YT mode to XY mode by pressing HORIZONTAL>MENU>TIME BASE> XY.
   Now Ch1 is the horizontal axis (X) and Ch2 is the vertical axis (Y).

4. Record the transfer curve and the Noise margins (details below)

**Measure Noise Margins:**

Find the low and high noise margins ($N_{ML}$ , $N_{MH}$) from your measured transfer characteristic.
You will need to ROUGHLY estimate where the slope of the curve equals -1.
This tells us how robust the inverter is to noise on the gate input before flipping incorrectly.




*The output high voltage is $V_{OH} = V_{DD}$* *$V_{IH}$ is the input voltage where the slope = -1*

The noise margin high ($N_{MH}$) is the difference: $N_{MH} = V_{OH} - V_{IH}$

*The output low voltage is $V_{OL} = 0$* *$V_{IL}$ is the input voltage where the slope = -1*

The noise margin low ($N_{ML}$) is the difference: $N_{ML} = V_{IL} - V_{OL}$

*See Section 5.1 in the Agarwal textbook for more discussion of noise margin.*

*Note the subscripts referring to either $V_I$ or $V_O$ ( IN or OUT)*

$V_O$ is the output voltage value (y axis)

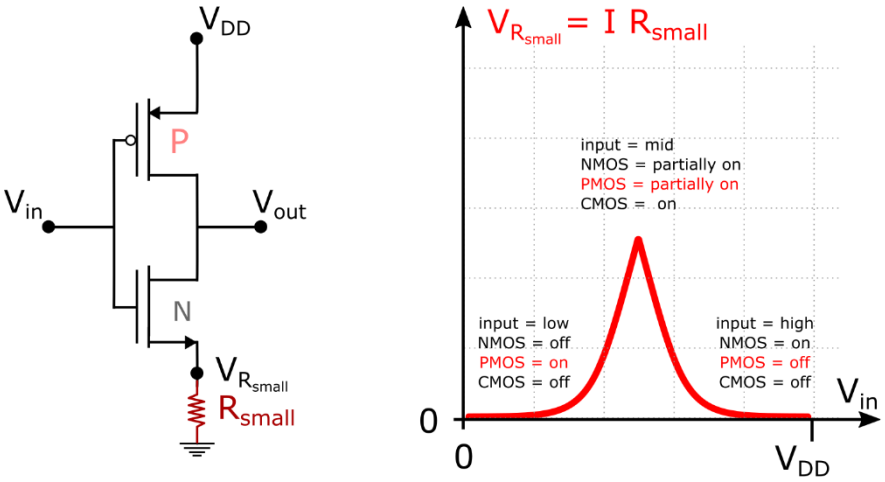
$V_I$ is the input voltage value (x axis)

## RECORD A TABLE of:

$V_{IH}$, $V_{IL}$ and the low and high noise margins $N_{ML}$, $N_{MH}$

**Measuring CMOS maximum power dissipation**

Next, we want to measure the maximum power of the CMOS inverter during the transfer curve. To do this we will add a small resistor $R_{small}$ in series with the circuit, turning the current into a voltage that we can plot on the oscilloscope. Then calculating power from $P = I \cdot V$.




It is easiest to measure this voltage relative to ground, so we will add the small resistance $R_{small}$ between the circuit and ground.

$R_{small}$ must be small compared to the resistance of the CMOS inverter when it is partially on. We've already seen that the NMOS alone will be about $R_{on}^{NMOS}$~300 Ω 'on', and expect PMOS to be similar. Plus, we know that in the 'partially on' state each will have a higher resistance.

$$R_{on}^{CMOS} > R_{on,partial}^{PMOS} + R_{on,partial}^{NMOS}$$

Therefore, $R_{small}$ should be less than 1kΩ and we can use ~100Ω without changing $V_{ss}$. Record your value of $R_{small}$ and add it to the circuit.

Now you should be able to monitor $V_{R_{small}}$ to see the current spike during the sweep of the transfer curve, when the PMOS and NMOS are both partially on.

1. RECORD the current vs input voltage of the triangle wave from the signal generator.
2. Estimate the maximum power dissipation during the transfer curve.
3. What is the power dissipation in the off state? On state?

**LAB REPORT DUE NEXT WEEK**

Start outlining report. Do you have all the data you need?
Do you need to take pictures of your circuits?
DETAILED RUBRIC ON NEXT PAGE

# Lab Report 9 – Rubric

**2,000-word limit  1 report/group**

| | | Points | Grade |
|---|---|---|---|
| | Introduce and define concepts (with citations) | 5 | |
| | Motivation for experiment | 5 | |
| **1** | Experimental Diagram (drawing + PICTURE with labels) | 5 | |
| | PLOT – **CMOS Inverter Transfer Curve** (with input) | 5 | |
| | Analysis (remember to show your work for calculations) | 5 | |
| **2** | TABLE – **Noise Margins from Transfer Curve** | 5 | |
| | Analysis (remember to show your work for calculations) | 5 | |
| **3** | Experimental Diagram (drawing + PICTURE with labels) | 5 | |
| | PLOT – **Power dissipation of CMOS inverter** (with input) | 5 | |
| | Analysis (remember to show your work for calculations) | 5 | |
| | Conclusion | 5 | |
| | | 55 | |