ECE 331 – Fall 2024
Homework 6
Assigned Monday, November 8
Due Monday, November 15

1. (35 pts.) For the following sequential list of 32-bit memory address references,

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   20, 43, 22, 180, 88, 190, 13, 189, 44, 186, 181, 255
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   given as byte addresses, consider byte addressable memory to answer the following questions.

   a. For each of the references, for an initially empty direct-mapped cache with 16 32-bit word blocks, complete the following table with the binary address, tag, and index. The tag and index should be given as decimal values and a simple H or M can be used to indicate a cache *Hit* or *Miss*.

Byte Address	Binary Address	Tag	Index	Hit/ Miss
20				
43				
22				
180				
88				
190				
13				
189				
44				
186				
181				
255				

b. For each of the references, for an initially empty direct-mapped cache with 8 64-bit word blocks, complete the following table with the binary address, tag, and index.

Byte Address	Binary Address	Tag	Index	Hit/ Miss
20				
43				
22				
180				
88				
190				
13				
189				
44				
186				
181				
255				

c. If the cache can only hold 8-words of data (32 bytes), for three possible configurations of the cache: i.) cache C1 has 1-word blocks, ii.) cache C2 has 2-word blocks, and iii.) C3 has 4-word blocks, complete the following table:

		C1		C2		C3	
Byte Address	Tag	Index	Hit/ Miss	Index	Hit/ Miss	Index	Hit/ Miss
20							
43							
22							
180							
88							
190							
13							
189							
44							
186							
181							
255							

d. For part (c) above, in terms of miss rate, which cache design is the best?

e. For part (c) above, if the miss stall time is 30 cycles and the access times for the caches are: 2 cycles for C1, 4 cycles for C2 and 5 cycles for C3, determine the average memory access time for each Cache architecture, and based on this evaluation, state which one has the best performance.

2. (35 pts.) Assuming that main memory access time takes 50 ns and that memory accesses are 30% of all instructions, if the following table shows data for L1 caches for two different processors, P1 and P2,

Processor	L1 Size	L1 Miss Rate	L1 hit time
P1	2 kB	8.5 %	0.4 ns
P2	4 kB	5.0 %	0.8 ns

a. Assuming that the L1 hit time determines the cycle times for P1 and P2, what are the clock rates of these two processors?

b. What is the Average Memory Access Time (AMAT) for P1 and P2?

c. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster?

For the next three problems, consider the addition of an L2 cache to P1 in order to help make up for its limited L1 cache capacity. Use the L1 cache capacities and hit times from the previous table.

Processor	L2 Size	L2 Miss Rate	L2 Hit Time
P1	1 MB	1.1%	5.0 ns

d. What is the AMAT for P1 with the addition of the L2 cache? Is this better or worse with the L2 cache?

e. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?

f. Now that P1 has an L2 cache, Which processor is faster? If P1 is faster, what miss rate would P2 need in its L1 cache to match P1's performance? If P2 is faster, what miss rate would P1 need in its L1 cache to match P2's performance?

3. (30 pts.) Patterson and Hennessy (ZyBooks) exercise 5.5